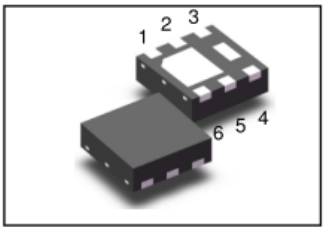
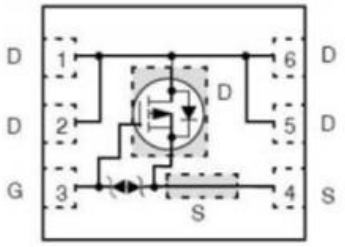
LP3218DT1G

12V P-Channel Enhancement MOSFET





Pin configuration (Top view)

1. FEATURES

- Low Profile DFN 2.0x2.0x0.62 mm for Board Space Saving
- Ultra Low RDS(on)
- ESD Diode.Protected Gate
- This is a Pb-Free Device
- We declare that the material of product are Halogen Free and compliance with RoHS requirements.

2.APPLICATIONS

- Battery Switch
- High Side Load Switch

3. ORDERING INFORMATION

Device	Marking	Shipping
LP3218DT1G	32	4000/Tape&Reel

4. MAXIMUM RATINGS(Ta = 25ºC unless otherwise stated)

Parameter	Symbol	Limits	Unit
Drain−to−Source Voltage	VDSS	12	V
Gate−to−Source Voltage	VGS	±8	V
Drain Current (Note 1)Steady State	ID	8.2	A
Pulsed Drain Current (tp = 10 μs)	IDM	25	A
Power Dissipation (Note 1) Steady State t < 7 s	PD	 1.7 3.8	W
Operating Junction and Storage Temperature Range	TJ , TSTG	−55 ~ +150	ºC
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)	TL	260	ºC
Gate−Source ESD Rating (HBM, Method 3015)	ESD	2000	V

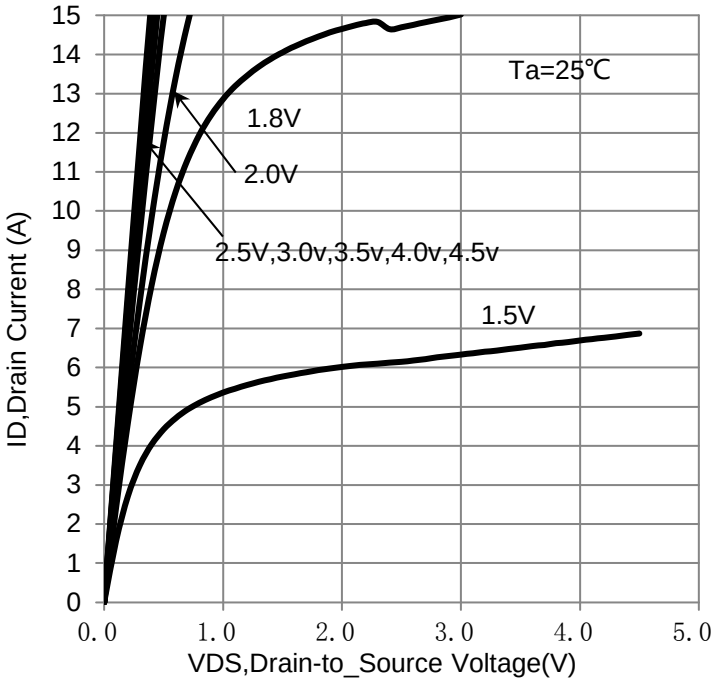
1. Surface−mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces)

5. ELECTRICAL CHARACTERISTICS

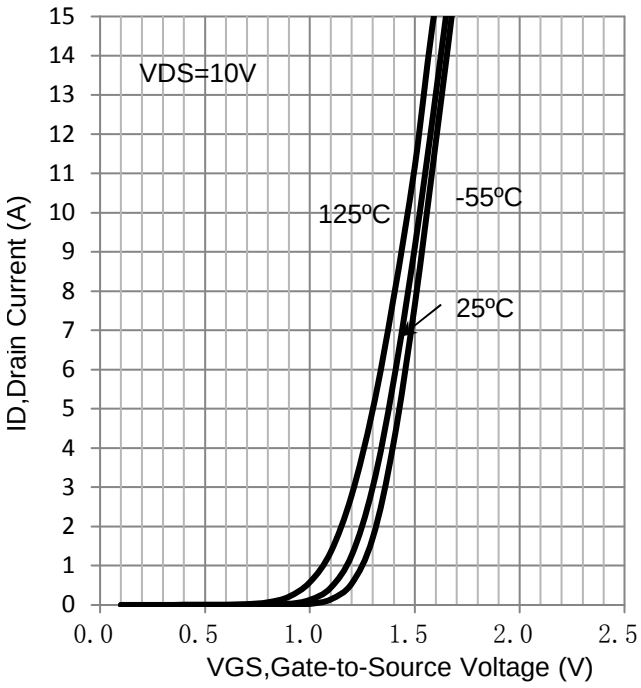
Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
NMOSFET							
Drain-Source Breakdown Voltage	V(BR)DSS	VGS = 0 V, ID = 250 μA		-12			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	V(BR)DSS /TJ				10		mV/°C
Zero Gate Voltage Drain Curren	IDSS	VGS = 0 V, VDS = -20 V	TJ = 25°C			-1	μA
Gate−to−Source Leakage Current	IGSS	VDS = 0 V, VGS = ±5 V		-0.4		±5	μA
Gate Threshold Voltage (Note2)	VGS(TH)	VGS = V DS , ID = 250 μA				-1	V
Negative Threshold Temperature Coefficient (Note2)	VGS(TH) /TJ				3.0		mV/°C
Drain−to−Source On Resistance (Note2)	RDS(on)	VGS = -4.5 V, ID = -7 A			14.6	18	mΩ
		VGS = -2.5 V, ID = -5 A			19	25	
		VGS = -1.8 V, ID = -3 A			25	50	
		VGS = -1.5 V, ID = -1 A			40	90	
Forward Transconductance (Note2)	gFS	VDS = -5 V, ID = -3A			40		S
Input Capacitance	CISS	VGS = 0 V, f = 1 MHz, VDS = -15 V			2240		pF
Output Capacitance	COSS				240		
Reverse Transfer Capacitance	CRSS				210		
Total Gate Charge	QG(TOT)	VGS = -4.5 V, VDS = -15 V; ID = -4A			28		nC
Threshold Gate Charge	QG(TH)				1.0		
Gate−to−Source Charge	QGS				2.9		
Gate−to−Drain Charge	QGD				8.8		
Turn−On Delay Time (Note3)	td(ON)	VGS = -4.5 V, VDD = -15 V; ID = -4A, RG = 1Ω			8.6		ns
Rise Time (Note3)	tr				15		
Turn−Off Delay Time (Note3)	td(OFF)				150		
Fall Time (Note3)	tf				88		
Forward Diode Voltage	VSD	VGS = 0 V, IS = -1A	TJ = 25°C		0.63	1	V
			TJ = 125°C		0.5		

2. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%
3. Switching characteristics are independent of operating junction temperatures

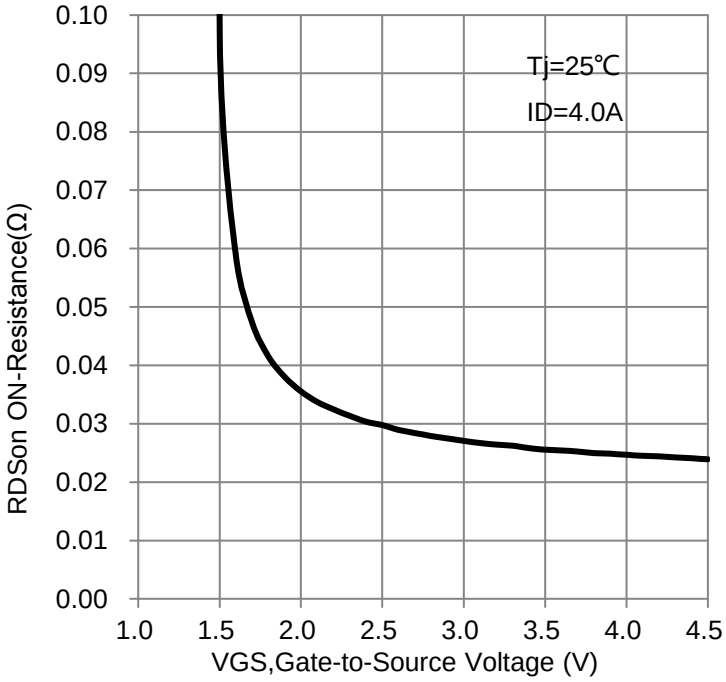
6.ELECTRICAL CHARACTERISTICS CURVES



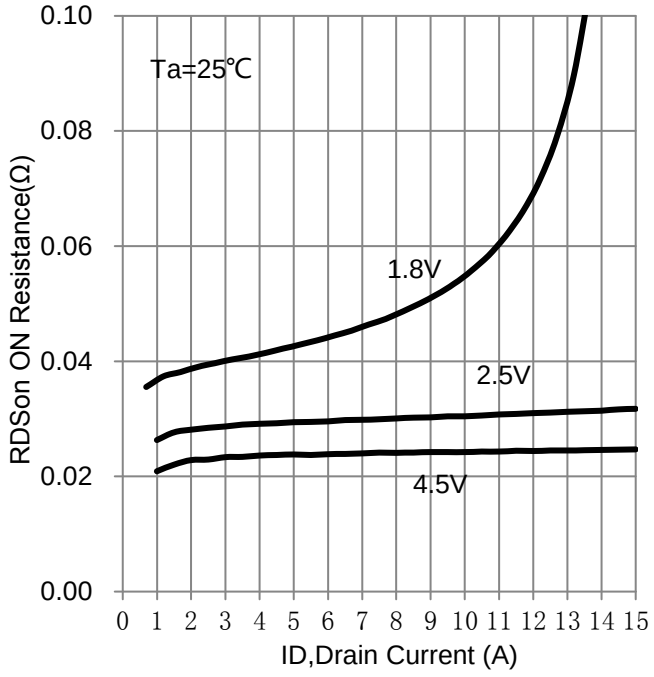
On-Region Characteristics



Transfer Characteristics

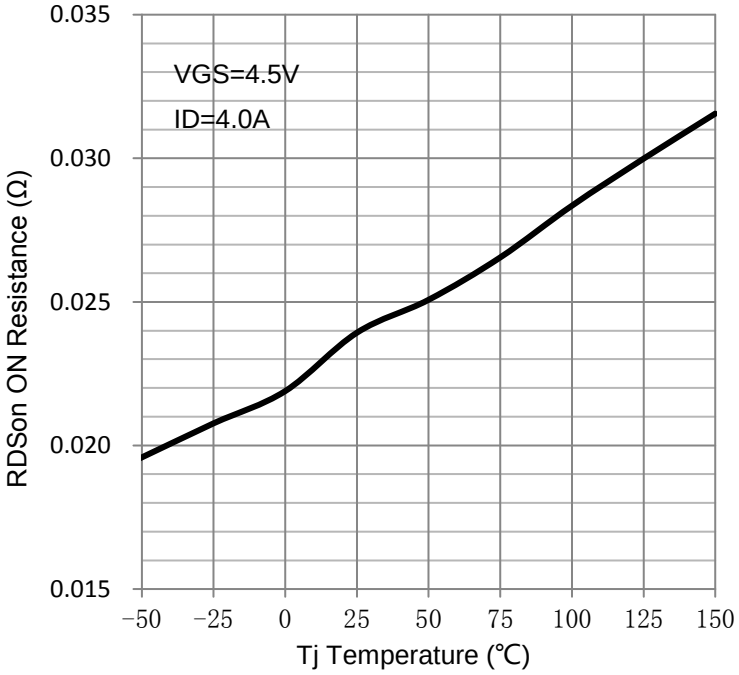


On-Resistance vs. Gate-to-Source Voltage

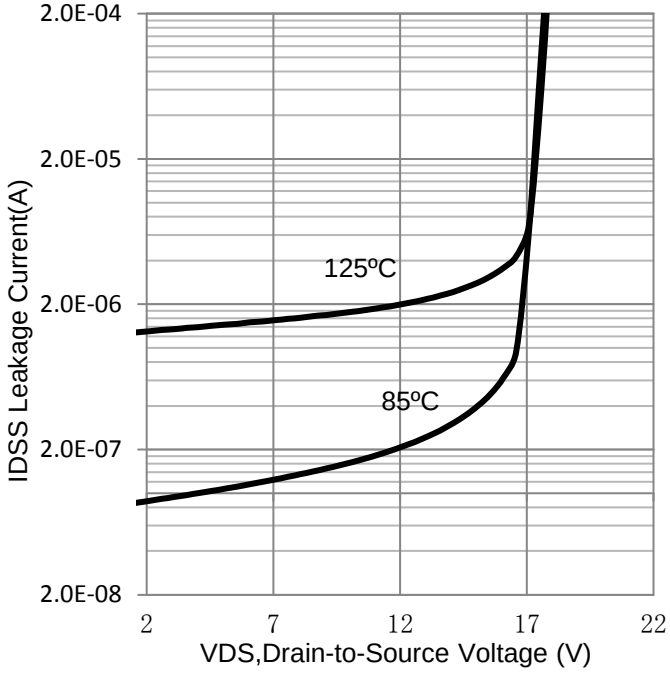


On-Resistance vs. Drain Current and Gate Voltage

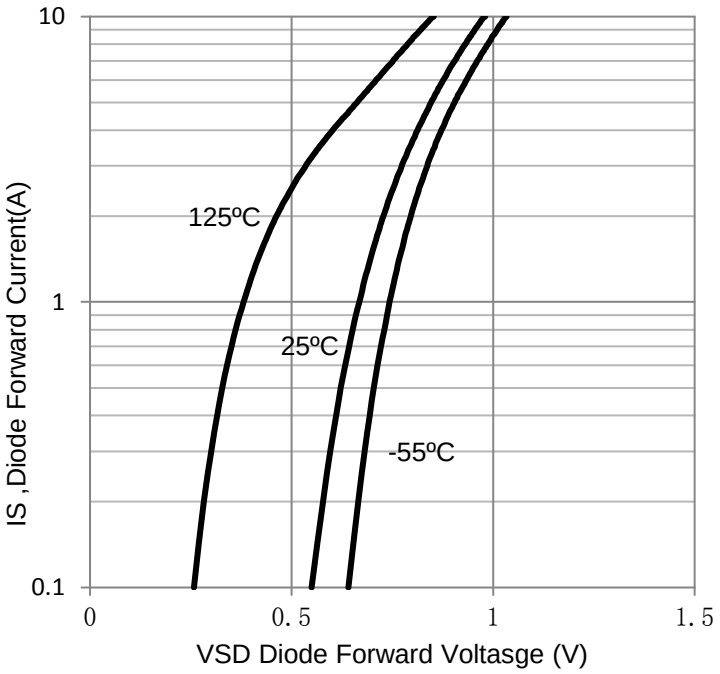
6.ELECTRICAL CHARACTERISTICS CURVES（Con.）



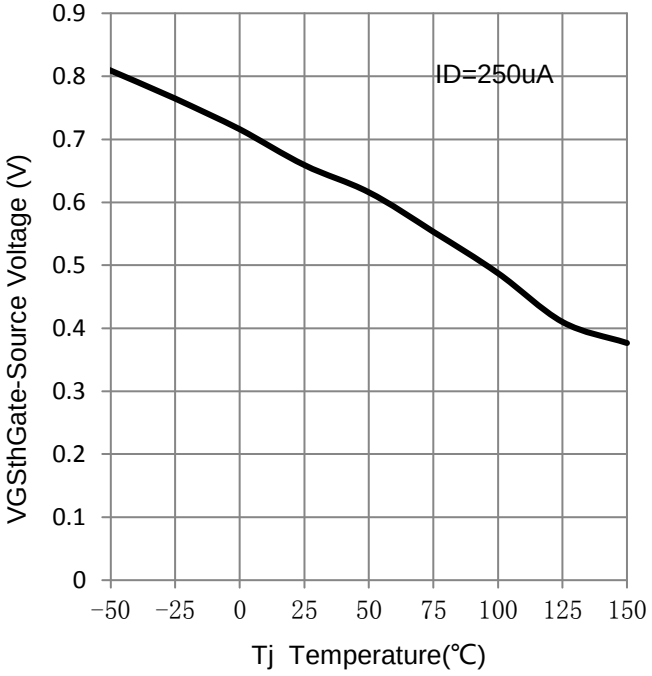
On-Resistance Variation with Temperature



Drain-to-Source Leakage Current vs. Voltage

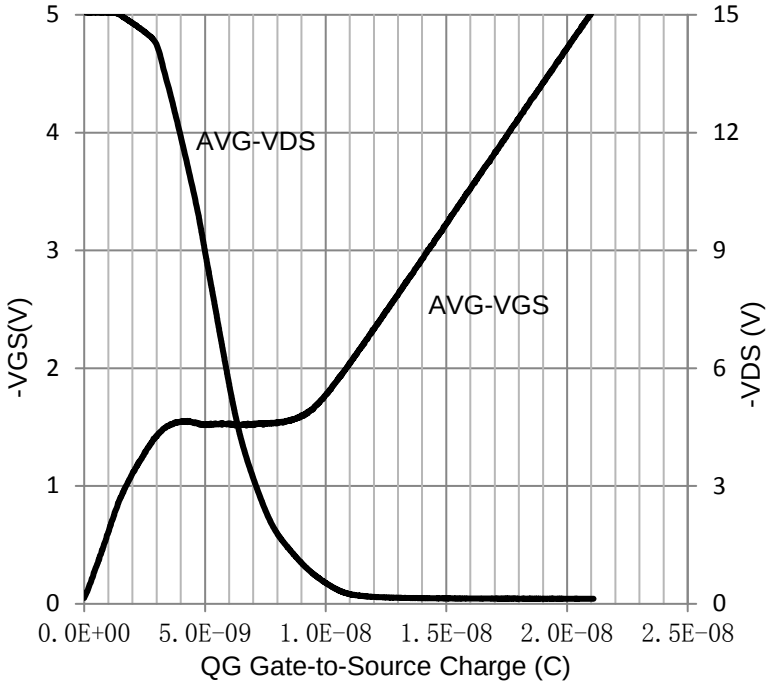


Diode Forward Voltage vs. Current

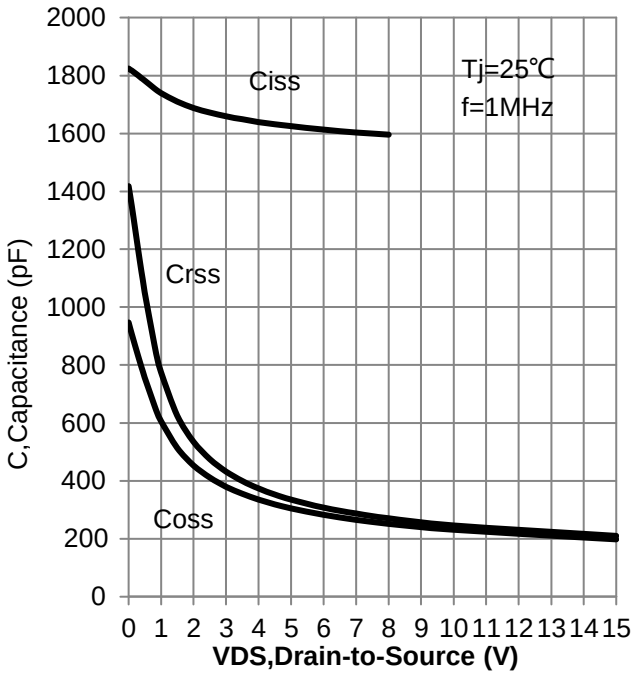


Threshold Voltage

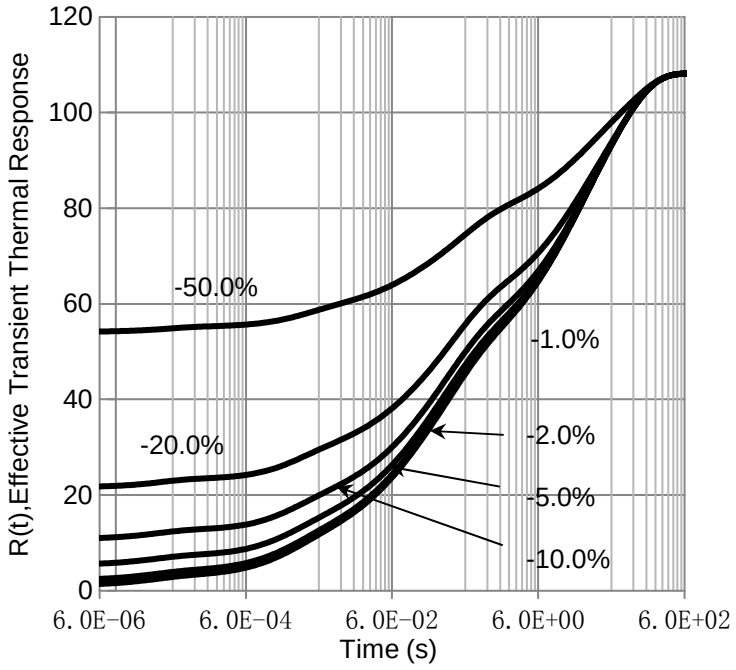
6.ELECTRICAL CHARACTERISTICS CURVES（Con.）



Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

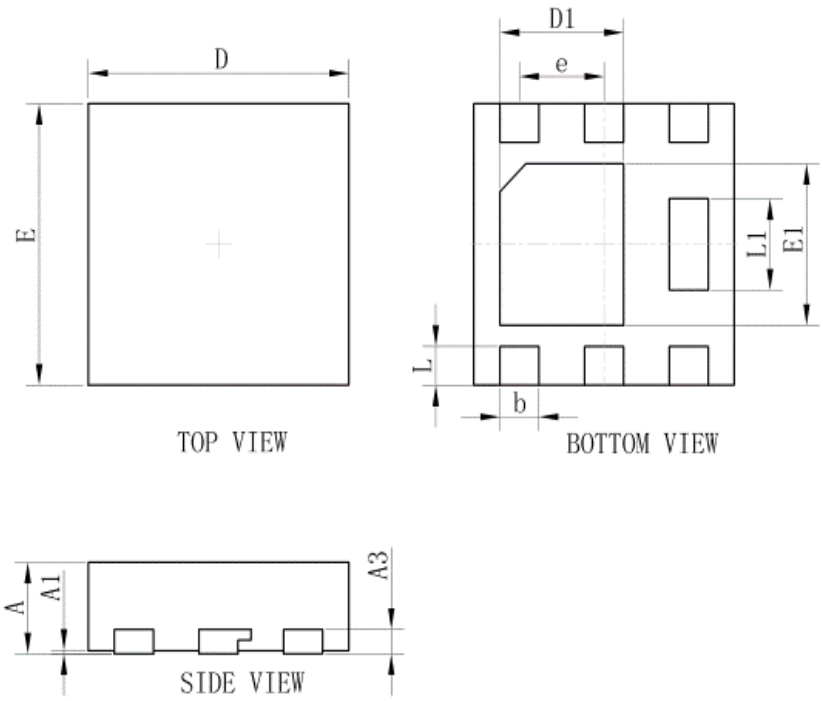


Capacitance variation



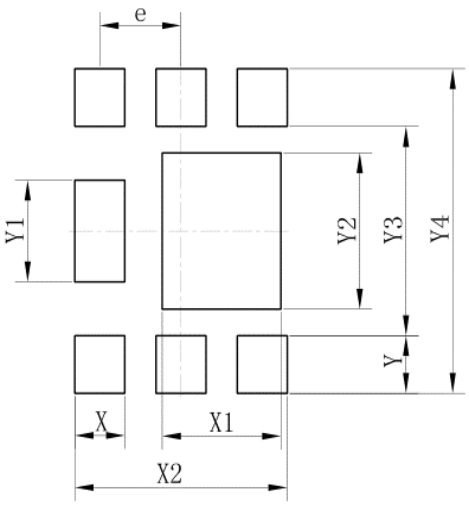
FET Thermal Response

7.OUTLINE AND DIMENSIONS



DFN2020-6S			
DIM	MIN	NOR	MAX
A	0.60	0.65	0.70
A1	0.01	0.03	0.05
b	0.25	0.30	0.35
D	1.95	2.00	2.05
E	1.95	2.00	2.05
e	0.65TYP.		
L	0.23	0.28	0.33
L1	0.60	0.65	0.65
D1	0.90	0.95	1.00
E1	1.10	1.15	1.20
A3	0.152REF		
All Dimensions in mm			

8.SOLDERING FOOTPRINT



DFN2020-6S	
Dim	(mm)
X	0.40
X1	0.95
X2	1.70
e	0.65
Y	0.43
Y1	0.75
Y2	1.15
Y3	1.54
Y4	2.39