

SE30P50

P-Channel Enhancement-Mode MOSFET

Revision: A

General Description

Thigh Density Cell Design For Ultra Low On-Resistance Fully Characterized Avalanche Voltage and Current Improved Shoot-Through FOM

- Simple Drive Requirement
- Small Package Outline
- Surface Mount Device

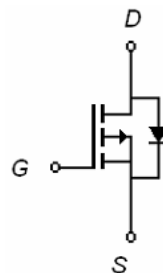
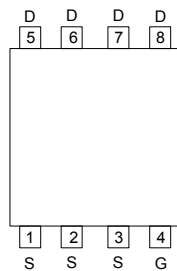
Features

For a single MOSFET

- $V_{DS} = -30V$
- $R_{DS(ON)} = 4.4m\Omega @ V_{GS}=-10 @ I_D=-20A$

Pin configurations

See Diagram below



Absolute Maximum Ratings

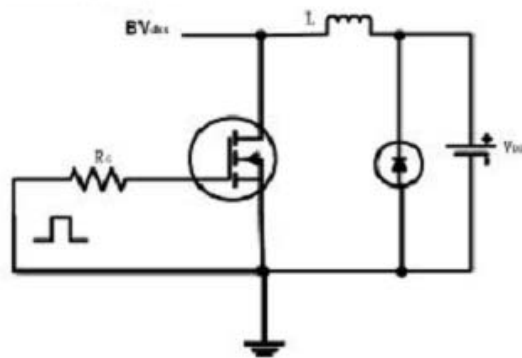
Parameter	Symbol	Rating	Units
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current	I_D	Continuous	-50
		Pulsed	-120
Total Power Dissipation	P_D	90	W
Operating Junction Temperature Range	T_J	-55 to 150	$^{\circ}C$

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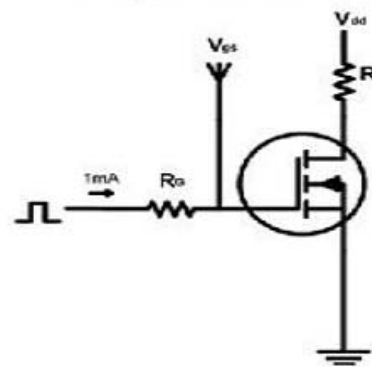
Electrical Characteristics (T _J =25°C unless otherwise noted)						
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS (Note 2)						
B _V DSS	Drain-Source Breakdown Voltage	I _D =-250μA, V _{GS} =0 V	-30			V
I _{DSS}	Drain to Source Leakage Current	V _{DS} = -30V, V _{GS} =0V			1	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =20 V			100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D =250μA	-1.2	-1.5	-2.2	V
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =-10V, I _D =-20A	-	4.4	7	mΩ
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =15V, f=1MHz		7032		pF
C _{oss}	Output Capacitance			898		pF
C _{rss}	Reverse Transfer Capacitance			743		pF
SWITCHING PARAMETERS						
Q _g	Total Gate Charge ²	V _{GS} =10V, V _{DS} =15V, I _D =30A		80		nC
Q _{gs}	Gate Source Charge			19		nC
Q _{gd}	Gate Drain Charge			38		nC
t _{d(on)}	Turn-On Delay Time	V _{GS} =10V, V _{DS} =15V, R _{GEN} =1Ω I _D =1A		20		ns
t _{d(off)}	Turn-Off Delay Time			80		ns
t _{d(r)}	Turn-On Rise Time			36		ns
t _{d(f)}	Turn-Off Fall Time			33		ns
Thermal Resistance						
Symbol	Parameter		Typ	Max		Units
R _{θJC}	Junction to Case		-	2		°C/W
R _{θJA}	Junction to Ambient (t ≤ 10s)		-	50		°C/W

Test Circuits and Waveform

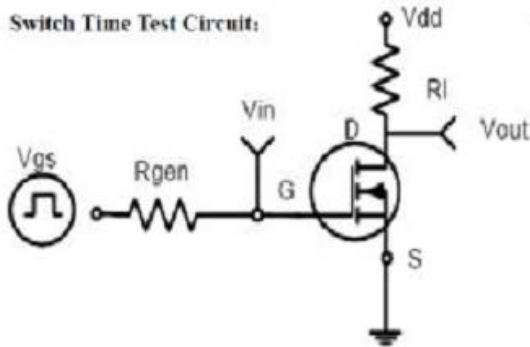
EAS test circuits:



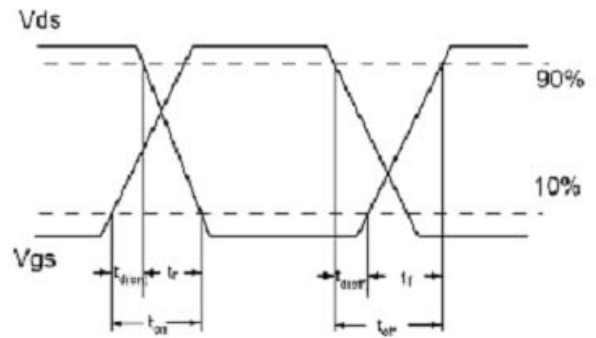
Gate charge test circuit:



Switch Time Test Circuit:



Waveforms:



Typical Characteristics

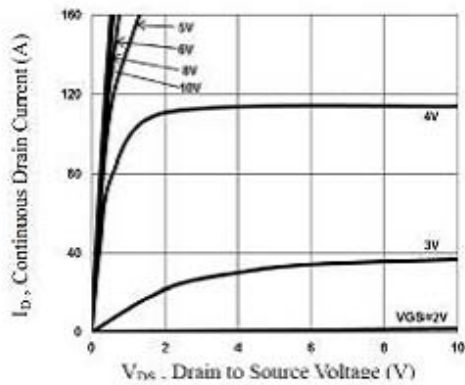


Figure 1: Typical Output Characteristics

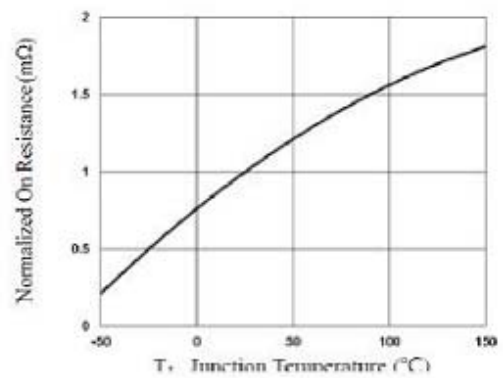


Figure 2: Normalized $R_{DS(on)}$ vs. T_J

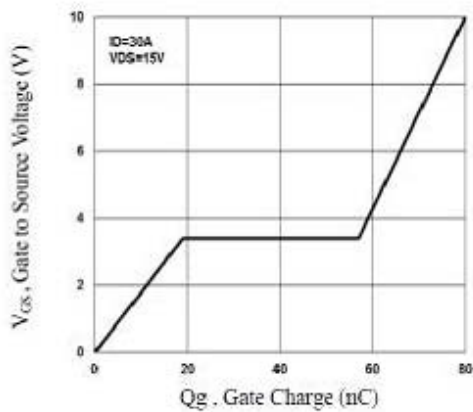


Figure 3: Gate-Charge Characteristics

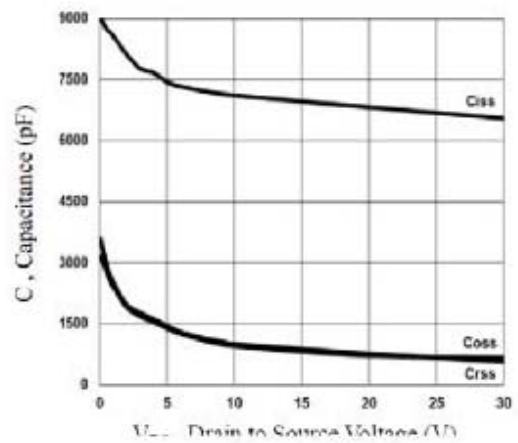


Figure 4: Capacitance Characteristics

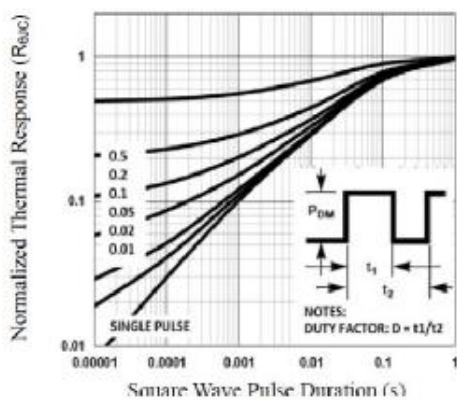


Figure 5: Normalized Thermal transient Impedance Curve

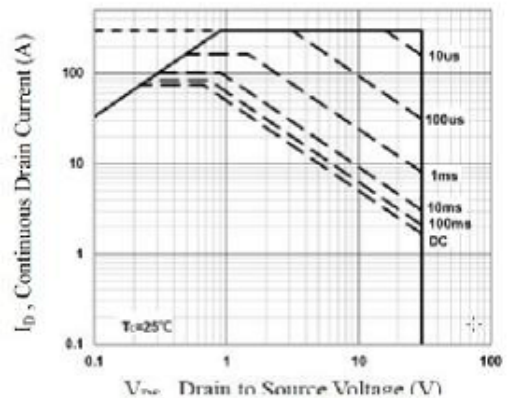
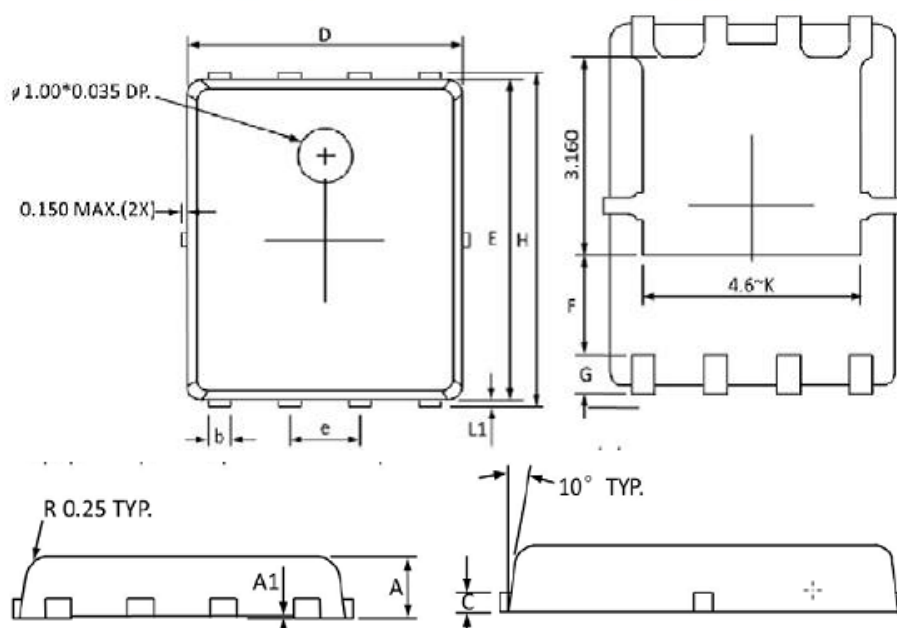


Figure 6: Maximum Safe Operation Area

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Package Outline Dimension

DFN5 × 6



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.000	0.032	0.039
A1	0.000	0.005	0.000	0.000
b	0.350	0.490	0.014	0.019
C	0.254 Ref		0.254 Ref	
D	4.900	5.100	0.193	0.200
E	5.700	5.900	0.225	0.232
e	1.27 BSC		1.27 BSC	
F	1.600 Ref		1.600 Ref	
G	0.600 Ref		0.600 Ref	
H	5.950	6.200	0.235	0.244
L1	0.100	0.180	0.004	0.007
K	3.200 Ref		3.200 Ref	

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SHANGHAI SINO-IC MICROELECTRONICS CO., LTD

Add: Building 3, Room 3401-03, No.200 Zhangheng Road,
ZhangJiang Hi-Tech Park, Pudong, Shanghai 201203, China

Phone: +86-21-33932402 33932403

33932405 33933508 33933608

Fax: +86-21-33932401

Email: webmaster@sino-ic.com

Website: <http://www.sino-ic.com>