

TL284x, TL384x CURRENT-MODE PWM CONTROLLERS

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- Optimized for Off-Line and dc-to-dc Converters
- Low Start-Up Current (<1 mA)
- Automatic Feed-Forward Compensation
- Pulse-by-Pulse Current Limiting
- Enhanced Load-Response Characteristics
- Undervoltage Lockout With Hysteresis
- Double-Pulse Suppression
- High-Current Totem-Pole Output
- Internally Trimmed Bandgap Reference
- 500-kHz Operation
- Error Amplifier With Low Output Resistance
- Designed to Be Interchangeable With UC2842 and UC3842 Series

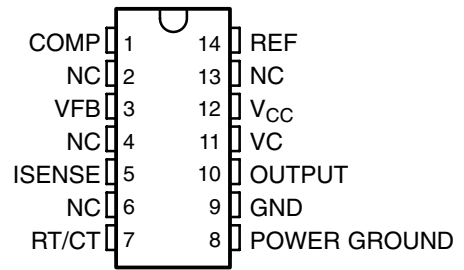
description/ordering information

The TL284x and TL384x series of control integrated circuits provide the features that are necessary to implement off-line or dc-to-dc fixed-frequency current-mode control schemes, with a minimum number of external components. Some of the internally implemented circuits are an undervoltage lockout (UVLO), featuring a start-up current of less than 1 mA, and a precision reference trimmed for accuracy at the error amplifier input. Other internal circuits include logic to ensure latched operation, a pulse-width modulation (PWM) comparator (that also provides current-limit control), and a totem-pole output stage designed to source or sink high-peak current. The output stage, suitable for driving N-channel MOSFETs, is low when it is in the off state.

Major differences between members of these series are the UVLO thresholds and maximum duty-cycle ranges. Typical UVLO thresholds of 16 V (on) and 10 V (off) on the TLx842 and TLx844 devices make them ideally suited to off-line applications. The corresponding typical thresholds for the TLx843 and TLx845 devices are 8.4 V (on) and 7.6 V (off). The TLx842 and TLx843 devices can operate to duty cycles approaching 100%. A duty-cycle range of 0 to 50% is obtained by the TLx844 and TLx845 by the addition of an internal toggle flip-flop, which blanks the output off every other clock cycle.

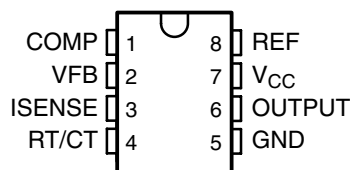
The TL284x-series devices are characterized for operation from -40°C to 85°C . The TL384x devices are characterized for operation from 0°C to 70°C .

**D PACKAGE
(TOP VIEW)**



NC – No internal connection

**D-8 OR P PACKAGE
(TOP VIEW)**



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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ORDERING INFORMATION†

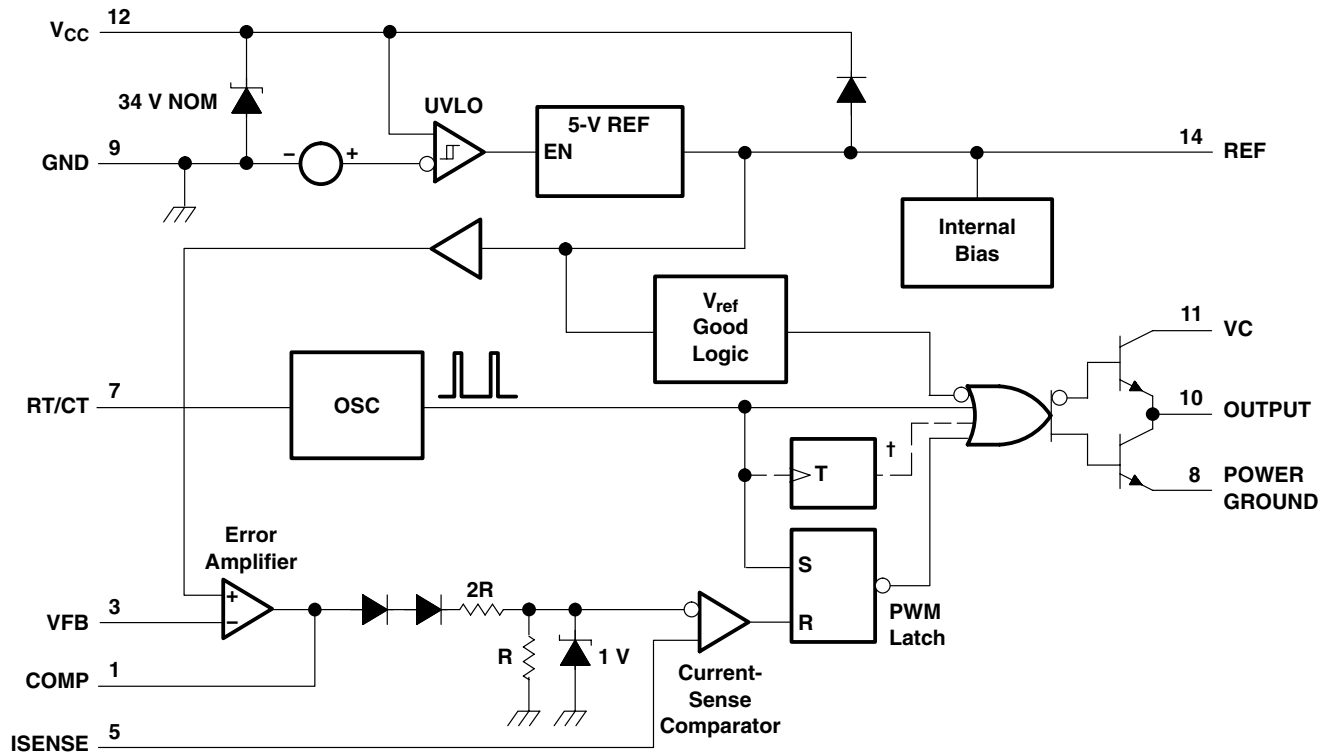
| T _A | PACKAGE‡ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|----------------------|--------------|-----------------------|------------------|
| 0°C to 70°C | PDIP (P) (8 pin) | Tube of 50 | TL3842P | TL3842P |
| | | | TL3843P | TL3843P |
| | | | TL3844P | TL3844P |
| | | | TL3845P | TL3845P |
| | SOIC (D) (8 pin) | Tube of 75 | TL3842D-8 | TL3842 |
| | | | TL3842DR-8 | |
| | | Reel of 2500 | TL3843D-8 | TL3843 |
| | | | TL3843DR-8 | |
| | | Tube of 75 | TL3844D-8 | TL3844 |
| | | | TL3844DR-8 | |
| | | Reel of 2500 | TL3845D-8 | TL3845 |
| | | | TL3845DR-8 | |
| | SOIC (D) (14 pin) | Tube of 50 | TL3842D | TL3842 |
| | | | TL3842DR | |
| | | Reel of 2500 | TL3843D | TL3843 |
| | | | TL3843DR | |
| | | Tube of 50 | TL3844D | TL3844 |
| | | | TL3844DR | |
| Reel of 2500 | | TL3845D | TL3845 | |
| | | TL3845DR | | |
| -40°C to 85°C | PDIP (P) (8 pin) | Tube of 50 | TL2842P | TL2842P |
| | | | TL2843P | TL2843P |
| | | | TL2844P | TL2844P |
| | | | TL2845P | TL2845P |
| | SOIC (D) (8 pin) | Tube of 75 | TL2842D-8 | TL2842 |
| | | | TL2842DR-8 | |
| | | Reel of 2500 | TL2843D-8 | TL2843 |
| | | | TL2843DR-8 | |
| | | Tube of 75 | TL2844D-8 | TL2844 |
| | | | TL2844DR-8 | |
| | | Reel of 2500 | TL2845D-8 | TL2845 |
| | | | TL2845DR-8 | |
| | SOIC (D) (14 pin) | Tube of 50 | TL2842D | TL2842 |
| | | | TL2842DR | |
| | | Reel of 2500 | TL2843D | TL2843 |
| | | | TL2843DR | |
| | | Tube of 50 | TL2844D | TL2844 |
| | | | TL2844DR | |
| | | Reel of 2500 | TL2845D | TL2845 |
| | | | TL2845DR | |

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at <http://www.ti.com>.

‡ Package drawings, thermal data, and symbolization are available at <http://www.ti.com/packaging>.



functional block diagram



† The toggle flip-flop is present only in TL2844, TL2845, TL3844, and TL3845.
Pin numbers shown are for the D (14-pin) package.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

| | |
|---|-----------------|
| Supply voltage (see Note 1) ($I_{CC} < 30$ mA) | Self limiting |
| Analog input voltage range, V_I (VFB and ISENSE) | -0.3 V to 6.3 V |
| Output voltage, V_O (OUTPUT) | 35 V |
| Input voltage, V_I , (VC, D package only) | 35 V |
| Supply current, I_{CC} | 30 mA |
| Output current, I_O | ± 1 A |
| Error amplifier output sink current | 10 mA |
| Package thermal impedance, θ_{JA} (see Notes 2 and 3): | |
| D package | 86°C/W |
| D-8 package | 97°C/W |
| P package | 85°C/W |
| Virtual junction temperature, T_J | 150°C |
| Output energy (capacitive load) | 5 μ J |
| Lead temperature, 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |
| Storage temperature range, T_{stg} | -65°C to 150°C |

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
- All voltages are with respect to the device GND terminal.
 - Maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
 - The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|-----------------------------------|------------------------------------|--------|-----|-----|------|
| V_{CC} and VC [‡] | Supply voltage | | | 30 | V |
| V_I , RT/CT | Input voltage | 0 | | 5.5 | V |
| V_I , VFB and ISENSE | Input voltage | 0 | | 5.5 | V |
| V_O , OUTPUT | Output voltage | | | 30 | V |
| V_O , POWER GROUND [‡] | Output voltage | -0.1 | | 1 | V |
| I_{CC} | Supply current, externally limited | | | 25 | mA |
| I_O | Average output current | | | 200 | mA |
| $I_{O(ref)}$ | Reference output current | | | -20 | mA |
| f_{osc} | Oscillator frequency | | 100 | 500 | kHz |
| T_A | Operating free-air temperature | TL284x | -40 | 85 | °C |
| | | TL384x | 0 | 70 | |

[‡] These recommended voltages for VC and POWER GROUND apply only to the D package.



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electrical characteristics over recommended operating free-air temperature range, $V_{CC} = 15\text{ V}$ (see Note 4), $R_T = 10\text{ k}\Omega$, $C_T = 3.3\text{ nF}$ (unless otherwise specified)

reference section

| PARAMETER | TEST CONDITIONS | TL284x | | | TL384x | | | UNIT |
|---|---|--------|------|------|--------|------|------|---------------|
| | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| Output voltage | $I_O = 1\text{ mA}$, $T_A = 25^\circ\text{C}$ | 4.95 | 5 | 5.05 | 4.9 | 5 | 5.1 | V |
| Line regulation | $V_{CC} = 12\text{ V to }25\text{ V}$ | | 6 | 20 | | 6 | 20 | mV |
| Load regulation | $I_O = 1\text{ mA to }20\text{ mA}$ | | 6 | 25 | | 6 | 25 | mV |
| Temperature coefficient of output voltage | | | 0.2 | 0.4 | | 0.2 | 0.4 | mV/°C |
| Output voltage with worst-case variation | $V_{CC} = 12\text{ V to }25\text{ V}$, $I_O = 1\text{ mA to }20\text{ mA}$ | 4.9 | | 5.1 | 4.82 | | 5.18 | V |
| Output noise voltage | $f = 10\text{ Hz to }10\text{ kHz}$, $T_A = 25^\circ\text{C}$ | | 50 | | | 50 | | μV |
| Output-voltage long-term drift | After 1000 h at $T_A = 25^\circ\text{C}$ | | 5 | 25 | | 5 | 25 | mV |
| Short-circuit output current | | -30 | -100 | -180 | -30 | -100 | -180 | mA |

† All typical values are at $T_A = 25^\circ\text{C}$.

NOTE 4: Adjust V_{CC} above the start threshold before setting it to 15 V.

oscillator section

| PARAMETER | TEST CONDITIONS | TL284x | | | TL384x | | | UNIT |
|--------------------------------------|---------------------------------------|--------|------|-----|--------|------|-----|--------|
| | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| Oscillator frequency (see Note 5) | $T_A = 25^\circ\text{C}$ | 47 | 52 | 57 | 47 | 52 | 57 | kHz |
| Frequency change with supply voltage | $V_{CC} = 12\text{ V to }25\text{ V}$ | | 2 | 10 | | 2 | 10 | Hz/kHz |
| Frequency change with temperature | | | 50 | | | 50 | | Hz/kHz |
| Peak-to-peak amplitude at RT/CT | | | 1.7 | | | 1.7 | | V |

† All typical values are at $T_A = 25^\circ\text{C}$.

NOTES: 4. Adjust V_{CC} above the start threshold before setting it to 15 V.

5. Output frequency equals oscillator frequency for the TLx842 and TLx843. Output frequency is one-half the oscillator frequency for the TLx844 and TLx845.

error-amplifier section

| PARAMETER | TEST CONDITIONS | TL284x | | | TL384x | | | UNIT |
|---------------------------------|--|--------|------|------|--------|------|------|---------------|
| | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| Feedback input voltage | COMP at 2.5 V | 2.45 | 2.50 | 2.55 | 2.42 | 2.50 | 2.58 | V |
| Input bias current | | | -0.3 | -1 | | -0.3 | -2 | μA |
| Open-loop voltage amplification | $V_O = 2\text{ V to }4\text{ V}$ | 65 | 90 | | 65 | 90 | | dB |
| Gain-bandwidth product | | 0.7 | 1 | | 0.7 | 1 | | MHz |
| Supply-voltage rejection ratio | $V_{CC} = 12\text{ V to }25\text{ V}$ | 60 | 70 | | 60 | 70 | | dB |
| Output sink current | VFB at 2.7 V, COMP at 1.1 V | 2 | 6 | | 2 | 6 | | mA |
| Output source current | VFB at 2.3 V, COMP at 5 V | -0.5 | -0.8 | | -0.5 | -0.8 | | mA |
| High-level output voltage | VFB at 2.3 V, $R_L = 15\text{ k}\Omega$ to GND | 5 | 6 | | 5 | 6 | | V |
| Low-level output voltage | VFB at 2.7 V, $R_L = 15\text{ k}\Omega$ to GND | | 0.7 | 1.1 | | 0.7 | 1.1 | V |

† All typical values are at $T_A = 25^\circ\text{C}$.

NOTE 4: Adjust V_{CC} above the start threshold before setting it to 15 V.



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electrical characteristics over recommended operating free-air temperature range, $V_{CC} = 15\text{ V}$ (see Note 4), $R_T = 10\text{ k}\Omega$, $C_T = 3.3\text{ nF}$ (unless otherwise specified) (continued)

current-sense section

| PARAMETER | TEST CONDITIONS | TL284x | | | TL384x | | | UNIT |
|------------------------------------|--|---------|------|------|---------|------|------|---------------|
| | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| Voltage amplification | See Notes 6 and 7 | 2.85 | 3 | 3.13 | 2.85 | 3 | 3.15 | V/V |
| Current-sense comparator threshold | COMP at 5 V, See Note 6 | 0.9 | 1 | 1.1 | 0.9 | 1 | 1.1 | V |
| Supply-voltage rejection ratio | $V_{CC} = 12\text{ V}$ to 25 V , See Note 6 | 70 | | | 70 | | | dB |
| Input bias current | | -2 -10 | | | -2 -10 | | | μA |
| Delay time to output | | 150 300 | | | 150 300 | | | ns |

† All typical values are at $T_A = 25^\circ\text{C}$.

NOTES: 4. Adjust V_{CC} above the start threshold before setting it to 15 V.

6. These parameters are measured at the trip point of the latch, with VFB at 0 V.

7. Voltage amplification is measured between ISENSE and COMP, with the input changing from 0 V to 0.8 V.

output section

| PARAMETER | TEST CONDITIONS | TL284x | | | TL384x | | | UNIT |
|---------------------------|--|--------|------|-----|--------|------|-----|------|
| | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| High-level output voltage | $I_{OH} = -20\text{ mA}$ | 13 | 13.5 | | 13 | 13.5 | | V |
| | $I_{OH} = -200\text{ mA}$ | 12 | 13.5 | | 12 | 13.5 | | |
| Low-level output voltage | $I_{OL} = 20\text{ mA}$ | | 0.1 | 0.4 | | 0.1 | 0.4 | V |
| | $I_{OL} = 200\text{ mA}$ | | 1.5 | 2.2 | | 1.5 | 2.2 | |
| Rise time | $C_L = 1\text{ nF}$, $T_A = 25^\circ\text{C}$ | | 50 | 150 | | 50 | 150 | ns |
| Fall time | $C_L = 1\text{ nF}$, $T_A = 25^\circ\text{C}$ | | 50 | 150 | | 50 | 150 | ns |

† All typical values are at $T_A = 25^\circ\text{C}$.

NOTE 4: Adjust V_{CC} above the start threshold before setting it to 15 V.

undervoltage-lockout section

| PARAMETER | | TL284x | | | TL384x | | | UNIT |
|---|----------------|--------|------|-----|--------|------|------|------|
| | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| Start threshold voltage | TLx842, TLx844 | 15 | 16 | 17 | 14.5 | 16 | 17.5 | V |
| | TLx843, TLx845 | 7.8 | 8.4 | 9 | 7.8 | 8.4 | 9 | |
| Minimum operating voltage after startup | TLx842, TLx844 | 9 | 10 | 11 | 8.5 | 10 | 11.5 | V |
| | TLx843, TLx845 | 7 | 7.6 | 8.2 | 7 | 7.6 | 8.2 | |

† All typical values are at $T_A = 25^\circ\text{C}$.

NOTE 4: Adjust V_{CC} above the start threshold before setting it to 15 V.

pulse-width-modulator section

| PARAMETER | | TL284x | | | TL384x | | | UNIT |
|--------------------|----------------|--------|------|-----|--------|------|-----|------|
| | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| Maximum duty cycle | TLx842, TLx843 | 95 | 97 | 100 | 95 | 97 | 100 | % |
| | TLx844, TLx845 | 46 | 48 | 50 | 46 | 48 | 50 | |
| Minimum duty cycle | | 0 | | | 0 | | | |

† All typical values are at $T_A = 25^\circ\text{C}$.

NOTE 4: Adjust V_{CC} above the start threshold before setting it to 15 V.



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electrical characteristics over recommended operating free-air temperature range, $V_{CC} = 15\text{ V}$ (see Note 4), $R_T = 10\text{ k}\Omega$, $C_T = 3.3\text{ nF}$ (unless otherwise specified) (continued)

supply voltage

| PARAMETER | TEST CONDITIONS | TL284x | | | TL384x | | | UNIT |
|--------------------------|-------------------------|--------|------|-----|--------|------|-----|------|
| | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| Start-up current | | | 0.5 | 1 | | 0.5 | 1 | mA |
| Operating supply current | VFB and ISENSE at 0 V | | 11 | 17 | | 11 | 17 | mA |
| Limiting voltage | $I_{CC} = 25\text{ mA}$ | | 34 | | | 34 | | V |

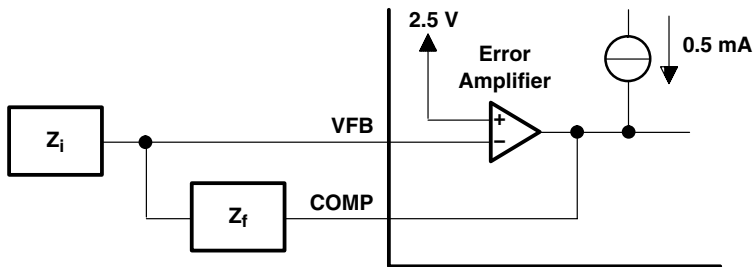
† All typical values are at $T_A = 25^\circ\text{C}$.

NOTE 4: Adjust V_{CC} above the start threshold before setting it to 15 V.

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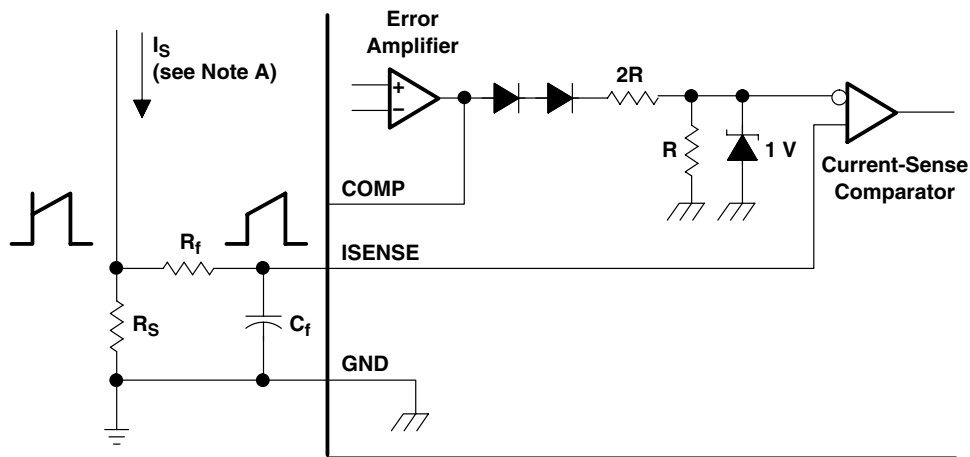
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APPLICATION INFORMATION



NOTE A: Error amplifier can source or sink up to 0.5 mA.

Figure 1. Error-Amplifier Configuration

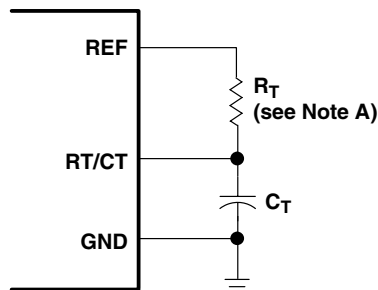


NOTE A: Peak current (I_S) is determined by the formula:

$$I_{S(max)} = \frac{1V}{R_S}$$

A small RC filter formed by resistor R_f and capacitor C_f may be required to suppress switch transients.

Figure 2. Current-Sense Circuit



NOTE A: For $R_T > 5 \text{ k}\Omega$: $f \approx \frac{1.72}{R_T C_T}$

Figure 3. Oscillator Section

APPLICATION INFORMATION

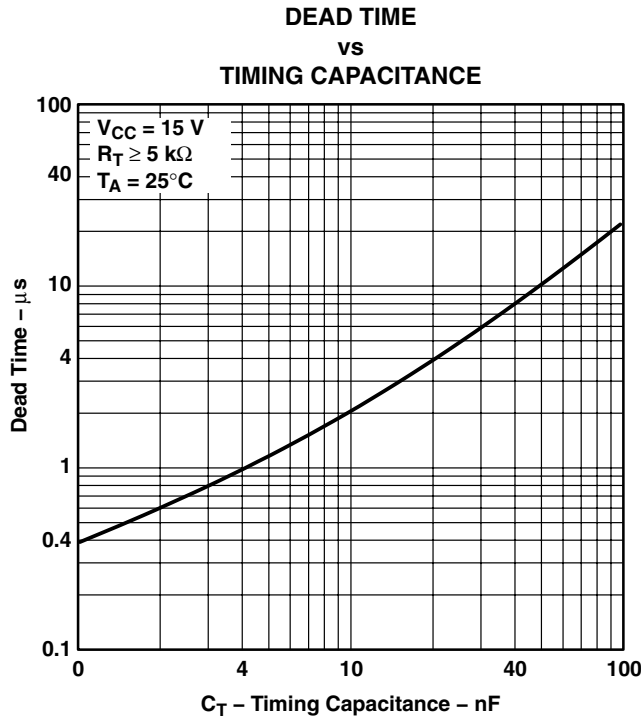


Figure 4

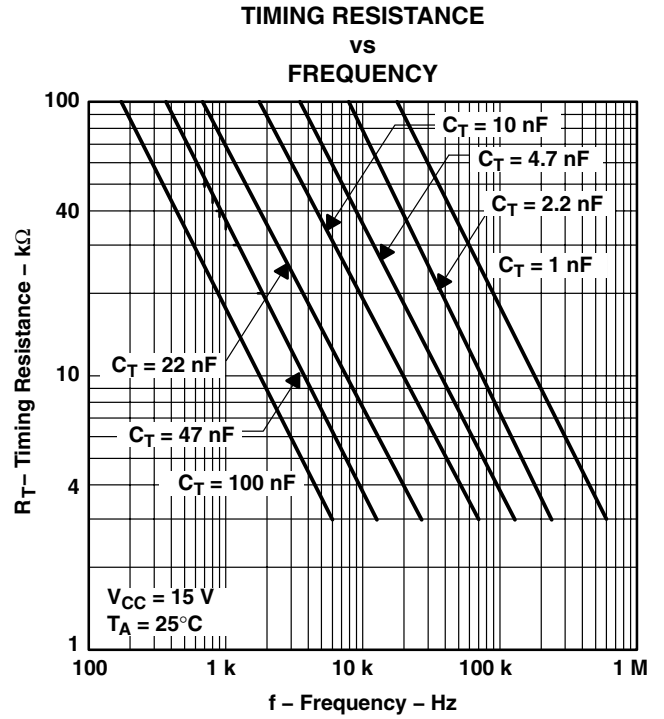


Figure 5

open-loop laboratory test fixture

In the open-loop laboratory test fixture (see Figure 6), high peak currents associated with loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to the GND terminal in a single-point ground. The transistor and 5-k Ω potentiometer sample the oscillator waveform and apply an adjustable ramp to the ISENSE terminal.

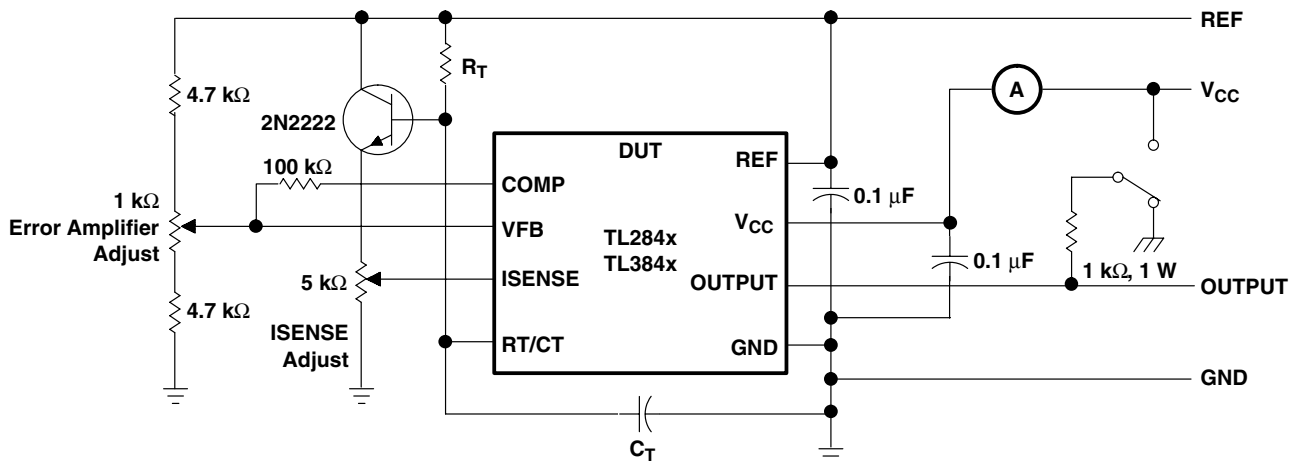


Figure 6. Open-Loop Laboratory Test Fixture

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shutdown technique

The PWM controller (see Figure 7) can be shut down by two methods: either raise the voltage at ISENSE above 1 V or pull the COMP terminal below a voltage two diode drops above ground. Either method causes the output of the PWM comparator to be high (refer to block diagram). The PWM latch is reset dominant so that the output remains low until the next clock cycle after the shutdown condition at the COMP or ISENSE terminal is removed. In one example, an externally latched shutdown can be accomplished by adding an SCR that resets by cycling V_{CC} below the lower UVLO threshold. At this point, the reference turns off, allowing the SCR to reset.

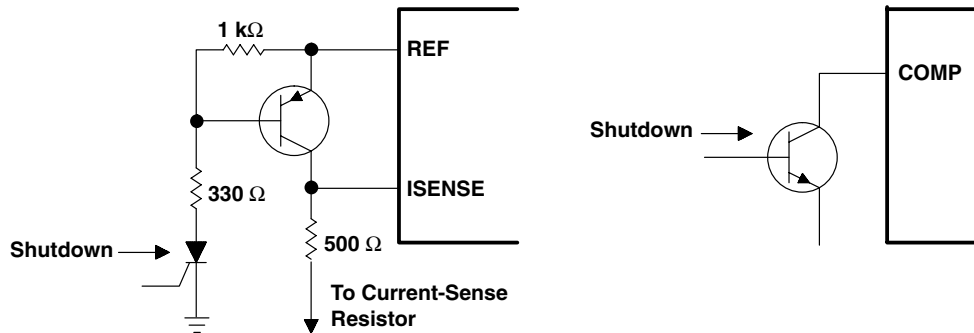


Figure 7. Shutdown Techniques

A fraction of the oscillator ramp can be summed resistively with the current-sense signal to provide slope compensation for converters requiring duty cycles over 50% (see Figure 8). Note that capacitor C forms a filter with R2 to suppress the leading-edge switch spikes.

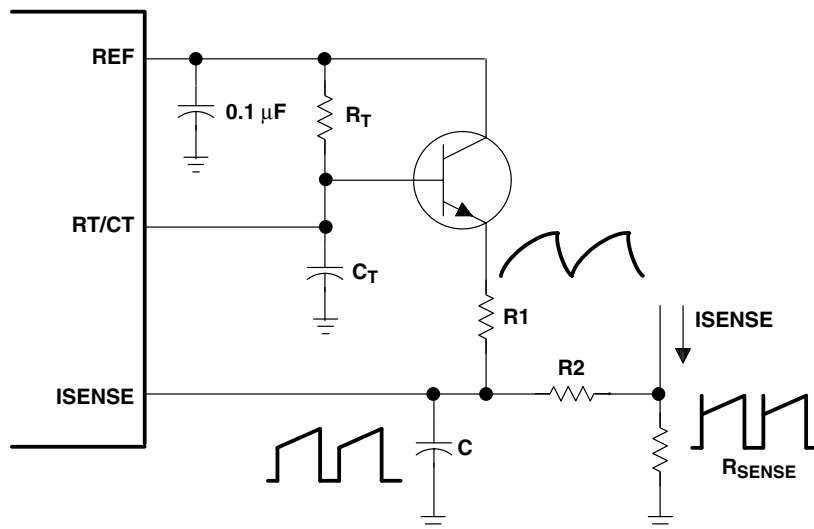


Figure 8. Slope Compensation

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TL2842D | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TL2842 | Samples |
| TL2842D-8 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TL2842 | Samples |
| TL2842DE4-8 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TL2842 | Samples |
| TL2842DR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TL2842 | Samples |
| TL2842DR-8 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TL2842 | Samples |
| TL2842P | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 85 | TL2842P | Samples |
| TL2843D | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL2843 | Samples |
| TL2843D-8 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL2843 | Samples |
| TL2843DG4-8 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL2843 | Samples |
| TL2843DR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL2843 | Samples |
| TL2843DR-8 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL2843 | Samples |
| TL2843DRE4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL2843 | Samples |
| TL2843DRG4-8 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL2843 | Samples |
| TL2843P | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 85 | TL2843P | Samples |
| TL2844D | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL2844 | Samples |
| TL2844D-8 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL2844 | Samples |
| TL2844DR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL2844 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TL2844DR-8 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL2844 | Samples |
| TL2844DRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL2844 | Samples |
| TL2844P | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 85 | TL2844P | Samples |
| TL2844PE4 | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 85 | TL2844P | Samples |
| TL2845D | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL2845 | Samples |
| TL2845D-8 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL2845 | Samples |
| TL2845DG4-8 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL2845 | Samples |
| TL2845DR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL2845 | Samples |
| TL2845DR-8 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL2845 | Samples |
| TL2845DRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL2845 | Samples |
| TL2845P | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 85 | TL2845P | Samples |
| TL2845PE4 | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 85 | TL2845P | Samples |
| TL3842D | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | TL3842 | Samples |
| TL3842D-8 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | TL3842 | Samples |
| TL3842DE4-8 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | TL3842 | Samples |
| TL3842DR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | TL3842 | Samples |
| TL3842DR-8 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | TL3842 | Samples |
| TL3842DRE4-8 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | TL3842 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TL3842P | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | TL3842P | Samples |
| TL3842PE4 | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | TL3842P | Samples |
| TL3843D | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL3843 | Samples |
| TL3843D-8 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL3843 | Samples |
| TL3843DR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL3843 | Samples |
| TL3843DR-8 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL3843 | Samples |
| TL3843DRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL3843 | Samples |
| TL3843DRG4-8 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL3843 | Samples |
| TL3843P | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | TL3843P | Samples |
| TL3843PE4 | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | TL3843P | Samples |
| TL3844D | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL3844 | Samples |
| TL3844D-8 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL3844 | Samples |
| TL3844DG4-8 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL3844 | Samples |
| TL3844DR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL3844 | Samples |
| TL3844DR-8 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL3844 | Samples |
| TL3844P | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | TL3844P | Samples |
| TL3844PE4 | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | TL3844P | Samples |
| TL3845D | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL3845 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TL3845D-8 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL3845 | Samples |
| TL3845DR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL3845 | Samples |
| TL3845DR-8 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL3845 | Samples |
| TL3845DRE4-8 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL3845 | Samples |
| TL3845DRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL3845 | Samples |
| TL3845P | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | TL3845P | Samples |
| TL3845PE4 | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | TL3845P | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

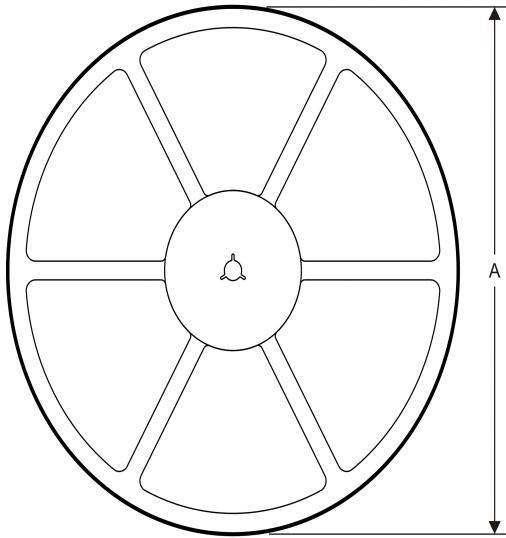
⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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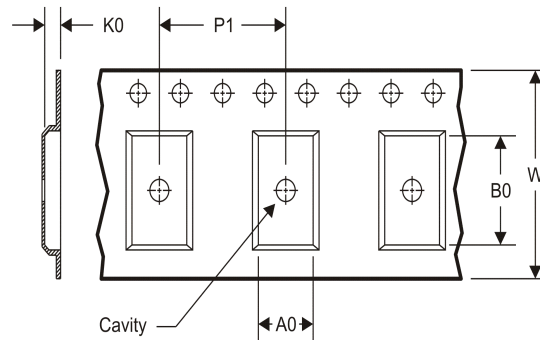
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TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS

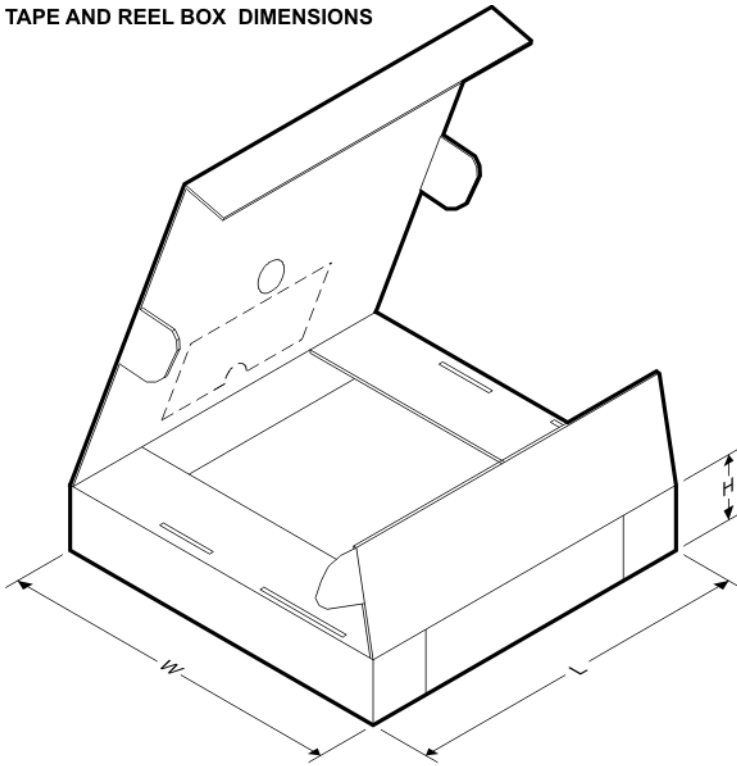


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TL2842DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TL2842DR-8 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TL2843DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TL2843DR-8 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TL2844DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TL2844DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TL2844DR-8 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TL2845DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TL2845DR-8 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TL3842DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TL3842DR-8 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TL3843DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TL3843DR-8 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TL3844DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TL3844DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TL3844DR-8 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TL3845DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TL3845DR-8 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TL2842DR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| TL2842DR-8 | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TL2843DR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| TL2843DR-8 | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TL2844DR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| TL2844DR | SOIC | D | 14 | 2500 | 333.2 | 345.9 | 28.6 |
| TL2844DR-8 | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TL2845DR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| TL2845DR-8 | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TL3842DR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| TL3842DR-8 | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TL3843DR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| TL3843DR-8 | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TL3844DR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| TL3844DR | SOIC | D | 14 | 2500 | 333.2 | 345.9 | 28.6 |
| TL3844DR-8 | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TL3845DR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| TL3845DR-8 | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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