

NC-Cap/PSR-II™ (Primary Side Regulation) CV/CC Controller

FEATURES

- ◆ Proprietary NC-Cap/PSR-II™ Control:
 - $\pm 4\%$ CC and CV Precision
 - Proprietary “Audio Noise Cancellation” Control
 - Built-in “Fast Dynamic Response” Control to Meet USB Charge Requirements
 - Proprietary “Zero-Output Startup” Control
 - Proprietary “Smart Output Short Protection”
 - Without External Compensation/Filtering Capacitor Needed
 - Max. 50V Output for AC/DC LED Lighting
- ◆ Proprietary Cable Drop Compensation
- ◆ Multi Mode Control
- ◆ Low Standby Power Under 70mW
- ◆ Wide VDD Operating Range
- ◆ Cycle-by-Cycle Current Limiting
- ◆ Leading Edge Blanking (LEB)
- ◆ Built-in Soft Start
- ◆ Pin Floating Protection
- ◆ VDD Under Voltage Lockout (UVLO)
- ◆ VDD OVP & Clamp

APPLICATIONS

- ◆ Battery chargers for cellular phones, cordless phones, PDA, digital cameras, etc
- ◆ Replaces linear transformer and RCC SMPS
- ◆ AC/DC LED lighting

GENERAL DESCRIPTION

SF5930S is a high performance, highly integrated DCM (Discontinuous Conduction Mode) Primary Side Regulation (PSR) power controller for offline small power converter applications. It can achieve less than $\pm 4\%$ CV/CC precision.

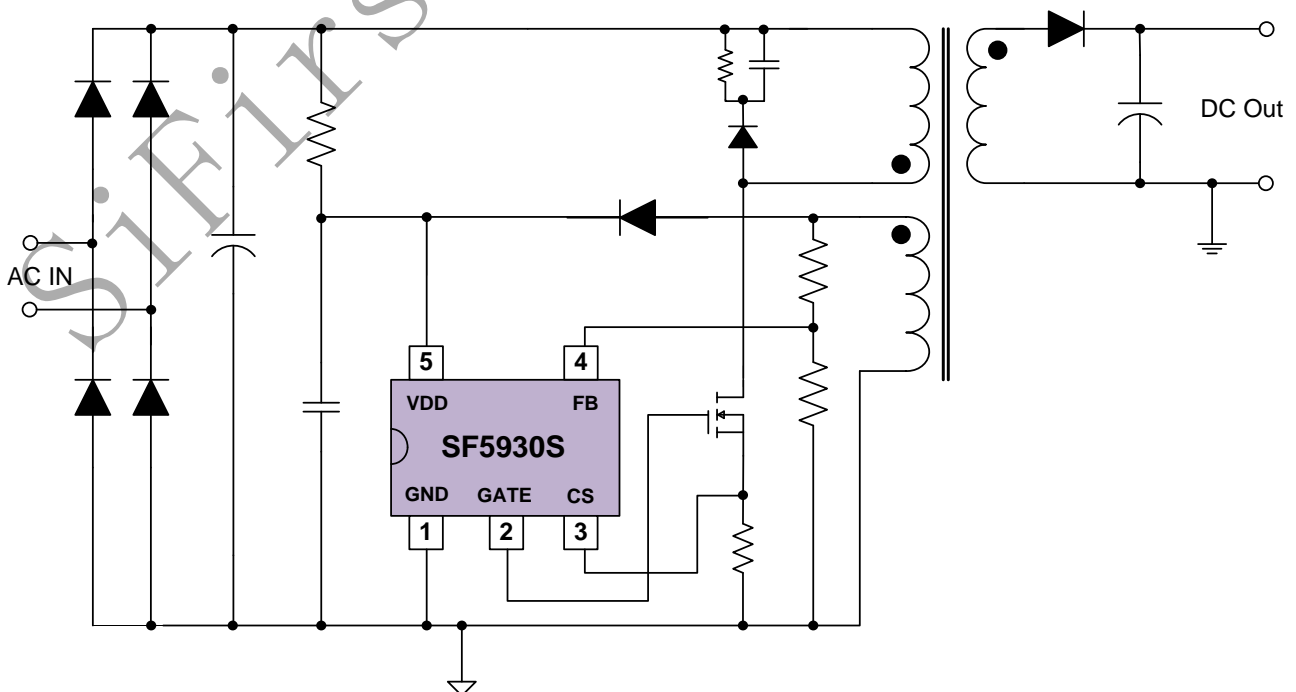
SF5930S has built-in proprietary **NC-Cap/PSR-II™** control for CV control, which eliminates external compensation or filtering capacitor. It has built-in cable drop compensation function, which can provide excellent CV performance. The IC uses Multi Mode Control to improve efficiency and reliability and to decrease audio noise energy @ light loadings. The IC can achieve less than 70mW standby power.

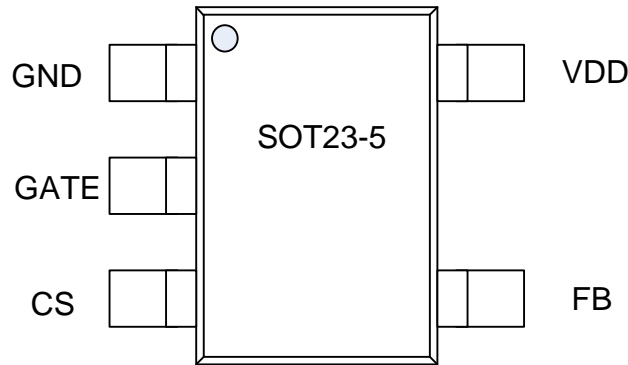
SF5930S integrates proprietary “**Audio Noise Cancellation**” control for audio noise free operation. The IC has built-in “**Fast Dynamic Response**” control to meet USB Charge requirements. SF5930S also integrates proprietary “**Zero-Output Startup**” control to achieve startup when output is near zero voltage. The IC has proprietary “**Smart Output Short Protection**”, which can protect the system with large leakage inductance when output is short circuit.

SF5930S integrates functions and protections of FB Short Protection, Under Voltage Lockout (UVLO), VDD Over Voltage Protection (VDD OVP), Soft Start, Cycle-by-cycle Current Limiting (OCP), Pin Floating Protection, Gate Clamping, VDD Clamping.

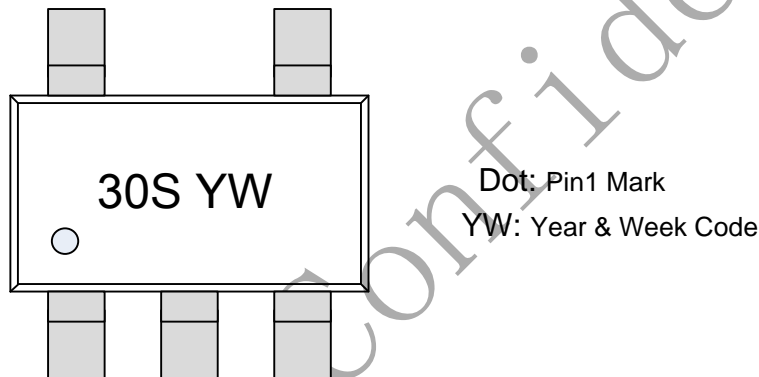
SF5930S is available in SOT23-5 package.

TYPICAL APPLICATION



Pin Configuration

Ordering Information

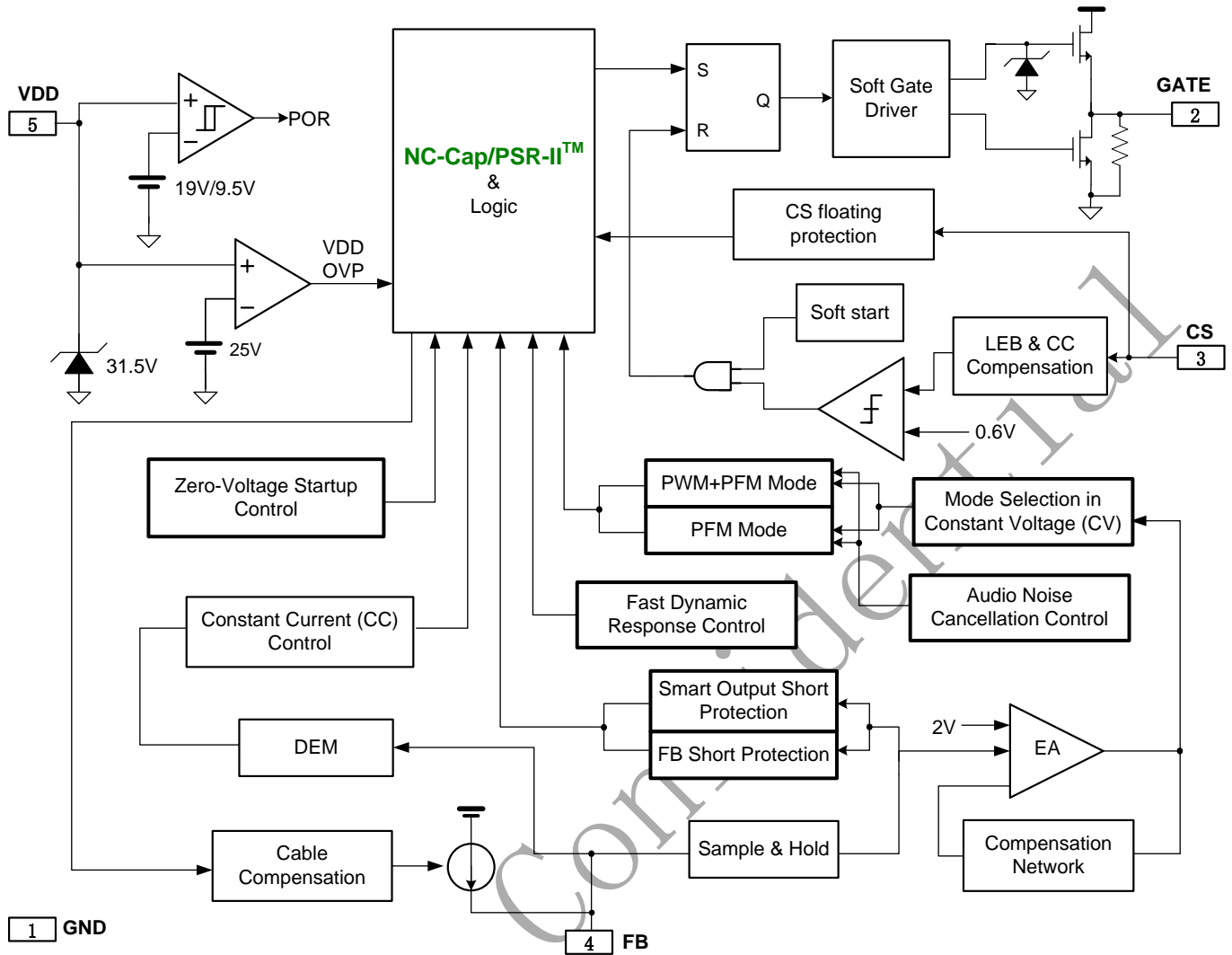
Part Number	Top Mark	Package		Tape & Reel
SF5930SMGT	.30SYW	SOT23-5	Green	Yes

Marking Information

Pin Description

Pin Num	Pin Name	I/O	Description
1	GND	P	Ground
2	GATE	O	Totem-pole gate driver output to drive the external MOSFET.
3	CS	I	Current sense pin.
4	FB	I	System feedback pin. This control input regulates both the output voltage in CV mode and output current in CC mode based on the flyback voltage of the auxiliary winding.
5	VDD	P	IC power supply pin.

Comparison between NC-Cap/PSR-II™ and NC-Cap/PSR™

Function	NC-Cap/PSR-II™	NC-Cap/PSR™
CV/CC Precision	±4%	±5%
Audio Noise Cancellation Control	✓	
Fast Dynamic Response Control	✓	
Zero Output Startup Control	✓	
Smart Output Short Protection	✓	
FB Short Protection	✓	
Maximum Output Voltage	50V	20V

Block Diagram

Absolute Maximum Ratings (Note 1)

Parameter	Value	Unit
VDD DC Supply Voltage	31	V
VDD DC Clamp Current	10	mA
GATE pin	20	V
FB, CS voltage range	-0.3 to 7	V
Package Thermal Resistance (SOT-23-5)	300	°C/W
Maximum Junction Temperature	150	°C
Operating Temperature Range	-40 to 85	°C
Storage Temperature Range	-65 to 150	°C
Lead Temperature (Soldering, 10sec.)	260	°C
ESD Capability, HBM (Human Body Model)	3	kV
ESD Capability, MM (Machine Model)	250	V

Recommended Operation Conditions (Note 2)

Parameter	Value	Unit
Supply Voltage, VDD	11 to 23	V
Operating Ambient Temperature	-40 to 85	°C
Maximum Switching Frequency	70K	Hz

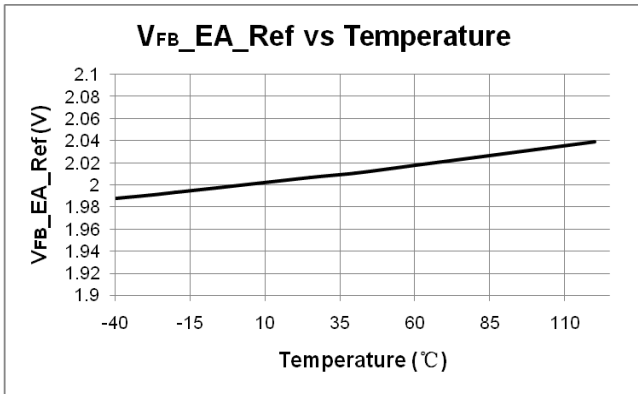
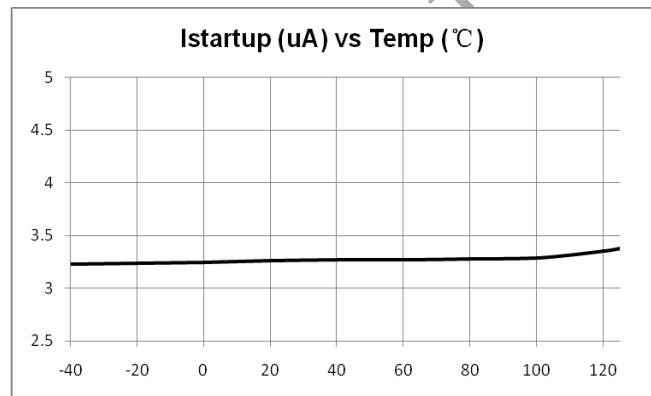
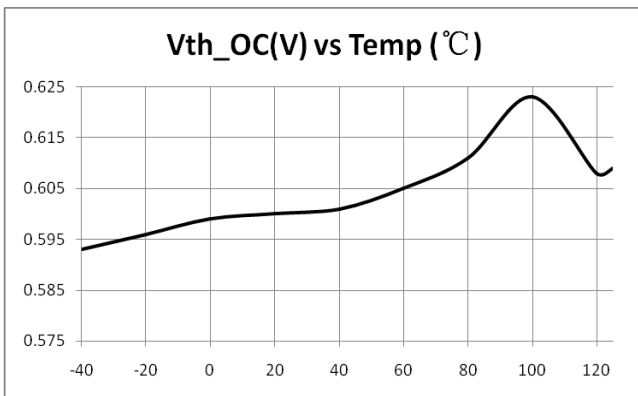
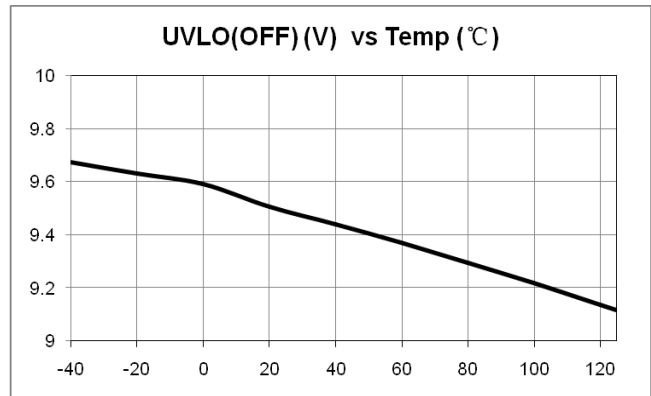
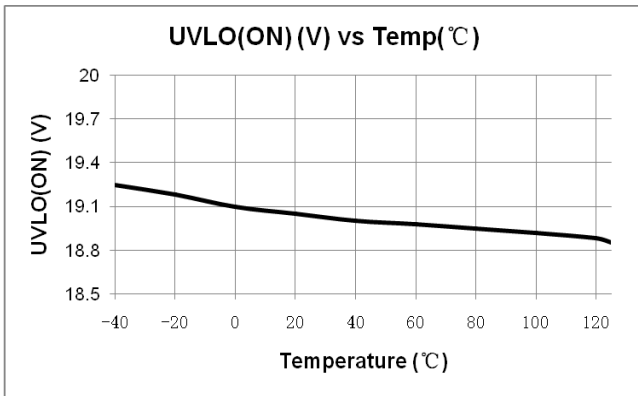
ELECTRICAL CHARACTERISTICS

 (T_A = 25°C, VDD=16V, if not otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Voltage (VDD) Section						
I_Startup	VDD Start up Current	VDD =UVLO(ON)-1V, Measure current into VDD		3	20	uA
I_VDD_Op	Operation Current	VDD=20V		0.8	1.5	mA
UVLO(ON)	VDD Under Voltage Lockout Exit (Startup)		17	19	20	V
UVLO(OFF)	VDD Under Voltage Lockout Enter		8.5	9.5	10.5	V
VDD_OVP	VDD Over Voltage Protection trigger		23	25	27	V
V _{DD} _Clamp	VDD Zener Clamp Voltage	I(V _{DD}) = 10 mA	30	31.5	33	V
T_Softstart	Soft Start Time			2		mSec
Feedback Input Section(FB Pin)						
V _{FB_EA_Ref}	Internal Error Amplifier(EA) reference input		1.97	2.0	2.03	V
V _{FB_DEM}	Demagnetization comparator threshold			25		mV
T _{min_OFF}	Minimum OFF time			2		uSec
T _{max_OFF}	Maximum OFF time			5		mSec
V _{FB_Short}	Output Short Circuit Threshold			0.9		V
T _{FB_Short}	Output Short Circuit Debounce Time			13		mSec
T _{CC} /T _{DEM}	Ratio between switching period in CC mode and demagnetization time			2		
I _{Cable_max}	Max Cable compensation current			50		uA
Current Sense Input Section (CS Pin)						
T _{blanking}	CS Input Leading Edge Blanking Time			500		nSec
V _{th_OC}	Current limiting threshold		588	600	612	mV
T _{D_OC}	Over Current Detection and Control Delay	CL=0.5nF at GATE,		100		nSec
Gate Drive Output						
VOL	Output Low Level	I _o = 20 mA (sink)			1	V
VOH	Output High Level	I _o = 20 mA (source)	7.5			V
V _G _Clamp	Output Clamp Voltage Level	VDD=24V		16		V
T _r	Output Rising Time	CL = 0.5nF		700		nSec
T _f	Output Falling Time	CL =0.5nF		35		nSec

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2. The device is not guaranteed to function outside its operating conditions.

CHARACTERIZATION PLOTS


OPERATION DESCRIPTION

SF5930S is a high performance, highly integrated DCM (Discontinuous Conduction Mode) Primary Side Regulation (PSR) controller. The built-in high precision CV/CC control makes it very suitable for offline small power converter applications.

◆ PSR Technology Introduction

Assuming the system works in DCM mode, the power transfer function is given by

$$P = \frac{\eta}{2} \times L_m \times I_{pk}^2 \times f_s = V_o \times I_o \quad (\text{Eq.1})$$

In the equation above, P is output power, Vo and Io are system output voltage and current respectively, η is system power transfer efficiency, Lm is transformer primary inductance, fs is system switching frequency, Ipk is primary peak current in a switching cycle. The following figure illustrates the waveform in a switching cycle.

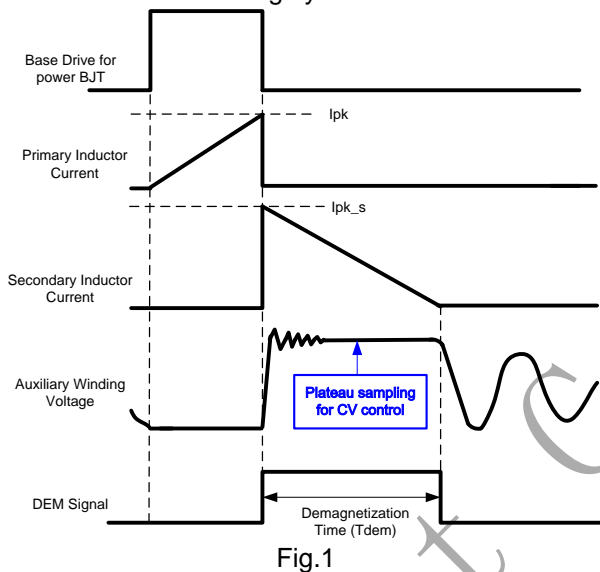


Fig.1

In the figure shown above, the IC generates a demagnetization signal (DEM) in each switching cycle through auxiliary winding. Tdem is demagnetization time for CV/CC control. In DCM mode, Tdem can be expressed as;

$$\frac{V_o}{L_m} \times T_{dem} = \frac{N_s}{N_p} \times I_{pk} \quad (\text{Eq.2})$$

In Eq.2, Np and Ns are primary and secondary winding turns respectively.

Combined with Eq.1 and Eq. 2, the average output current can be expressed as:

$$I_o = \frac{\eta}{2} \times I_{pk} \times \frac{N_p}{N_s} \times f_s \times T_{dem} \quad (\text{Eq.3})$$

CC (Constant Current) Control Scheme

From Eq.3, it can be easily seen that there are two ways to implement CC control: one is PFM (Pulse Frequency Modulation), the control scheme is to keep Ipk to be constant, let the product of Ts and Tdem (fs*Tdem) to be a constant. In this way, Io

will be a value independent to the variation of Vo, Lm, and line input voltage. Another realization method is PWM duty control, the control scheme is to keep fs to be constant, let the product of Tdem and Ipk (Tdem*Ipk) to be a constant, in another words, by modulating system duty cycle to realize a constant Io independent to the variation of Vo, Lm and line voltages.

SF5930S adopts PFM for CC control, the product of Ts and Tdem is given by

$$f_s \times T_{dem} = 0.5 \quad (\text{Eq.4})$$

CV (Constant Voltage) Control Scheme

CV control should sample the plateau of auxiliary winding voltage in flyback phase, as shown in Fig.1 The CV control has many implementations, for example, PWM, or PFM, or a combination of both one. In SF5930S, the CV control adopts proprietary multi mode control, as mention below.

◆ Startup Current / Startup Control / Operating Current

Startup current of SF5930S is designed to be very low (typically 3uA) so that VDD could be charged up above UVLO(ON) threshold level and device starts up quickly. The operating current in SF5930S is as small as 0.5mA (typical). The small operating current results in higher efficiency and reduces the VDD hold-up capacitance requirement.

◆ NC-Cap/PSR-II™ Introduction

● ±4% Precision CV/CC Performance

SF5930S can achieve less than ±4% variation of CC/CV precision due to the built-in CV accuracy improvement and CC line and load compensation, as shown in Fig.2.

● Proprietary “Audio Noise Cancellation” Control

SF5930S has a proprietary “Audio Noise Cancellation” control, which can achieve audio noise free operation in the whole loading range.

● Built-in Fast Dynamic Response Control to Meet USB Charge Requirements

In SF5930S, a fast dynamic response control is integrated to improve system dynamic response performance, thus the charger system can meet the USB charge requirements.

● Smart Output Short Protection

The output short circuit protection of conventional PSR system is based on the coupling between auxiliary winding and secondary winding. When output is short, the auxiliary winding cannot provide enough energy to the IC any more. In this way, the system will enter into auto-recovery mode protection. However, the IC may be wrongly supplied if the leakage inductance of the primary

winding is large enough.

In SF5930S, if output short circuit occurs, the IC will detect the situation and enter into auto-recovery mode protection.

• **Proprietary Zero-Output Startup Control**

Conventional PSR system may suffer startup failure when output voltage is near zero voltage, which means that there is a gap between OCP (CC point in PSR CV/CC system) and full loading. Larger OCP gap causes larger system cost.

In SF5930S, a proprietary “Zero-Output Startup Control” is adopted to achieve successful startup @ $V_{out} \approx 0V$, as shown in Fig.2.

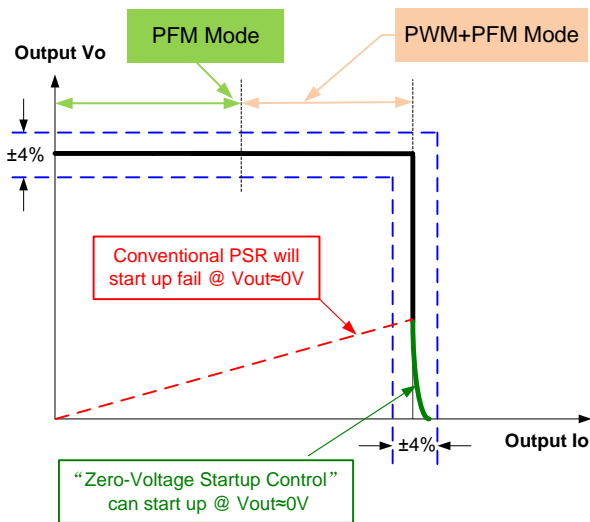


Fig.2

• **No External Compensation/Filtering Capacitor Needed**

SF5930S uses a proprietary control to eliminate external compensation capacitor, which can simplify system design and lower system cost.

• **Maximum 50V Output for LED Lighting**

SF5930S can support maximum 50V output, which can be used in AC/DC LED lighting.

◆ **Proprietary Cable Drop Compensation**

SF5930S has a proprietary built-in cable voltage drop compensation block which can provide a constant output voltage at the end of the cable over the entire load range in CV mode.

◆ **Multi Mode PSR Control for High Reliability , High Efficiency**

Conventional pure PFM controlled PSR system may suffer transformer saturation issue when heavy loading. In SF5930S, a proprietary multi mode control is adopted to suppress this issue, as shown in Fig.2. Around the full load, the system operates in PWM+PFM mode, which improve the system reliability. Under normal to light load

conditions, the IC operates in PFM mode to achieve excellent regulation and high efficiency.

◆ **Soft Start**

SF5930S features an internal 2ms (typical) soft start that slowly increases the threshold of cycle-by-cycle current limiting comparator during startup sequence. Every startup process is followed by a soft start activation.

◆ **Leading Edge Blanking (LEB)**

Each time the power MOSFET is switched on, a turn-on spike occurs across the sensing resistor. To avoid premature termination of the switching pulse, an internal leading edge blanking circuit is built in. During this blanking period (500ns, typical), the cycle-by-cycle current limiting comparator is disabled and cannot switch off the GATE driver.

◆ **Minimum and Maximum OFF Time**

In SF5930S, a minimum OFF time (typically 2us) is implemented to suppress ringing when GATE drive is pull off. The maximum OFF time in SF5930S is typically 5ms, which provides a large range for frequency reduction. In this way, a low standby power of 70mW can be achieved.

◆ **Pin Floating Protection**

In SF5930S, if pin floating situation occurs, the IC is designed to have no damage to system.

◆ **Built-in Load and AC Line CC Compensation**

In conventional PSR system, the output CC (Constant Current) point can vary with output and AC line voltage. In SF5930S the IC has built-in blocks to compensate the variation, as shown in Fig3. The IC can adjust CC point based on sensed output voltage and PFM duty. In this way, CC accuracy can be improved.

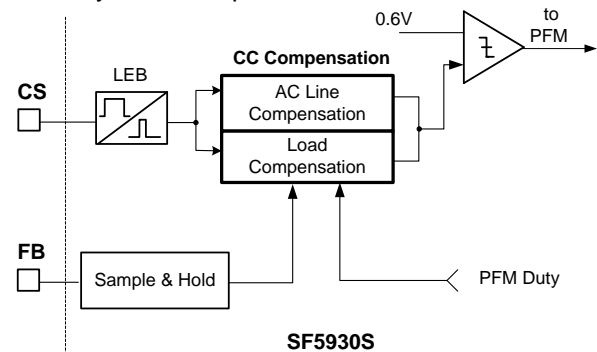


Fig.3

◆ **Auto Recovery Mode Protection**

As shown in Fig.4, once a fault condition is detected, switching will stop. This will cause VDD to fall because no power is delivered from the auxiliary winding. When VDD falls to UVLO(off) (typical 9.5V), the protection is reset and the

operating current reduces to the startup current, which causes VDD to rise, as shown in Fig.4. However, if the fault still exists, the system will experience the above mentioned process. If the fault has gone, the system resumes normal operation. In this manner, the auto restart can alternatively enable and disable the switching until the fault condition is disappeared.

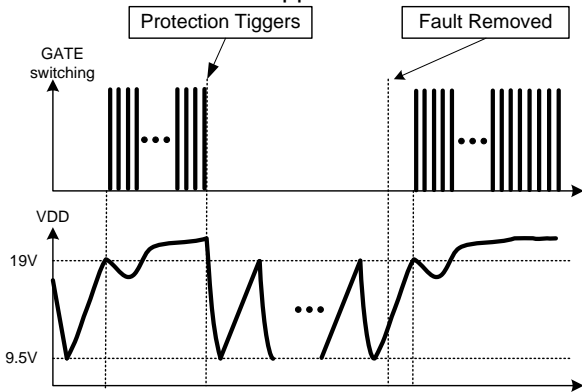


Fig.4

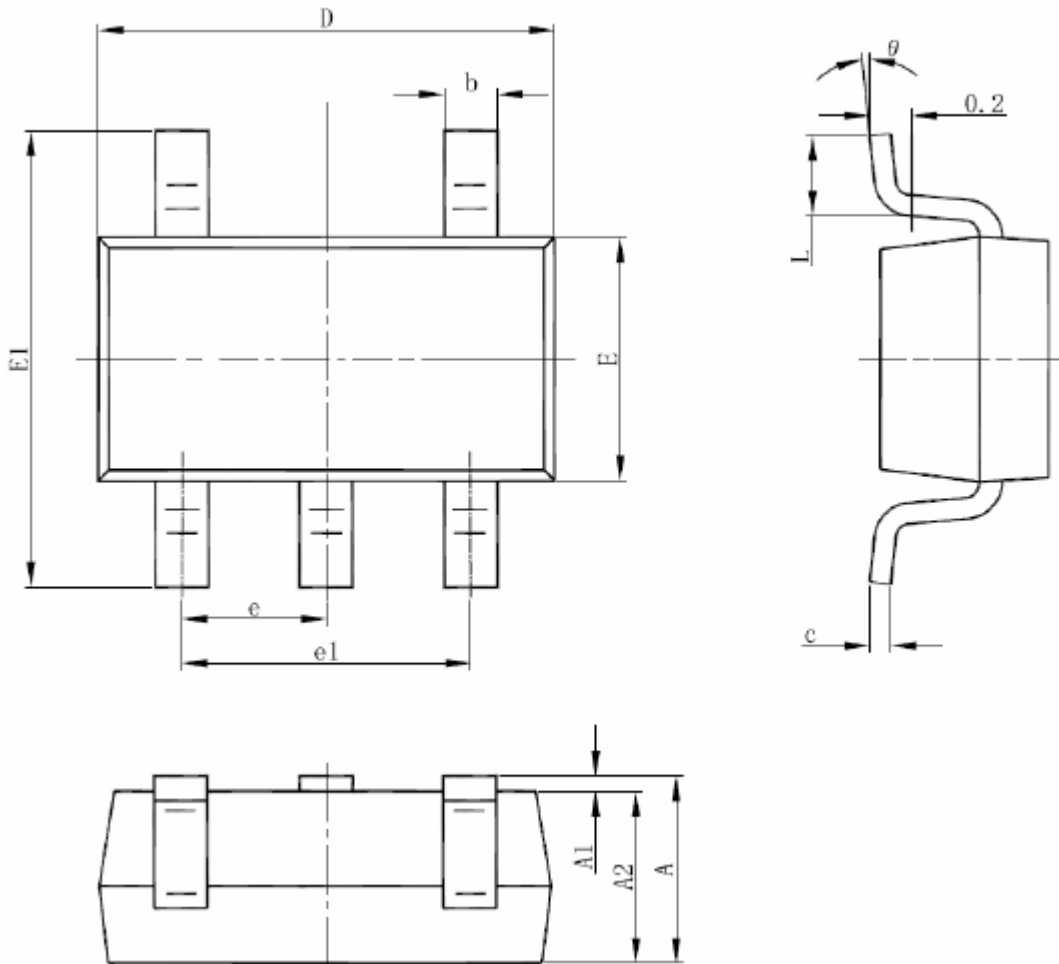
◆ **VDD OVP(Over Voltage Protection)**

VDD OVP is implemented in SF5930S and it is a protection of auto-recovery mode.

◆ **Soft Gate Drive**

SF5930S has a soft totem-pole gate driver with optimized EMI performance. An internal 16V clamp is added for MOSFET gate protection at higher than expected VDD input.

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PACKAGE MECHANICAL DATA
SOT-23-5L PACKAGE OUTLINE DIMENSIONS


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950 (BSC)		0.037 (BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

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