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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

March 2015

FDD8451
N-Channel PowerTrench® MOSFET
40V, 28A, 24mΩ

Features

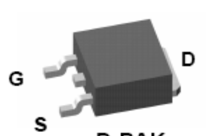
- Max $r_{DS(on)}$ = 24mΩ at V_{GS} = 10V, I_D = 9A
- Max $r_{DS(on)}$ = 30mΩ at V_{GS} = 4.5V, I_D = 7A
- Low gate charge
- Fast Switching
- High performance trench technology for extremely low $r_{DS(on)}$
- RoHS compliant

General Description

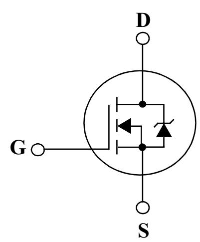
This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, fast switching speed and extremely low $r_{DS(on)}$.

Application

- DC/DC converter
- Backlight inverter



D-PAK
(TO-252)



MOSFET Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	40	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current -Continuous @T_C=25°C	28	A
	-Continuous @T_A=25°C (Note 1a)	9	
	-Pulsed	78	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	20	mJ
P_D	Power Dissipation	30	W
T_J, T_{STG}	Operating and Storage Temperature	-55 to 150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	4.1	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	40	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	96	°C/W

Package Marking and Ordering Information

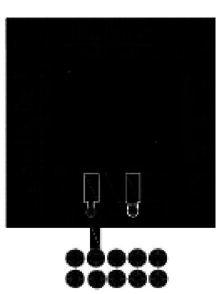
Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD8451	FDD8451	D-PAK(TO-252)	13''	16mm	2500 units

Electrical Characteristics T_J = 25°C unless otherwise noted

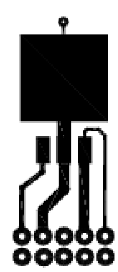
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V	40			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250μA, referenced to 25°C		33.5		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 32V, V_{GS} = 0V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V, V_{DS} = 0V			±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, I_D = 250μA	1	2.1	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250μA, referenced to 25°C		-5.7		mV/°C
$r_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 10V, I_D = 9A		19	24	mΩ
		V_{GS} = 4.5V, I_D = 7A		23	30	
		V_{GS} = 10V, I_D = 9A, T_J = 150°C		32	41	
g_{FS}	Forward Transcondductance	V_{DS} = 5V, I_D = 9A		29		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 20V, V_{GS} = 0V, f = 1MHz		780	990	pF
C_{oss}	Output Capacitance			112	150	pF
C_{rss}	Reverse Transfer Capacitance			72	110	pF
R_g	Gate Resistance	f = 1MHz		1.1		Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 20V, I_D = 9A, V_{GS} = 10V, R_{GEN} = 6Ω		7	14	ns
t_r	Rise Time			3	10	ns
$t_{d(off)}$	Turn-Off Delay Time			19	34	ns
t_f	Fall Time			2	10	ns
Q_g	Total Gate Charge at 10V	V_{DS}= 20V, I_D = 9A, V_{GS} = 10V		16	20	nC
Q_g	Total Gate Charge at 5V			8.6	11	nC
Q_{gs}	Gate to Source Gate Charge			2.5		nC
Q_{gd}	Gate to Drain "Miller"Charge			3.7		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0V, I_S = 9A		0.87	1.2	V
t_{rr}	Reverse Recovery Time	I_F = 9A, di/dt = 100A/μs		25	38	ns
Q_{rr}	Reverse Recovery Charge	I_F = 9A, di/dt = 100A/μs		19	29	nC

Notes:

1: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a) 40 °C/W when mounted on a 1 in^2 pad of 2 oz copper



b) 96 °C/W when mounted on a minimum pad

2: Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

3: Starting T_J = 25 °C, L = 0.1 mH, I_{AS} = 20 A, V_{DD} = 36 V, V_{GS} = 10 V.

Typical Characteristics T_J = 25°C unless otherwise noted

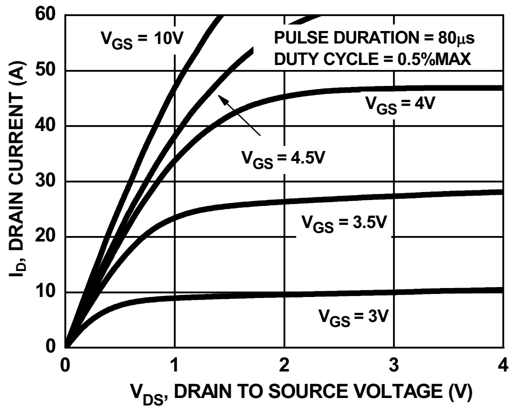


Figure 1. On Region Characteristics

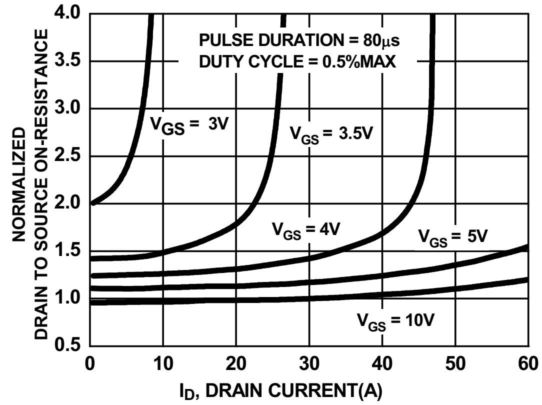


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

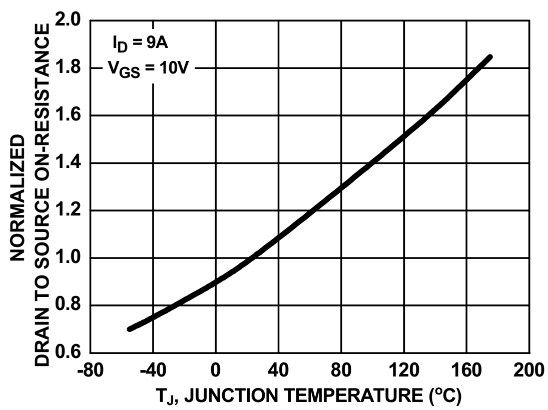


Figure 3. Normalized On Resistance vs Junction Temperature

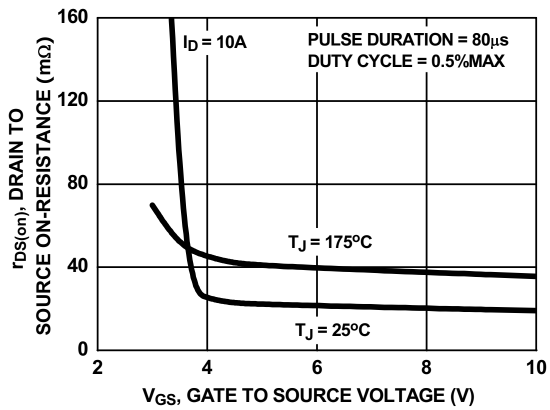


Figure 4. On-Resistance vs Gate to Source Voltage

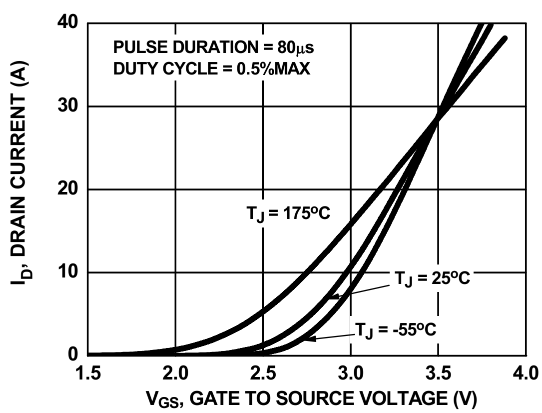


Figure 5. Transfer Characteristics

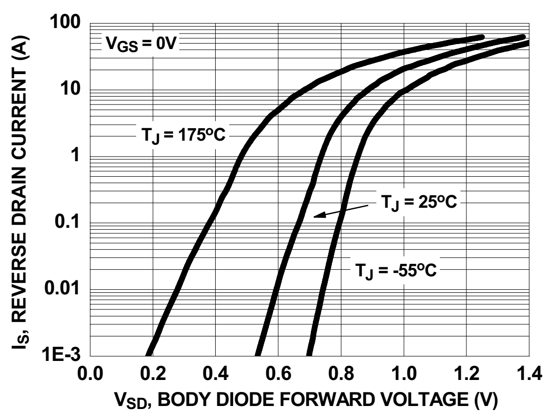


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25°C unless otherwise noted

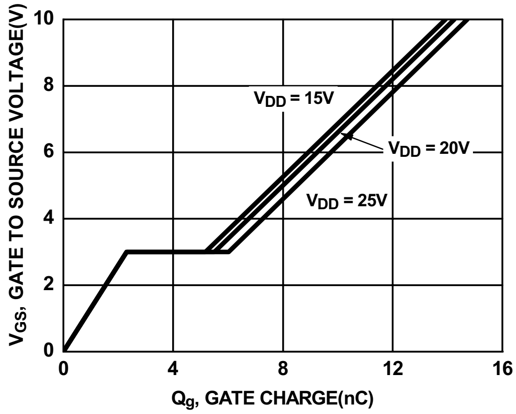


Figure 7. Gate Charge Characteristics

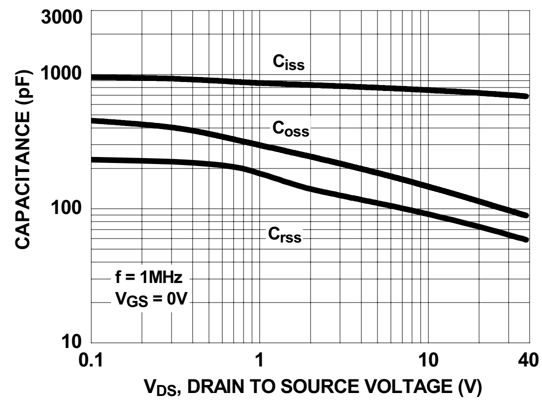


Figure 8. Capacitance vs Drain to Source Voltage

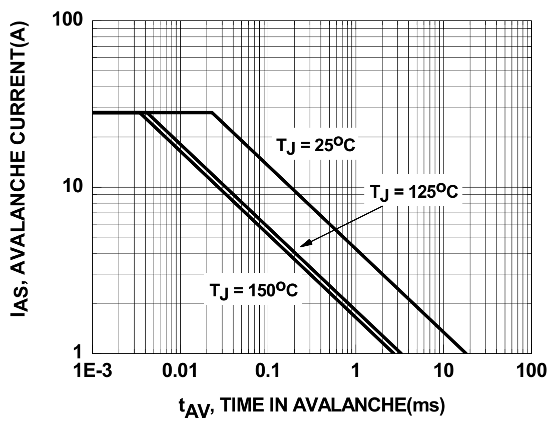


Figure 9. Unclamped Inductive Switching Capability

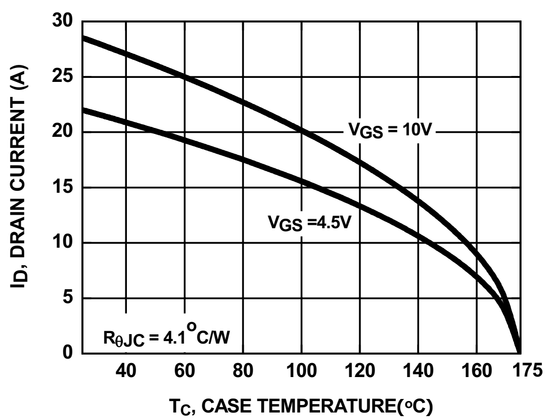


Figure 10. Maximum Continuous Drain Current vs Case Temperature

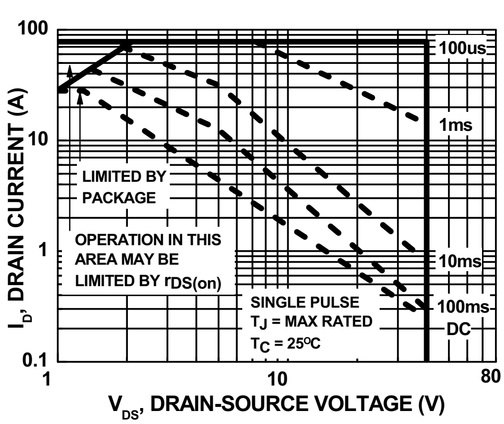
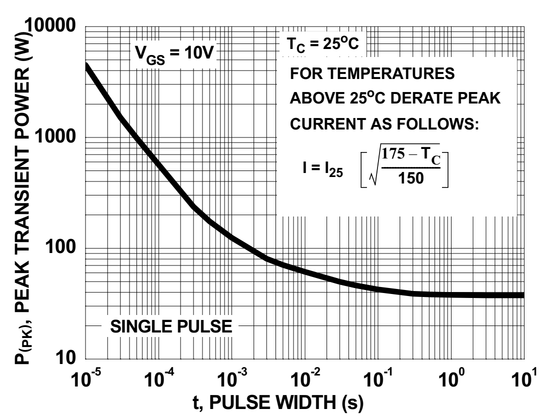


Figure 11. Forward Bias Safe Operating Area



$$I = I_{25}\left[\sqrt{\frac{175 - T_C}{150}}\right]$$

Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25°C unless otherwise noted

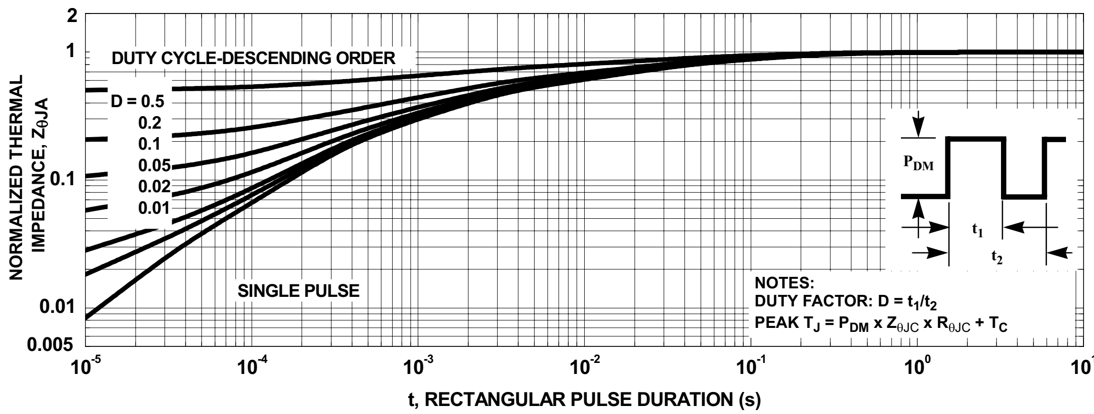
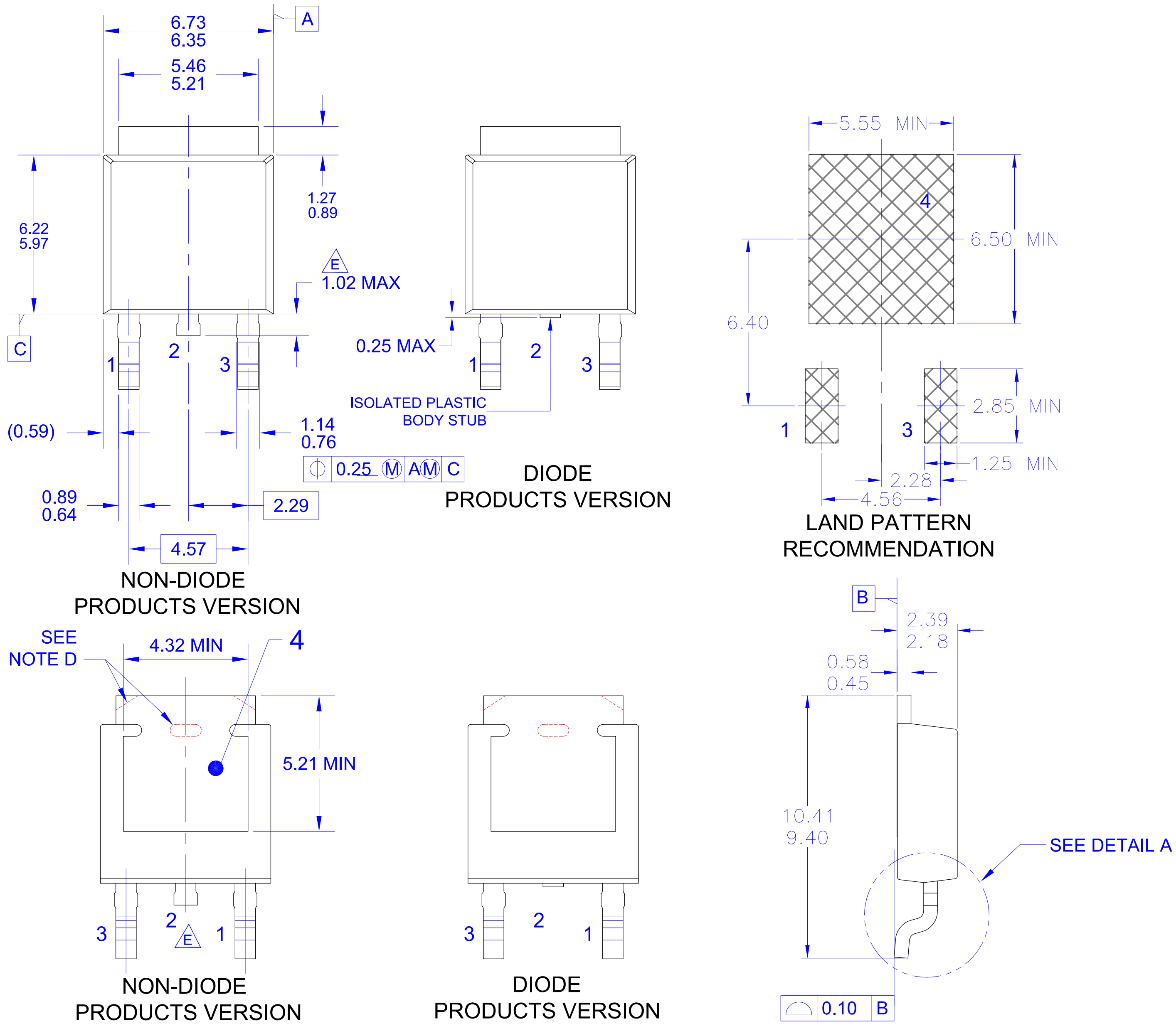


Figure 13. Transient Thermal Response Curve



NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.

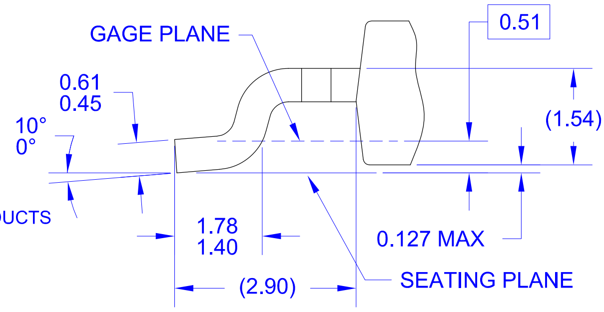
D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.

E) TRIMMED METAL CENTER LEAD IS PRESENT ON FOR NON-DIODE PRODUCTS

F) DIMENSIONS ARE EXCLUSIVE OF BURS, MOLD FLASH AND TIE BAR EXTRUSIONS.

G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.

H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV11



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