High Voltage, High and Low Side Driver

The NCP5109 is a high voltage gate driver IC providing two outputs for direct drive of 2 N-channel power MOSFETs or IGBTs arranged in a half-bridge configuration version B or any other high-side + low-side configuration version A.

It uses the bootstrap technique to ensure a proper drive of the high-side power switch. The driver works with 2 independent inputs.

Features

- High Voltage Range: Up to 200 V
- dV/dt Immunity ±50 V/nsec
- Negative Current Injection Characterized Over the Temperature Range
- Gate Drive Supply Range from 10 V to 20 V
- High and Low Drive Outputs
- Output Source / Sink Current Capability 250 mA / 500 mA
- 3.3 V and 5 V Input Logic Compatible
- Up to V_{CC} Swing on Input Pins
- Extended Allowable Negative Bridge Pin Voltage Swing to −10 V for Signal Propagation
- Matched Propagation Delays Between Both Channels
- Outputs in Phase with the Inputs
- Independent Logic Inputs to Accommodate All Topologies (Version A)
- Cross Conduction Protection with 100 ns Internal Fixed Dead Time (Version B)
- Under V_{CC} LockOut (UVLO) for Both Channels
- Pin-to-Pin Compatible with Industry Standards
- These are Pb-Free Devices

Typical Applications

- Half-Bridge Power Converters
- Any Complementary Drive Converters (Asymmetrical Half–Bridge, Active Clamp) (A Version Only).
- Full-Bridge Converters



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MARKING DIAGRAMS



SOIC-8 D SUFFIX CASE 751





DFN10 MN SUFFIX CASE 506DH



5109 = Specific Device Code

x = A or B version

A = Assembly Location

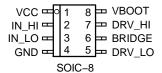
L = Wafer Lot Y = Year

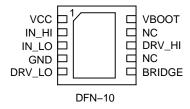
W = Work Week

■ = Pb-Free Package

(Note: Microdot may be in either location)

PINOUT INFORMATION





ORDERING INFORMATION

See detailed ordering and shipping information on page 16 of this data sheet.

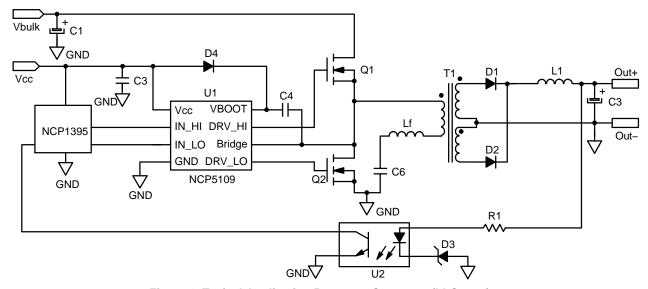


Figure 1. Typical Application Resonant Converter (LLC type)

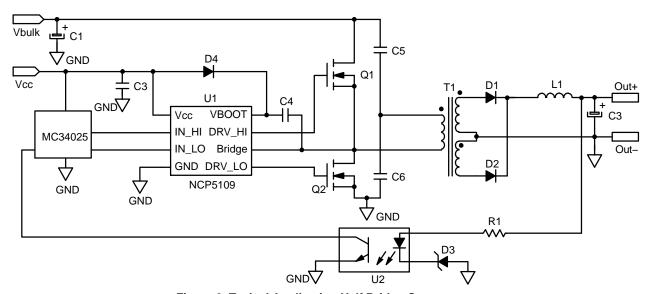


Figure 2. Typical Application Half Bridge Converter

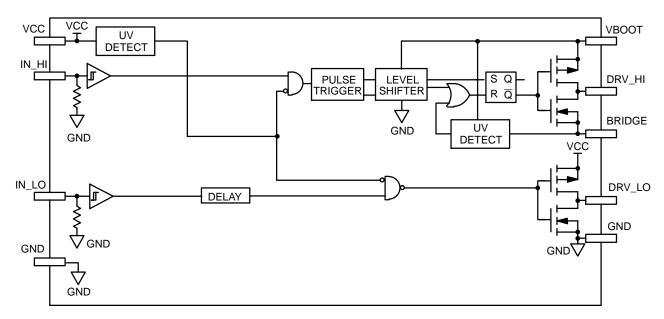


Figure 3. Detailed Block Diagram: Version A

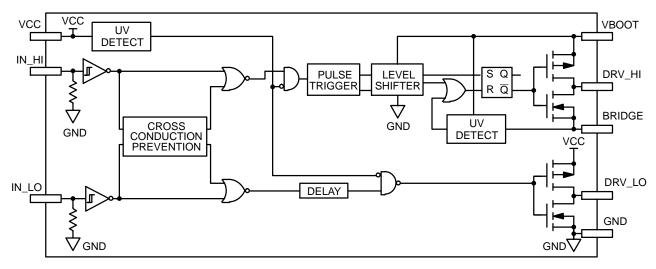


Figure 4. Detailed Block Diagram: Version B

PIN DESCRIPTION

Pin Name	Description	
IN_HI	Logic Input for High Side Driver Output in Phase	
IN_LO	Logic Input for Low Side Driver Output in Phase	
GND	Ground	
DRV_LO	Low Side Gate Drive Output	
V _{CC}	Low Side and Main Power Supply	
V _{BOOT}	Bootstrap Power Supply	
DRV_HI	High Side Gate Drive Output	
BRIDGE	Bootstrap Return or High Side Floating Supply Return	
NC	Removed for creepage distance (DFN package only)	

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
V _{CC}	Main power supply voltage	-0.3 to 20	V
V _{CC_transient}	Main transient power supply voltage: IV _{CC_max} = 5 mA during 10 ms	23	V
V _{BRIDGE}	VHV: High Voltage BRIDGE pin	-1 to 200	V
V _{BRIDGE}	Allowable Negative Bridge Pin Voltage for IN_LO Signal Propagation to DRV_LO (see characterization curves for detailed results)	-10	V
$V_{BOOT-}V_{BRIDGE}$	VHV: Floating supply voltage	-0.3 to 20	V
V_{DRV_HI}	VHV: High side output voltage	$V_{BRIDGE} - 0.3$ to $V_{BOOT} + 0.3$	V
V_{DRV_LO}	Low side output voltage	-0.3 to $V_{CC} + 0.3$	V
dV _{BRIDGE} /dt	Allowable output slew rate	50	V/ns
V _{IN_XX}	Inputs IN_HI, IN_LO	-1.0 to V _{CC} + 0.3	V
	ESD Capability: - HBM model (all pins except pins 6–7–8 in 8 pins package or 11–12–13 in 14 pins package) - Machine model (all pins except pins 6–7–8 in 8 pins package or 11–12–13 in 14 pins package)	2 200	kV V
	Latch up capability per JEDEC JESD78		
R_{\thetaJA}	Power dissipation and Thermal characteristics SO–8: Thermal Resistance, Junction–to–Air DFN10 3x3: Thermal Resistance, Junction–to–Ambient 1 Oz Cu 50 mm ² Printed Circuit Copper Clad	178 172	°C/W
T _{ST}	Storage Temperature Range	-55 to +150	°C
T _{J_max}	Maximum Operating Junction Temperature	+150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ELECTRICAL CHARACTERISTIC ($V_{CC} = V_{boot} = 15 \text{ V}, V_{GND} = V_{bridge}, -40^{\circ}\text{C} < T_{J} < 125^{\circ}\text{C}, \text{ Outputs loaded with 1 nF)}$

PUT SECTION Full high short circuit pulsed current $V_{DRV} = 0 \text{ V}$, $PW \le 10 \text{ µs}$ (Note 1) Full tow short circuit pulsed current $V_{DRV} = V_{CC}$, $PW \le 10 \text{ µs}$ (Note 1) Full tow short circuit pulsed current $V_{DRV} = V_{CC}$, $PW \le 10 \text{ µs}$ (Note 1) Full tresistor (Typical value @ 25°C) Source Full resistor (Typical value @ 25°C) Sink Full level output voltage, $V_{BIAS} = V_{DRV} = V_{CC} =$	RVsource DRVsink ROH ROL DRV_H DRV_L ton toff tr tf	Min 20	100 100 85 30 100 -	Max 60 20 1.6 0.6 170 170 160 75 35 190	mA mA Ω V V ns ns ns ns
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level output voltage V _{DRV_XX} @ I _{DRV_XX} = 20 mA VAIAMIC OUTPUT SECTION -on propagation delay (Vbridge = 0 V) -off propagation delay (Vbridge = 0 V or 50 V) (Note 2) out voltage rise time (from 10% to 90% @ V _{CC} = 15 V) with 1 nF load out voltage fall time (from 90% to 10% @ V _{CC} = 15 V) with 1 nF load agation delay matching between the High side and the Low side @ 25°C (Note 3) onal fixed dead time (only valid for B version) (Note 4) mum input width that changes the output mum input width that does not change the output SOIC-8 DFN10 UT SECTION level input voltage threshold c "1" input bias current @ V _{IN_XX} = 5 V @ 25°C c "0" input bias current @ V _{IN_XX} = 0 V @ 25°C PPLY SECTION UV Start-up voltage threshold UV Shut-down voltage threshold VCC eresis on V _{CC} ot Start-up voltage threshold reference to bridge pin	ton toff tr tf Δt DT tpw1	- - - - - 65	0.2 100 100 85 35 20	0.6 170 170 160 75 35	v ns ns ns ns
AMIC OUTPUT SECTION -on propagation delay (Vbridge = 0 V) -off propagation delay (Vbridge = 0 V or 50 V) (Note 2) tut voltage rise time (from 10% to 90% @ V _{CC} = 15 V) with 1 nF load tut voltage fall time (from 90% to 10% @V _{CC} = 15 V) with 1 nF load agation delay matching between the High side and the Low side @ 25°C (Note 3) and fixed dead time (only valid for B version) (Note 4) mum input width that changes the output mum input width that does not change the output SOIC-8 DFN10 UT SECTION level input voltage threshold c "1" input bias current @ V _{IN_XX} = 5 V @ 25°C c "0" input bias current @ V _{IN_XX} = 0 V @ 25°C CPLY SECTION UV Start-up voltage threshold UV Shut-down voltage threshold VCC eresis on V _{CC} ot Start-up voltage threshold reference to bridge pin	t _{ON} t _{OFF} tr tf Δt DT t _{PW1}	- - - - - 65	100 100 85 35 20	170 170 160 75 35	ns ns ns
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out voltage rise time (from 10% to 90% @ V _{CC} = 15 V) with 1 nF load out voltage fall time (from 90% to 10% @V _{CC} = 15 V) with 1 nF load agation delay matching between the High side and the Low side @ 25°C (Note 3) anal fixed dead time (only valid for B version) (Note 4) anum input width that changes the output anum input width that does not change the output SOIC-8 DFN10 UT SECTION Ievel input voltage threshold at pull-down resistor (V _{IN} < 0.5 V) Ievel input voltage threshold at "1" input bias current @ V _{IN_XX} = 5 V @ 25°C at "0" input bias current @ V _{IN_XX} = 0 V @ 25°C PPLY SECTION UV Start-up voltage threshold UV Shut-down voltage threshold vcc eresis on V _{CC} Vot Start-up voltage threshold reference to bridge pin	tr tf Δt DT tp _{W1}	- - - 65	85 35 20	160 75 35	ns ns
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UT SECTION level input voltage threshold t pull-down resistor ($V_{IN} < 0.5 \text{ V}$) level input voltage threshold c "1" input bias current @ $V_{IN_XX} = 5 \text{ V}$ @ 25°C c "0" input bias current @ $V_{IN_XX} = 0 \text{ V}$ @ 25°C PLY SECTION UV Start-up voltage threshold VCC to Start-up voltage threshold reference to bridge pin	t _{PW2}	20		50	ns
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t pull-down resistor (V _{IN} < 0.5 V) level input voltage threshold c "1" input bias current @ V _{IN_XX} = 5 V @ 25°C c "0" input bias current @ V _{IN_XX} = 0 V @ 25°C PLY SECTION UV Start-up voltage threshold VCC UV Shut-down voltage threshold vcc t Start-up voltage threshold reference to bridge pin					
level input voltage threshold c "1" input bias current @ V _{IN_XX} = 5 V @ 25°C c "0" input bias current @ V _{IN_XX} = 0 V @ 25°C PPLY SECTION UV Start-up voltage threshold VCC UV Shut-down voltage threshold vcc vcc t Start-up voltage threshold reference to bridge pin	V _{IN}	-	-	0.8	V
c "1" input bias current @ $V_{IN_XX} = 5 \text{ V}$ @ 25°C c "0" input bias current @ $V_{IN_XX} = 0 \text{ V}$ @ 25°C PPLY SECTION UV Start-up voltage threshold VCC UV Shut-down voltage threshold vCC eresis on V_{CC} VC t Start-up voltage threshold reference to bridge pin	R _{IN}	-	200	-	kΩ
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PPLY SECTION UV Start-up voltage threshold UV Shut-down voltage threshold vcc eresis on Vcc vt Start-up voltage threshold reference to bridge pin	I _{IN+}	-	5	25	μΑ
UV Start-up voltage threshold UV Shut-down voltage threshold VCC eresis on VCC VC VC VC VC VC VC VC VC VC	I _{IN} _	-	-	2.0	μΑ
UV Shut-down voltage threshold Vcc eresis on Vcc Vc t Start-up voltage threshold reference to bridge pin Vbc					
eresis on V _{CC} ot Start-up voltage threshold reference to bridge pin Vo	_{CC} _stup	8.0	8.9	9.9	V
ot Start-up voltage threshold reference to bridge pin Vbc	_shtdwn	7.3	8.2	9.1	V
. •	CC_hyst	0.3	0.7	_	V
or_arch = Apport = Applicable)	oot_stup	8.0	8.9	9.9	V
ot UV Shut-down voltage threshold Vboo	ot_shtdwn	7.3	8.2	9.1	V
eresis on Vboot Vbc	oot_hyst	0.3	0.7	-	V
age current on high voltage pins to GND I _{HV} DOT = V _{BRIDGE} = DRV_HI = 200 V)	D/ 1 = 4::	-	5	40	μΑ
sumption in active mode (V _{CC} = Vboot, fsw = 100 kHz and 1 nF load on both driver uts)	IV_LEAK	-	4	5	mA
sumption in inhibition mode (V _{CC} = Vboot)	ICC1			400	μΑ
current consumption in inhibition mode		_	250		
ot current consumption in inhibition mode	ICC1	-	250 200	_	μΑ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- Parameter guaranteed by design.

- Turn-off propagation delay @ Vbridge = 200 V is guaranteed by design.
 See characterization curve for Δt parameters variation on the full range temperature.
 Version B integrates a dead time in order to prevent any cross conduction between DRV_HI and DRV_LO. See timing diagram of Figure 10.
- 5. Timing diagram definition see: Figure 7, Figure 8 and Figure 9.

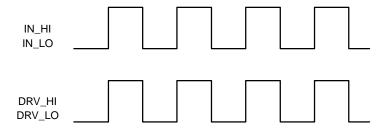


Figure 5. Input/Output Timing Diagram (A Version)

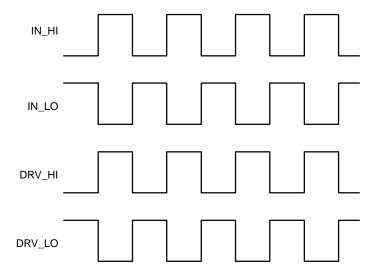


Figure 6. Input/Output Timing Diagram (B Version)

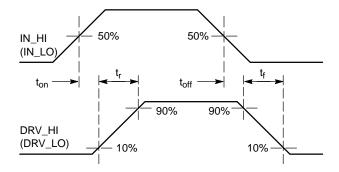


Figure 7. Propagation Delay and Rise / Fall Time Definition

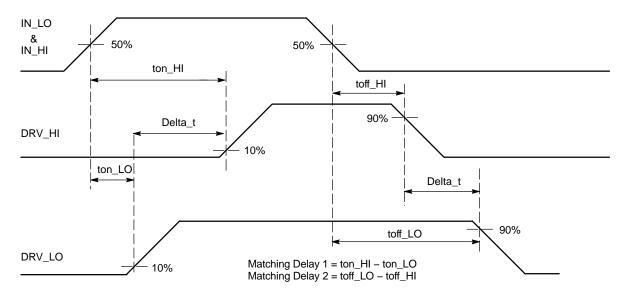


Figure 8. Matching Propagation Delay (A Version)

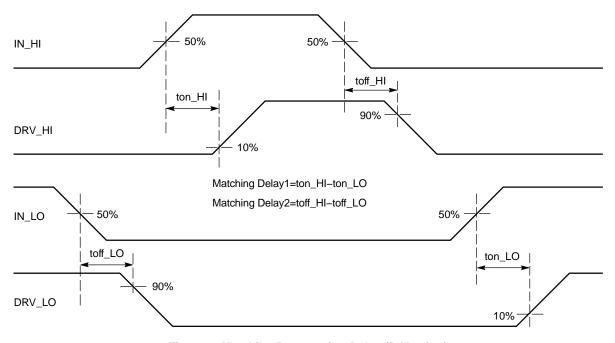


Figure 9. Matching Propagation Delay (B Version)

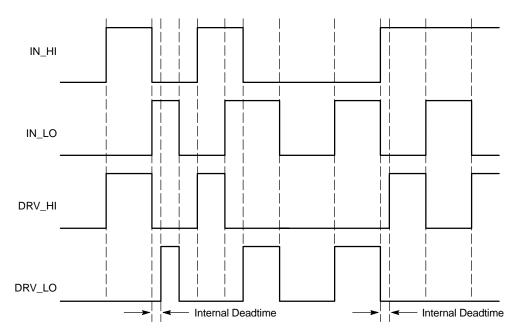
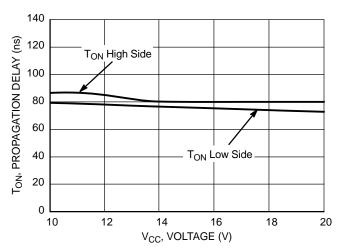


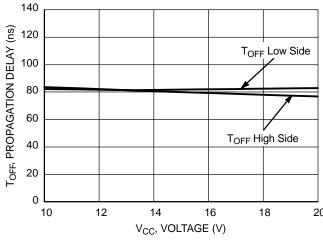
Figure 10. Input/Output Cross Conduction Output Protection Timing Diagram (B Version)



140 T_{ON}, PROPAGATION DELAY (ns) $T_{\mbox{ON}}$ Low Side 120 100 80 60 T_{ON} High Side 40 20 0 -20 20 60 -40 0 40 80 100 120 TEMPERATURE (°C)

Figure 11. Turn ON Propagation Delay vs. Supply Voltage ($V_{CC} = V_{BOOT}$)

Figure 12. Turn ON Propagation Delay vs.
Temperature



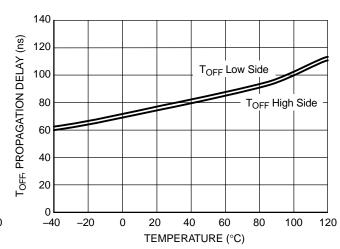
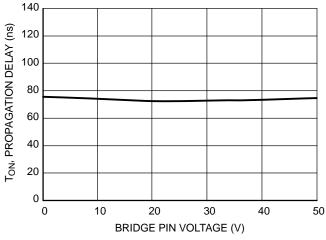


Figure 13. Turn OFF Propagation Delay vs. Supply Voltage ($V_{CC} = V_{BOOT}$)

Figure 14. Turn OFF Propagation Delay vs. Temperature



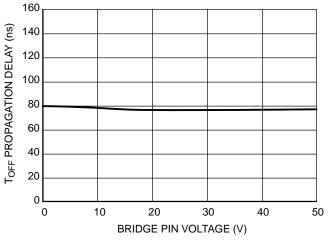


Figure 15. High Side Turn ON Propagation Delay vs. VBRIDGE Voltage

Figure 16. High Side Turn OFF Propagation Delay vs. VBRIDGE Voltage

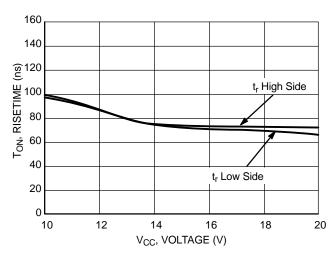


Figure 17. Turn ON Risetime vs. Supply Voltage ($V_{CC} = V_{BOOT}$)

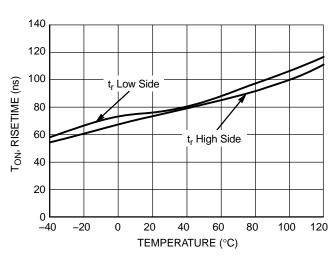


Figure 18. Turn ON Risetime vs. Temperature

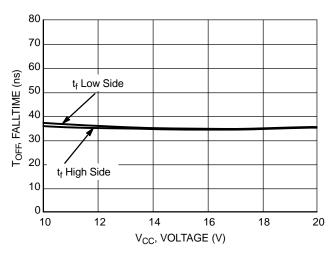


Figure 19. Turn OFF Falltime vs. Supply Voltage ($V_{CC} = V_{BOOT}$)

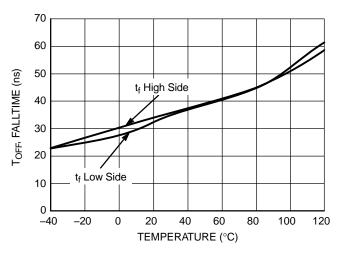


Figure 20. Turn OFF Falltime vs. Temperature

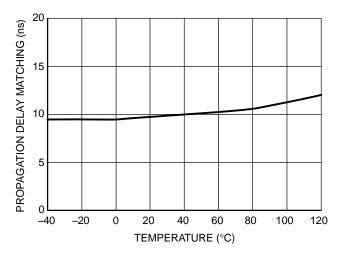


Figure 21. Propagation Delay Matching Between High Side and Low Side Driver vs. Temperature

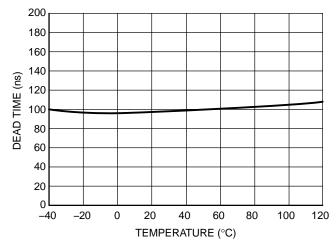


Figure 22. Dead Time vs. Temperature

CHARACTERIZATION CURVES

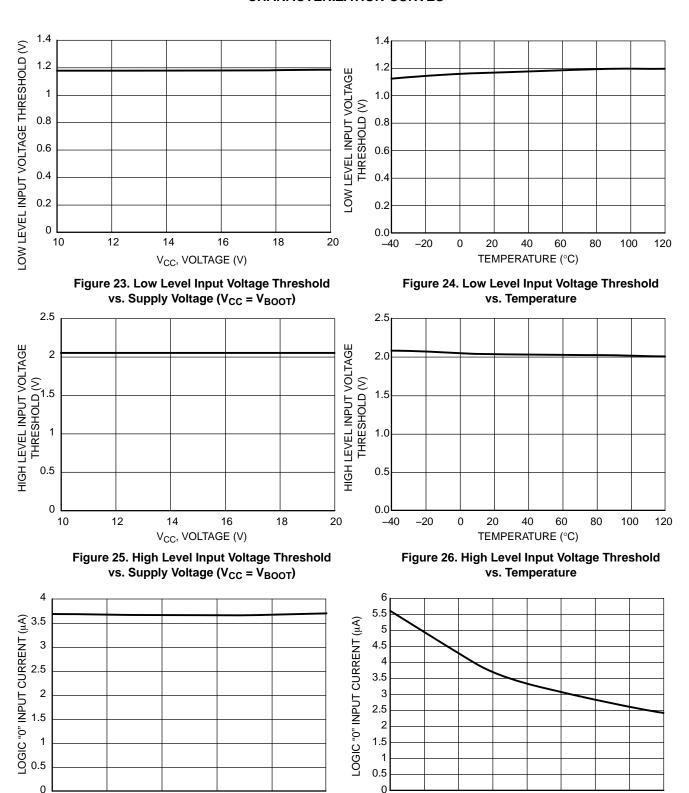


Figure 27. Logic "0" Input Current vs. Supply Voltage ($V_{CC} = V_{BOOT}$)

V_{CC}, VOLTAGE (V)

Figure 28. Logic "0" Input Current vs.
Temperature

TEMPERATURE (°C)

-20

-40

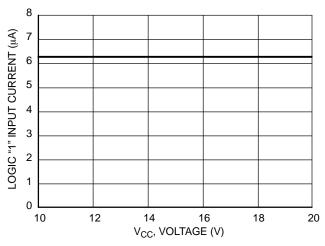


Figure 29. Logic "1" Input Current vs. Supply Voltage ($V_{CC} = V_{BOOT}$)

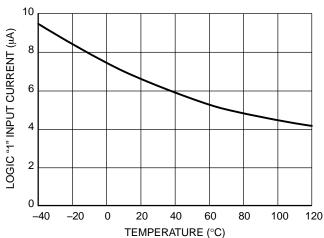


Figure 30. Logic "1" Input Current vs.
Temperature

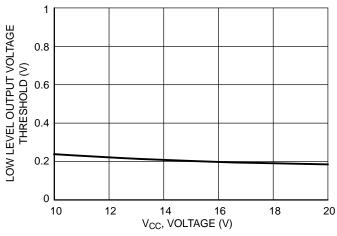


Figure 31. Low Level Output Voltage vs. Supply Voltage (V_{CC} = V_{BOOT})

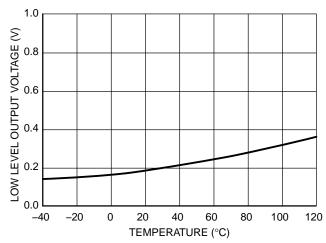


Figure 32. Low Level Output Voltage vs. Temperature

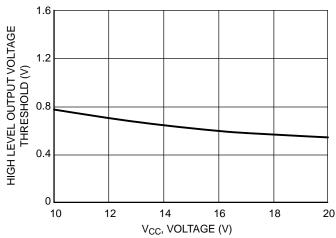


Figure 33. High Level Output Voltage vs. Supply Voltage ($V_{CC} = V_{BOOT}$)

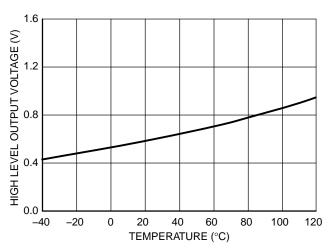
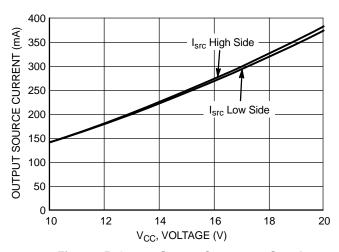


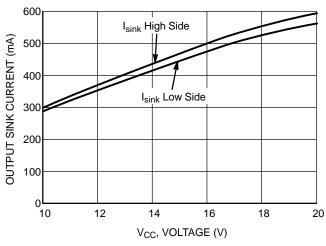
Figure 34. High Level Output Voltage vs. Temperature



400 OUTPUT SOURCE CURRENT (mA) 350 I_{src} High Side 300 250 200 $I_{\rm src}$ Low Side 150 100 50 0 40 -20 0 20 40 60 100 120 TEMPERATURE (°C)

Figure 35. Output Source Current vs. Supply Voltage ($V_{CC} = V_{BOOT}$)

Figure 36. Output Source Current vs. Temperature



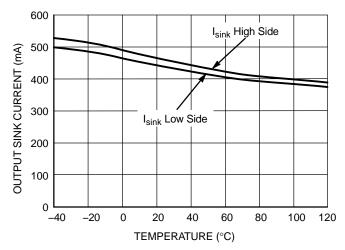


Figure 37. Output Sink Current vs. Supply Voltage ($V_{CC} = V_{BOOT}$)

Figure 38. Output Sink Current vs. Temperature

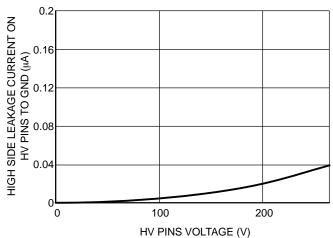


Figure 39. Leakage Current on High Voltage Pins (200 V) to Ground vs. V_{BRIDGE} Voltage (V_{BRIGDE} = V_{BOOT} = V_{DRV_HI})

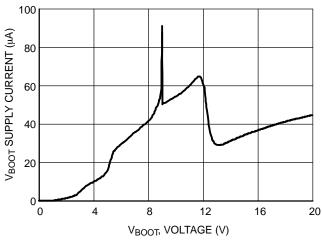


Figure 40. V_{BOOT} Supply Current vs. Bootstrap Supply Voltage

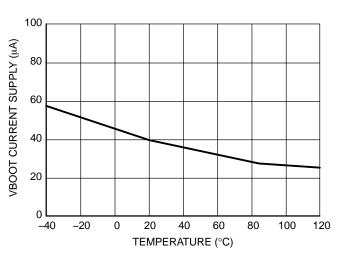


Figure 41. V_{BOOT} Supply Current vs. Temperature

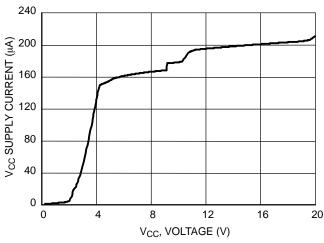


Figure 42. V_{CC} Supply Current vs. V_{CC} Supply Voltage

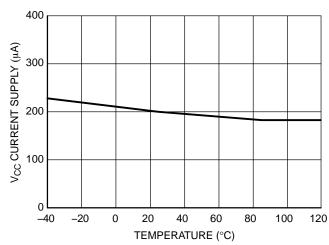


Figure 43. V_{CC} Supply Current vs. Temperature

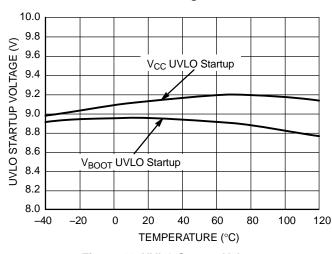


Figure 44. UVLO Startup Voltage vs. Temperature

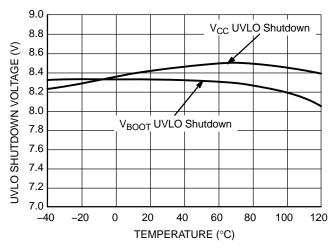


Figure 45. UVLO Shutdown Voltage vs. Temperature

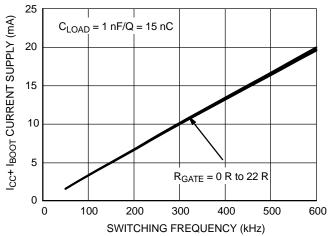


Figure 46. I_{CC1} Consumption vs. Switching Frequency with 15 nC Load on Each Driver @ V_{CC} = 15 V

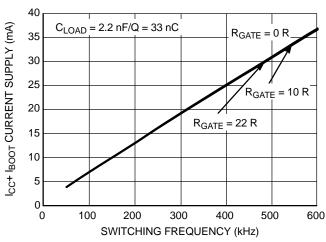


Figure 47. I_{CC1} Consumption vs. Switching Frequency with 33 nC Load on Each Driver @ V_{CC} = 15 V

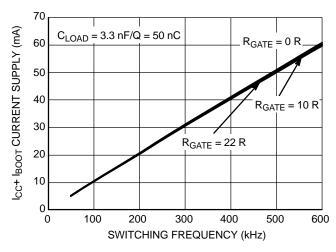


Figure 48. I_{CC1} Consumption vs. Switching Frequency with 50 nC Load on Each Driver @ V_{CC} = 15 V

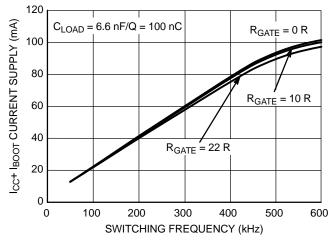


Figure 49. I_{CC1} Consumption vs. Switching Frequency with 100 nC Load on Each Driver @ V_{CC} = 15 V

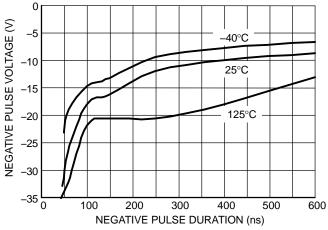


Figure 50. NCP5109A, Negative Voltage Safe Operating Area on the Bridge Pin

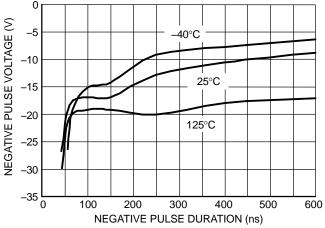


Figure 51. NCP5109B, Negative Voltage Safe Operating Area on the Bridge Pin

APPLICATION INFORMATION

Negative Voltage Safe Operating Area

When the driver is used in a half bridge configuration, it is possible to see negative voltage appearing on the bridge pin (pin 6) during the power MOSFETs transitions. When the high-side MOSFET is switched off, the body diode of the low-side MOSFET starts to conduct. The negative voltage applied to the bridge pin thus corresponds to the forward voltage of the body diode. However, as pcb copper tracks and wire bonding introduce stray elements (inductance and capacitor), the maximum negative voltage of the bridge pin will combine the forward voltage and the oscillations created by the parasitic elements. As any CMOS device, the deep negative voltage of a selected pin can inject carriers into the substrate, leading to an erratic behavior of the concerned component. ON Semiconductor provides characterization data of its half-bridge driver to show the maximum negative voltage the driver can safely operate with. To prevent the negative injection, it is the designer duty to verify that the amount of negative voltage pertinent to his/her application does not exceed the characterization curve we provide, including some safety margin.

In order to estimate the maximum negative voltage accepted by the driver, this parameter has been characterized over full the temperature range of the component. A test fixture has been developed in which we purposely negatively bias the bridge pin during the freewheel period of a buck converter. When the upper gate voltage shows signs of an erratic behavior, we consider the limit has been reached.

Figure 50 (or 51), illustrates the negative voltage safe operating area. Its interpretation is as follows: assume a negative 10 V pulse featuring a 100 ns width is applied on the bridge pin, the driver will work correctly over the whole die temperature range. Should the pulse swing to -20 V, keeping the same width of 100 ns, the driver will not work properly or will be damaged for temperatures below 125° C.

Summary:

- If the negative pulse characteristic (negative voltage level & pulse width) is above the curves the driver runs in safe operating area.
- If the negative pulse characteristic (negative voltage level & pulse width) is below one or all curves the driver will NOT run in safe operating area.

Note, each curve of the Figure 50 (or 51) represents the negative voltage and width level where the driver starts to fail at the corresponding die temperature.

If in the application the bridge pin is too close of the safe operating limit, it is possible to limit the negative voltage to the bridge pin by inserting one resistor and one diode as follows:

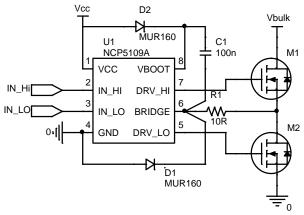


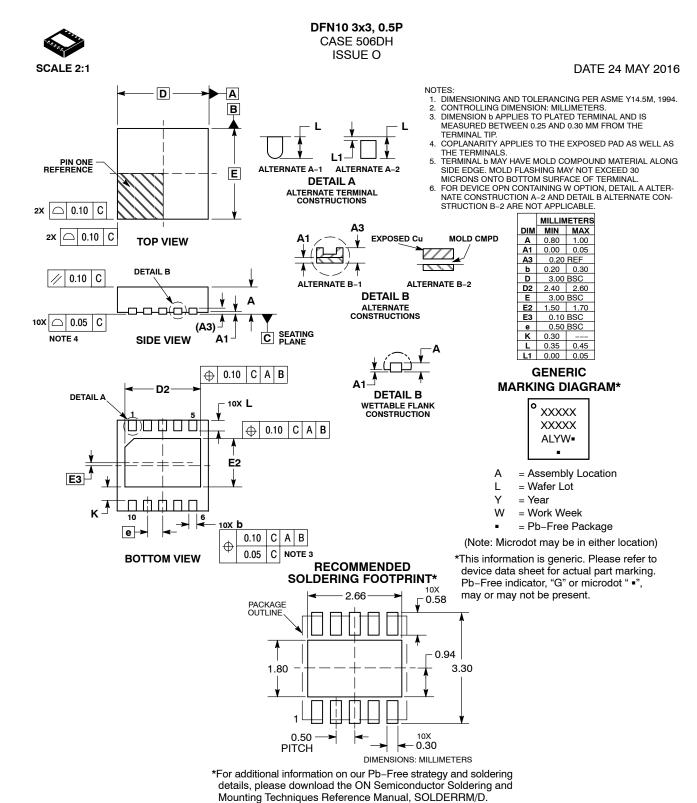
Figure 52. R1 and D1 Improves the Robustness of the Driver

R1 and D1 should be placed as close as possible of the driver. D1 should be connected directly between the bridge pin (pin 6) and the ground pin (pin 4). By this way the negative voltage applied to the bridge pin will be limited by D1 and R1 and will prevent any wrong behavior.

ORDERING INFORMATION

Device	Package	Shipping [†]
NCP5109ADR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel
NCP5109BDR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel
NCP5109AMNTWG	DFN10 (Pb-Free)	3000 / Tape & Reel
NCP5109BMNTWG	DFN10 (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



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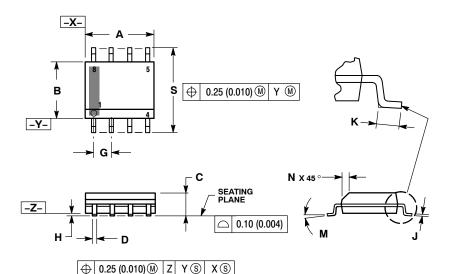
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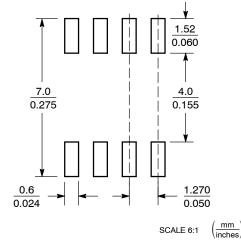
DATE 16 FEB 2011



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER
- ANSI Y14.5M, 1982.
 CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
- MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE
- DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
- 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

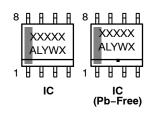
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
Α	4.80	5.00	0.189	0.197
В	3.80	4.00	0.150	0.157
С	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
Н	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
М	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



^{*}For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code = Assembly Location = Wafer Lot = Year = Work Week W

= Pb-Free Package

XXXXXX XXXXXX AYWW AYWW Ŧ \mathbb{H} Discrete **Discrete** (Pb-Free)

XXXXXX = Specific Device Code = Assembly Location Α = Year ww = Work Week = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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DATE 16 FEB 2011

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STYLE 5: PIN 1. DRAIN 2. DRAIN 3. DRAIN 4. DRAIN 5. GATE 6. GATE 7. SOURCE 8. SOURCE	STYLE 6: PIN 1. SOURCE 2. DRAIN 3. DRAIN 4. SOURCE 5. SOURCE 6. GATE 7. GATE 8. SOURCE	STYLE 7: PIN 1. INPUT 2. EXTERNAL BYPASS 3. THIRD STAGE SOURCE 4. GROUND 5. DRAIN 6. GATE 3 7. SECOND STAGE Vd 8. FIRST STAGE Vd	STYLE 8: PIN 1. COLLECTOR, DIE #1 2. BASE. #1
STYLE 9: PIN 1. EMITTER, COMMON 2. COLLECTOR, DIE #1 3. COLLECTOR, DIE #2 4. EMITTER, COMMON 5. EMITTER, COMMON 6. BASE, DIE #2 7. BASE, DIE #1 8. EMITTER, COMMON	STYLE 10: PIN 1. GROUND 2. BIAS 1 3. OUTPUT 4. GROUND 5. GROUND 6. BIAS 2 7. INPUT 8. GROUND	STYLE 11: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. DRAIN 2 7. DRAIN 1 8. DRAIN 1	STYLE 12: PIN 1. SOURCE 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN
STYLE 13: PIN 1. N.C. 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN	STYLE 14: PIN 1. N-SOURCE 2. N-GATE 3. P-SOURCE 4. P-GATE 5. P-DRAIN 6. P-DRAIN 7. N-DRAIN 8. N-DRAIN	STYLE 15: PIN 1. ANODE 1 2. ANODE 1 3. ANODE 1 4. ANODE 1 5. CATHODE, COMMON 6. CATHODE, COMMON 7. CATHODE, COMMON 8. CATHODE, COMMON	STYLE 16: PIN 1. EMITTER, DIE #1 2. BASE, DIE #1 3. EMITTER, DIE #2 4. BASE, DIE #2 5. COLLECTOR, DIE #2 7. COLLECTOR, DIE #2 8. COLLECTOR, DIE #1 8. COLLECTOR, DIE #1
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STYLE 25: PIN 1. VIN 2. N/C 3. REXT 4. GND 5. IOUT 6. IOUT 7. IOUT 8. IOUT	STYLE 26: PIN 1. GND 2. dv/dt 3. ENABLE 4. ILIMIT 5. SOURCE 6. SOURCE 7. SOURCE 8. VCC	STYLE 27: PIN 1. ILIMIT 2. OVLO 3. UVLO 4. INPUT+ 5. SOURCE 6. SOURCE 7. SOURCE 8. DRAIN	STYLE 28: PIN 1. SW TO GND 2. DASIC OFF 3. DASIC SW_DET 4. GND 5. V_MON 6. VBULK 7. VBULK 8. VIN
STYLE 29: PIN 1. BASE, DIE #1 2. EMITTER, #1 3. BASE, #2 4. EMITTER, #2 5. COLLECTOR, #2 6. COLLECTOR, #2 7. COLLECTOR, #1 8. COLLECTOR, #1	STYLE 30: PIN 1. DRAIN 1 2. DRAIN 1 3. GATE 2 4. SOURCE 2 5. SOURCE 1/DRAIN 2 6. SOURCE 1/DRAIN 2 7. SOURCE 1/DRAIN 2 8. GATE 1		

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