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Diodes Incorporated for Discrete and Analog Semiconductors

QPAK/PPAP- 2605

Qualification Report



Manufacturer No.: BAV70W-7-F

Revision 0

Date: September 29, 2010

Qualified By: Shanghai Kaihong Electronic Co., Ltd. & Diodes Shanghai Electronic Co., Ltd

Also Applicable To: BAV70W-7-F is Qualified By Similarity to BAV70LP-7-F. The included

Certificate of Design and Construction and the Reliability Test Summary are

for the BAV70LP-7-F.

Prepared By: Diodes DAL. Document Control Date September 29, 2010

Approved By: Doiodes DAL. QRA Department Date September 29, 2010



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DIODES INCORPORATED

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DUAL SURFACE MOUNT SWITCHING DIODE

Features

- Fast Switching Speed
- Ultra-Small Surface Mount Package
- For General Purpose Switching Applications
- High Conductance
- Lead Free/RoHS Compliant (Note 3)
- Qualified to AEC-Q101 Standards for High Reliability
- "Green" Device (Notes 4 and 5)

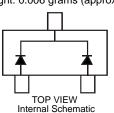
Mechanical Data

- Case: SOT-323
- Case Material: Molded Plastic, "Green" Molding Compound, Note 5. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020D
- Terminals: Solderable per MIL-STD-202, Method 208
- Lead Free Plating (Matte Tin Finish annealed over Alloy 42 leadframe)
- Polarity: See Diagram
- Marking Information: See Page 3
- Ordering Information: See Page 3
- Weight: 0.006 grams (approximate)

SOT-323



TOP VIEW



Maximum Ratings @T_A = 25°C unless otherwise specified

Characteristic		Symbol	Value	Unit
Non-Repetitive Peak Reverse Voltage		V_{RM}	100	V
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage		V _{RRM} V _{RWM} V _R	75	V
RMS Reverse Voltage		V _{R(RMS)}	53	V
Forward Continuous Current (Note 1)		I _{FM}	300	mA
Average Rectified Output Current (Note 1)		lo	150	mA
Non-Repetitive Peak Forward Surge Current (Note 1)	@ t = 1.0μs @ t = 1.0s	I _{FSM}	2.0 1.0	А

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Power Dissipation (Note 1)	P _D	200	mW
Thermal Resistance Junction to Ambient Air (Note 1)	$R_{ hetaJA}$	625	°C/W
Operating and Storage Temperature Range	T _J , T _{STG}	-65 to +150	°C

Electrical Characteristics @T_A = 25°C unless otherwise specified

Characteristic	Symbol	Min	Max	Unit	Test Condition
Reverse Breakdown Voltage (Note 2)	V _{(BR)R}	75	_	V	$I_R = 100 \mu A$
Forward Voltage	V _F	_	0.715 0.855 1.0 1.25	V	I _F = 1.0mA I _F = 10mA I _F = 50mA I _F = 150mA
Reverse Current (Note 2)	I _R	_	2.5 50 30 25	μΑ μΑ μΑ nA	$V_R = 75V$ $V_R = 75V$, $T_{J} = 150$ °C $V_R = 25V$, $T_{J} = 150$ °C $V_R = 20V$
Total Capacitance	C _T	_	2.0	pF	$V_R = 0, f = 1.0MHz$
Reverse Recovery Time	t _{rr}	_	4.0	ns	$I_F = I_R = 10 \text{mA},$ $I_{rr} = 0.1 \times I_R, R_L = 100 \Omega$

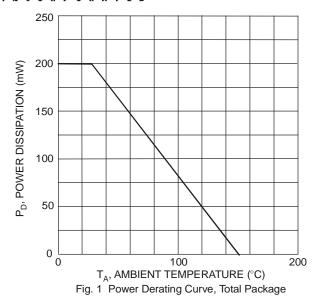
Notes:

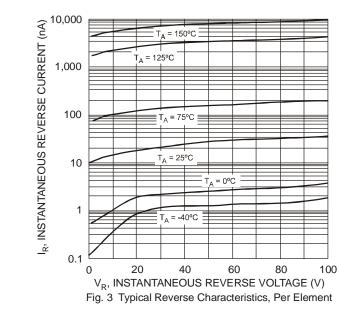
- Device mounted on FR-4 PC board with recommended pad layout, which can be found on our website at http://www.diodes.com/datasheets/ap02001.pdf.
- Short duration pulse test used to minimize self-heating effect.
- No purposefully added lead.

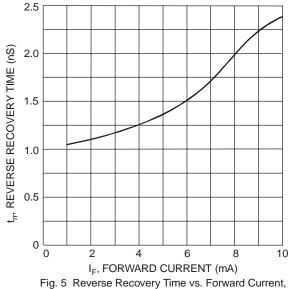
Document number: DS30063 Rev. 9 - 2

- Diodes Inc.'s "Green" policy can be found on our website at http://www.diodes.com/products/lead_free/index.php.
- Product manufactured with Date Code 0627 (week 27, 2006) and newer are built with Green Molding Compound. Product manufactured prior to Date Code 0627 are built with Non-Green Molding Compound and may contain Halogens or Sb₂O₃ Fire Retardants.

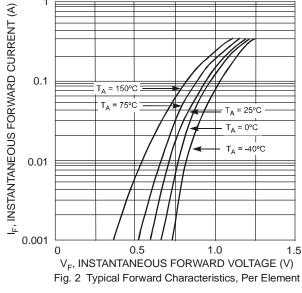








Per Element



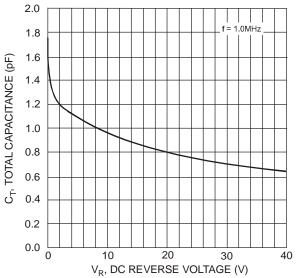


Fig. 4 Total Capacitance vs. Reverse Voltage, Per Element



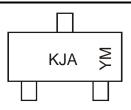
Ordering Information (Notes 5 & 6)

Part Number	Case	Packaging
BAV70W-7-F	SOT-323	3000/Tape & Reel

Notes:

6. For packaging details, go to our website at http://www.diodes.com/datasheets/ap02007.pdf.

Marking Information



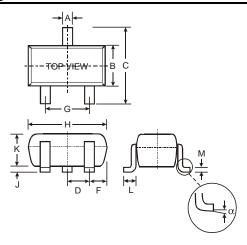
KJA = Product Type Marking Code YM = Date Code Marking Y = Year ex: N = 2002

M = Month ex: 9 = September

Date Code Key

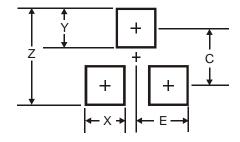
Year	2000	2001	2002	2003	2004	2005	2006	200	7 2008	2009	2010	2011	2012
Code	L	М	N	Р	R	S	Т	U	V	W	Х	Υ	Z
Month	Jan	Feb	Mar	Apr	Ма	y J	un	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5		6	7	8	9	0	Z	D

Package Outline Dimensions



SOT-323						
Dim	Max					
Α	0.25	0.40				
В	1.15	1.35				
С	2.00	2.20				
D	0.65 N	ominal				
F	0.30	0.40				
G	1.20	1.40				
Н	1.80	2.20				
J	0.0	0.10				
K	0.90	1.00				
L	0.25	0.40				
M	0.10	0.18				
α	0°	8°				
All Di	mensions	in mm				

Suggested Pad Layout



Dimensions	Value (in mm)
Z	2.8
X	0.7
Υ	0.9
С	1.9
F	1.0

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CERTIFICATE OF DESIGN AND CONSTRUCTION

Assembly and Test Site	DIODES INC	Glass transition temperature (T _G)	135℃
DIC P/N	BAV70LP-7	Lead material type	SLP1006P2(C7025HH)
Package Type	DFN1006-3	Lead Material manufacturer	ASM/MHT
DIE P/N	5DS21MQ	Lead plating/ coating	Pb free
Die line or process	Planar process technology	Lead frame material type	С7025НН
Wafer Diameter	5 inch	Header plating (Die land area)	NiPdAu
Wafer Fab Site(s)	Phenitec	Max junction temperature(T _j)	150℃
ID method (multiple sites)	N/A	Max thermal resistance junction to case (θ_{JC})	N/A
Assembly Locations(s)	Shanghai Kaihong Electronic Co., Ltd.	Max thermal resistance junction to ambient $(\theta_{JA})^*$	N/A
	Diodes Shanghai Co.,Ltd		
Test Locations(s)	Diodes Shanghai Co.,Ltd	Front metal type (Top layer)	Al
Die attach Method / Material	Epoxy(QMI519)	Front metal thickness (Top layer)	N/A
Bond wire material & dia.	Gold wire/0.8mil	Back metal type (All layers)	AuAs
Bond type (at top side of the die)	Thermo-Ultrasonic	Back metal thickness (all Layers)	N/A
Bond type (at leadframe)	Ероху	Die conforming coating	Classified information
No. of bonds over active area	1	Die size (width x length x thickness) in mm	0.390 x 0.390 x0.138
Package material type	EME-G770HCD	Die passivation thickness range	Not specified
Package material manufacturer	Sumitomo	No. of mask steps	6

^{*}Show conditions (i.e. pad size, board material, copper thickness, etc.

Attachments:

1) Die Photo

2) Package outline drawing

- 3) Die cross-section drawing
- 4) Wire bond & die placement diagram
- 5) Test circuits, bias levels and conditions

Requirements:

A separate Certificate of Design, Construction and Qualification shall be submitted for each P/N and assembly location.

Document shall be signed by a responsible individual at the supplier who can verify that all of the above information is correct. Type name and sign.

Completed by		Date	Certified by	Date
Typed/Printed	Hill Chen	September 16, 2010	Phil Mao	September 16, 2010
Signature				
Title	Wafer Engineer		Wafer section Mgr	

Rel Date: 5 Dec 07

Print Date: 9/29/10 3:30 PM

FACTORY:		PART NUMBER :BAV70LP SWB0816038 CUSTON	/FR·						
I ACTORT.		PART NUMBER :BAV70LP SWB0816038 CUSTOMER: Package:DFN1006-3 DIODES INC.:							
ABORATORY	' (If Different):	PART DESCRIPTION: Qualification for 5DS21M,EM			J ,QMI519				
DW-008 (AEC Q101) Test# Test Description		Test Conditions	#Lots	#To Test	Results	REMARKS			
7.3.2 (1)	PRE- AND POST- STRESS ELECTRICAL TEST (TEST)	Per Spec							
7.3.3 (2)	PRECONDITIONING (PC)	JSED22 A-113 N/A for Axial	1	385	0/385				
7.3.5.1 (3)	EXTERNAL VISUAL (EV)	MIL-STD-750 METHOD 2071	1	500	0/500				
7.3.5.2 (4)	PARAMETRIC VERIFICATION (PV)	Per Data Sheet Ta1=-55°C, Ta2=25°C, Ta3=85°C, Ta4=150°C Characteristic BVDSS@VGS=0V, ID=250uA Characteristic IDSS@VDS=30V, VGS=0V	1 of 3	25					
	Lot #2	Characteristic IGSS@VGS=±20V, VDS=0V Characteristic IGSS@VGS=±25V, VDS=0V Characteristic VGS(th)@VDS=VGS, ID=250uA Characteristic RDSON@VGS=10V, ID=5.8A	2 of 3	25					
	Lot #3	Characteristic RDSON@VGS=4.5V, ID=4.2A Characteristic yFS@VDS=5V,ID=4.2A Characteristic VSD@VGS=0V,IS=2.0A	3 of 3	25					
7.3.5.3	FORWARD SURGE	MIL-750D, Method 4066	1	45					
7.3.5.4 (5)	HIGH TEMP. REVERSE BIAS (HTRB)	T=150*C Vr=60V, PER JESD22 A-108	1	77					
	Pretest		1	77	0/77				
	@ 500 Hours	T=150*C Vr=60V, PER JESD22 A-108	1	77	0/77				
	Final 1000 Hours	T=150*C Vr=60V, PER JESD22 A-108	1	77	0/77				
(6)	HIGH TEMP GATE BIAS (HTGB)	MIL-750D, Method 4066	1	77					
7.3.5.5 (7)	TEMPERATURE CYCLING (TC)	T=-65*C-150*C, PER JESD22 A-104	1	77					
(Pretest		1	77	0/77				
	@ 500Cycles	T=-65*C-150*C, PER JESD22 A-104	1	77	0/77				
7050(0)	Final 1000 Cycles	T=-65*C-150*C, PER JESD22 A-104	1	77	0/77				
7.3.5.6 (8)	AUTOCLAVE (AC)	T=121*C 15PSIG 100%RH	1	77	0/77				
7.3.5.7 (9)	H³TRB Pretest	T=85*C RH=85% Vr=60V	1	77	0/77				
	@ 500Hours	T=85*C RH=85% Vr=60V	1	77	0/77				
	Final 1000 Hours	T=85*C RH=85% Vr=60V	1	77	0/77				
7.3.5.8 (10)	INTERMITTENTOPERATING LIFE (IOL)	If=150mA, PER MIL-STD-750 METHOD 1037	1	77		2 min on/off			
	Pretest	MIL-STD-750 METHOD 1037	1	77	0/77				
-	Midpoint	MIL-STD-750 METHOD 1037	1	77	0/77				
	After	MIL-STD-750 METHOD 1037	1	77	0/77				
(10a)	POWER AND TEMP. CYCLE (PTC)	JESD22 A-105, Per Table AEC-Q101, p11	1	77					
(Optional)	Pretest Midpoint	JESD22 A-105, Per Table AEC-Q101, p11 JESD22 A-105, Per Table AEC-Q101, p11	1 1	77					
	Midpoint After	JESD22 A-105, Per Table AEC-Q101, p11 JESD22 A-105, Per Table AEC-Q101, p11	1	77					
7.3.5.9 (11)	ESD CHARACTERIZATION (ESD)	PER AEC-Q101-001 & -002	1	60					
	D.P.A. (DPA)	AEC Q101-004 SEC. 4	1	6					
	PHYSICAL DIMENSION (PD)	PER JESD22 B-100	1	25	0/25				
	TERMINAL STRENGTH (TS) RESISTANCE TO SOLVENTS (RTS)	MIL-STD-750, Method 2036 JESD22 B-107	1 1	30					
(16)	CONSTANT ACCELERATION (CA)	N/A, not hermetically sealed device.	N/A	N/A					
(17)	VIBRATION VARIABLE FREQUENCY (VVF		N/A	N/A					
. ,	RESISTANCE TO SOLDER HEAT (RSH)	JESD22 B-106	1	30	0/30	260*C @30S			
. ,	SOLDERABILITY (SD)	J-STD-002	1	10	0/10	245*C @5S			
. ,	THERMAL RESISTANCE (TR)	JESD 24-3, 24-4, 24-6 as appropriate	1	10					
. ,	WIRE BOND STRENGTH (WBS)	MIL-STD-750 METHOD 2037	1	25	0/25				
,	BOND SHEAR (BS)	AEC-Q101-003	1	25	0/25				
7.3.5.19 (25)	DIE SHEAR (DS)	MIL-STD-750 METHOD 2017	1	25	0/25				