SPST CMOS ANALOG SWITCHES

FEATURES

- **2-V to 12-V Single-Supply Operation**
- **Specified ON-State Resistance:**
    - **15 Ω Max With 12-V Supply**
    - **20 Ω Max With 5-V Supply**
    - **50 Ω Max With 3.3-V Supply**
- **Specified Low OFF-Leakage Currents:**
    - **1 nA at 25°C**
    - **10 nA at 85°C**

- **Specified Low ON-Leakage Currents:**
    - **1 nA at 25°C**
    - **10 nA at 85°C**
- **Low Charge Injection: 11.5 pC (12-V Supply)**
- **Fast Switching Speed:**
  t_{ON} = 80 ns, t_{OFF} = 50 ns (12-V Supply)
- **Break-Before-Make Operation (t_{ON} > t_{OFF})**
- **TTL/CMOS-Logic Compatible With 5-V Supply**

DESCRIPTION/ORDERING INFORMATION

The TS12A4514/TS12A4515 are single pole/single throw (SPST), low-voltage, single-supply CMOS analog switches, with very low switch ON-state resistance. The TS12A4514 is normally open (NO). The TS12A4515 is normally closed (NC).

These CMOS switches can operate continuously with a single supply between 2 V and 12 V. Each switch can handle rail-to-rail analog signals. The OFF-leakage current maximum is only 1 nA at 25°C or 10 nA at 85°C.

All digital inputs have 0.8-V to 2.4-V logic thresholds, ensuring TTL/CMOS-logic compatibility when using a 5-V supply.

For pin-compatible parts for use with dual supplies, see the TS12A4516/TS12A4517.

ORDERING INFORMATION

T_A	PACKAGE[(1)(2)]		ORDERABLE PART NUMBER	TOP-SIDE MARKING[(3)]
−40°C to 85°C	PDIP – P	Reel of 1000	TS12A4514P	TS12A4514P
	SOIC – D	Reel of 1500	TS12A4514D	YD514
		Reel of 2500	TS12A4514DR	
	SOP (SOT-23) – DBV	Reel of 3000	TS12A4514DBVR	9CJ_
	PDIP – P	Reel of 1000	TS12A4515P	TS12A4515P
	SOIC – D	Reel of 1500	TS12A4515D	YD515
		Reel of 2500	TS12A4515DR	
	SOP (SOT-23) – DBV	Reel of 3000	TS12A4515DBVR	9CK_

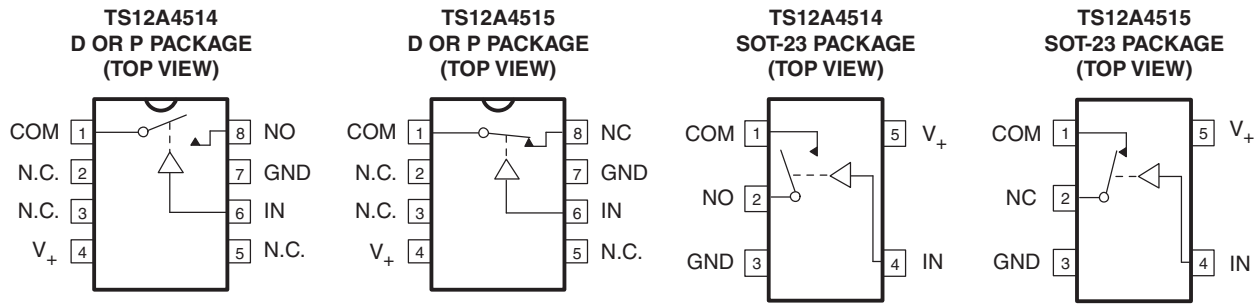(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(3) DBV: The last character designates assembly/test Site
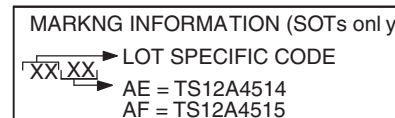
⚠ Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TS12A4514, TS12A4515

PIN CONFIGURATIONS

TS12A4514
D OR P PACKAGE
(TOP VIEW)

```
COM  1            8  NO
N.C. 2            7  GND
N.C. 3            6  IN
V+   4            5  N.C.
```

TS12A4515
D OR P PACKAGE
(TOP VIEW)

```
COM  1            8  NC
N.C. 2            7  GND
N.C. 3            6  IN
V+   4            5  N.C.
```

TS12A4514
SOT-23 PACKAGE
(TOP VIEW)

```
COM  1            5  V+
NO   2
GND  3            4  IN
```

TS12A4515
SOT-23 PACKAGE
(TOP VIEW)

```
COM  1            5  V+
NC   2
GND  3            4  IN
```

INPUT	SWITCH STATE	
	TS12A4514	TS12A4515
LOW	OFF	ON
HIGH	ON	OFF

MARKNG INFORMATION (SOTs onl y)

XX_XX → LOT SPECIFIC CODE
AE = TS12A4514
AF = TS12A4515

N.C. – Not internally connected

NO – Normally open

NC – Normally closed

Absolute Minimum and Maximum Ratings[1][2]

voltages referenced to GND

		MIN	MAX	UNIT
V_+	Supply voltage range[3]	−0.3	13	V
V_{NC} V_{NO} V_{COM}	Analog voltage range[4]	−0.3	$V_+ + 0.3$ or ±20 mA	V
	Continuous current into any terminal		±20	mA
	Peak current, NO or COM (pulsed at 1 ms, 10% duty cycle)		±30	mA
	ESD per method 3015.7		>2000	V
	Continuous power dissipation (T_A = 70°C) — 8-pin plastic DIP (derate 9.09 mW/°C above 70°C)		727	mW
	8-pin SOIC (derate 5.88 mW/°C above 70°C)		471	
	5-pin SOT-23 (derate 7.1 mW/°C above 70°C)		571	
T_A	Operating temperature range	−40	85	°C
T_{stg}	Storage temperature range	−65	150	°C
	Lead temperature (soldering, 10 s)		300	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(3) All voltages are with respect to ground, unless otherwise specified.
(4) Voltages exceeding V_+ or GND on any signal terminal are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Product Folder Link(s): *TS12A4514 TS12A4515*

Electrical Characteristics for 5-V Supply[1]

V_+ = 4.5 V to 5.5 V, V_{INH} = 2.4 V, V_{INL} = 0.8 V, T_A = −40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	MIN	TYP[2]	MAX	UNIT
Analog Switch							
Analog signal range	V_{COM}, V_{NO}, V_{NC}			0		V_+	V
ON-state resistance	r_{on}	V_+ = 4.5 V, V_{COM} = 3.5 V, I_{COM} = 1 mA	25°C		9.5	15	Ω
			Full			20	
ON-state resistance flatness	$r_{on(flat)}$	V_{COM} = 1 V, 2 V, 3 V, I_{COM} = 1 mA	25°C		1	3	Ω
			Full			4	
NO, NC OFF leakage current[3]	$I_{NO(OFF)}$, $I_{NC(OFF)}$	V_+ = 5.5 V, V_{COM} = 1 V, V_{NO} or V_{NC} = 4.5 V	25°C			1	nA
			Full			10	
COM OFF leakage current[3]	$I_{COM(OFF)}$	V_+ = 5.5 V, V_{COM} = 1 V, V_{NO} or V_{NC} = 4.5 V	25°C			1	nA
			Full			10	
COM ON leakage current[3]	$I_{COM(ON)}$	V_+ = 5.5 V, V_{COM} = 4.5 V, V_{NO} or V_{NC} = 4.5 V	25°C			1	nA
			Full			10	
Digital Control Input (IN)							
Input logic high	V_{IH}		Full	2.4		V_+	V
Input logic low	V_{IL}		Full	0		0.8	V
Input leakage current	I_{IH}, I_{IL}	V_{IN} = V_+, 0 V	Full			0.01	μA
Dynamic							
Turn-on time	t_{ON}	see Figure 2	25°C		32	100	ns
			Full			125	
Turn-off time	t_{OFF}	see Figure 2	25°C		25	50	ns
			Full			60	
Charge injection[4]	Q_C	C_L = 1 nF, V_{NO} = 0 V, R_S = 0 Ω, See Figure 1	25°C		−3		pC
NO, NC OFF capacitance	$C_{NO(OFF)}$, $C_{NC(OFF)}$	f = 1 MHz, See Figure 4	25°C		7.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	f = 1 MHz, See Figure 4	25°C		7.5		pF
COM ON capacitance	$C_{COM(ON)}$	f = 1 MHz, See Figure 4	25°C		19		pF
Digital input capacitance	C_I	V_{IN} = V_+, 0 V	25°C		1.5		pF
Bandwidth	BW	R_L = 50 Ω, C_L = 15 pF, V_{NO} = 1 V_{RMS}, f = 100 kHz	25°C		475		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, C_L = 15 pF, V_{NO} = 1 V_{RMS}, f = 100 kHz	25°C		−94		dB
Total harmonic distortion	THD	R_L = 50 Ω, C_L = 15 pF, V_{NO} = 1 V_{RMS}, f = 100 kHz	25°C		0.08		%
Supply							
V_+ supply current	I_+	V_{IN} = 0 V or V_+	25°C			0.05	μA
			Full			0.1	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(2) Typical values are at T_A = 25°C.
(3) Leakage parameters are 100% tested at maximum-rated hot operating temperature, and are ensured by correlation at 25°C.
(4) Specified by design, not production tested

TEXAS INSTRUMENTS

Electrical Characteristics for 12-V Supply[1]

V_+ = 11.4 V to 12.6 V, V_{INH} = 5 V, V_{INL} = 0.8 V, T_A = −40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	MIN	TYP[2]	MAX	UNIT
Analog Switch							
Analog signal range	V_{COM}, V_{NO}, V_{NC}			0		V_+	V
ON-state resistance	r_{on}	V_+ = 11.4 V, V_{COM} = 10 V, I_{COM} = 1 mA	25°C		6.5	10	Ω
			Full			15	
ON-state resistance flatness	$r_{on(flat)}$	V_+ = 11.4 V, V_{COM} = 2 V, 5 V, 10 V, I_{COM} = 1 mA	25°C		1.5	3	Ω
			Full			4	
NO, NC OFF leakage current[3]	$I_{NO(OFF)}$, $I_{NC(OFF)}$	V_+ = 12.6 V, V_{COM} = 1 V, V_{NO} or V_{NC} = 10 V	25°C			1	nA
			Full			10	
COM OFF leakage current[3]	$I_{COM(OFF)}$	V_+ = 12.6 V, V_{COM} = 1 V, V_{NO} or V_{NC} = 10 V	25°C			1	nA
			Full			10	
COM ON leakage current[3]	$I_{COM(ON)}$	V_+ = 12.6 V, V_{COM} = 10 V, V_{NO} or V_{NC} = 10 V	25°C			1	nA
			Full			10	
Digital Control Input (IN)							
Input logic high	V_{IH}		Full	5		V_+	V
Input logic low	V_{IL}		Full	0		0.8	V
Input leakage current	I_{IH}, I_{IL}	V_{IN} = V_+, 0 V	Full			0.01	µA
Dynamic							
Turn-on time	t_{ON}	See Figure 2	25°C		22	75	ns
			Full			80	
Turn-off time	t_{OFF}	See Figure 2	25°C		20	45	ns
			Full			50	
Charge injection[4]	Q_C	C_L = 1 nF, V_{NO} = 0 V, R_S = 0 Ω, See Figure 1	25°C		−11.5		pC
NO, NC OFF capacitance	$C_{NO(OFF)}$ $C_{NC(OFF)}$	f = 1 MHz, See Figure 4	25°C		7.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	f = 1 MHz, See Figure 4	25°C		7.5		pF
COM ON capacitance	$C_{COM(ON)}$	f = 1 MHz, See Figure 4	25°C		21.5		pF
Digital input capacitance	C_I	V_{IN} = V_+, 0 V	25°C		1.5		pF
Bandwidth	BW	R_L = 50 Ω, C_L = 15 pF, V_{NO} = 1 V_{RMS}, f = 100 kHz	25°C		520		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, C_L = 15 pF, V_{NO} = 1 V_{RMS}, f = 100 kHz	25°C		−95		dB
Total harmonic distortion	THD	R_L = 50 Ω, C_L = 15 pF, V_{NO} = 1 V_{RMS}, f = 100 kHz	25°C		0.07		%
Supply							
V_+ supply current	I_+	V_{IN} = 0 V or V_+	25°C			0.05	µA
			Full			0.2	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(2) Typical values are at T_A = 25°C.
(3) Leakage parameters are 100% tested at maximum-rated hot operating temperature, and are ensured by correlation at 25°C.
(4) Specified by design, not production tested

Product Folder Link(s): *TS12A4514 TS12A4515*

Electrical Characteristics for 3-V Supply[1]

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	MIN	TYP[2]	MAX	UNIT
Analog Switch							
Analog signal range	V_{COM}, V_{NO}, V_{NC}			0		V_+	V
ON-state resistance	r_{on}	V_+ = 3 V, V_{COM} = 1.5 V, I_{NO} = 1 mA,	25°C		18.5	40	Ω
			Full			50	
ON-state resistance flatness	$r_{on(flat)}$	V_+ = 3 V, V_{COM} = 1 V, 1.5 V, 2 V, I_{COM} = 1 mA	25°C		1	3	Ω
			Full			4	
NO, NC OFF leakage current[3]	$I_{NO(OFF)}$, $I_{NC(OFF)}$	V_+ = 3.6 V, V_{COM} = 1 V, V_{NO} or V_{NC} = 3 V	25°C			1	nA
			Full			10	
COM OFF leakage current[3]	$I_{COM(OFF)}$	V_+ = 3.6 V, V_{COM} = 1 V, V_{NO} or V_{NC} = 3 V	25°C			1	nA
			Full			10	
COM ON leakage current[3]	$I_{COM(ON)}$	V_+ = 3.6 V, V_{COM} = 3 V, V_{NO} or V_{NC} = 3 V	25°C			1	nA
			Full			10	
Digital Control Input (IN)							
Input logic high	V_{IH}		Full	2.4		V_+	V
Input logic low	V_{IL}		Full	0		0.8	V
Input leakage current	I_{IH}, I_{IL}	V_{IN} = V_+, 0 V	Full			0.01	µA
Dynamic							
Turn-on time[4]	t_{ON}	See Figure 2	25°C		63	120	ns
			Full			175	
Turn-off time[4]	t_{OFF}	See Figure 2	25°C		33	80	ns
			Full			120	
Charge injection[4]	Q_C	C_L = 1 nF, See Figure 1	25°C		–1.5		pC
NO, NC OFF capacitance	$C_{NO(OFF)}$, $C_{NC(OFF)}$	f = 1 MHz, See Figure 4	25°C		7.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	f = 1 MHz, See Figure 4	25°C		7.5		pF
COM ON capacitance	$C_{COM(ON)}$	f = 1 MHz, See Figure 4	25°C		17		pF
Digital input capacitance	C_I	V_{IN} = V_+, 0 V	25°C		1.5		pF
Bandwidth	BW	R_L = 50 Ω, C_L = 15 pF, V_{NO} = 1 V_{RMS}, f = 100 kHz	25°C		460		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, C_L = 15 pF, V_{NO} = 1 V_{RMS}, f = 100 kHz	25°C		–94		dB
Total harmonic distortion	THD	R_L = 50 Ω, C_L = 15 pF, V_{NO} = 1 V_{RMS}, f = 100 kHz	25°C		0.15		%
Supply							
V_+ supply current	I_+	V_{IN} = 0 V or V_+	25°C			0.03	µA
			Full			0.05	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(2) Typical values are at T_A = 25°C.
(3) Leakage parameters are 100% tested at maximum-rated hot operating temperature, and are ensured by correlation at 25°C.
(4) Specified by design, not production tested

PIN DESCRIPTION[1]

PIN NO.				NAME	DESCRIPTION
TS12A4514		TS12A4515			
D, P	SOT-23	D, P	SOT-23		
1	1	1	1	COM	Common
2, 3, 5	–	2, 3, 5	–	N.C.	No connect (not internally connected)
4	5	4	5	V+	Power supply
6	4	6	4	IN	Digital control to connect COM to NO or NC
7	3	7	3	GND	Digital ground
8	2	–	–	NO	Normally open
–	–	8	2	NC	Normally closed

(1) NO, NC, and COM pins are identical and interchangeable. Any may be considered as an input or an output; signals pass in both directions.

Product Folder Link(s): *TS12A4514 TS12A4515*

APPLICATION INFORMATION

Power-Supply Considerations

The TS12A4514/TS12A4515 construction is typical of most CMOS analog switches, except that they have only two supply pins: V_+ and GND. V_+ and GND drive the internal CMOS switches and set their analog voltage limits. Reverse ESD-protection diodes are internally connected between each analog-signal pin and both V_+ and GND. One of these diodes conducts if any analog signal exceeds V_+ or GND.

Virtually all the analog leakage current comes from the ESD diodes to V_+ or GND. Although the ESD diodes on a given signal pin are identical and, therefore, fairly well balanced, they are reverse biased differently. Each is biased by either V_+ or GND and the analog signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the V_+ and GND pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity.

There is no connection between the analog-signal paths and V_+ or GND.

V_+ and GND also power the internal logic and logic-level translators. The logic-level translators convert the logic levels to switched V_+ and GND signals to drive the analog signal gates.

Logic-Level Thresholds

The logic-level thresholds are CMOS/TTL compatible when V_+ is 5 V. As V_+ is raised, the level threshold increases slightly. When V_+ reaches 12 V, the level threshold is about 3 V – above the TTL-specified high-level minimum of 2.8 V, but still compatible with CMOS outputs.

CAUTION:

If the user is using the TS12A4514 or TS12A4515 with a V+ supply of 3 V, then the control input (IN) voltage should not exceed V+, otherwise the output levels can exceed 3 V and violate the absolute maximum rating, potentially damaging the device.

High-Frequency Performance

In 50-Ω systems, signal response is reasonably flat up to 250 MHz (see *Typical Operating Characteristics*). Above 20 MHz, the on response has several minor peaks that are highly layout dependent. The problem is not in turning the switch on; it is turning it off. The OFF-state switch acts like a capacitor and passes higher frequencies with less attenuation. At 10 MHz, OFF isolation is about –45 dB in 50-Ω systems, decreasing (approximately 20 dB per decade) as frequency increases. Higher circuit impedances also make OFF isolation decrease. OFF isolation is about 3 dB above that of a bare IC socket, and is due entirely to capacitive coupling.
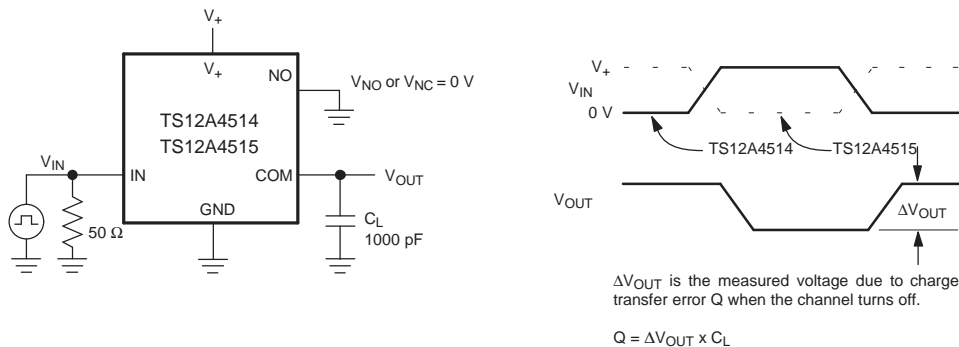
Test Circuits/Timing Diagrams

ΔV_{OUT} is the measured voltage due to charge transfer error Q when the channel turns off.

$$Q = \Delta V_{OUT} \times C_L$$

Figure 1. Charge Injection

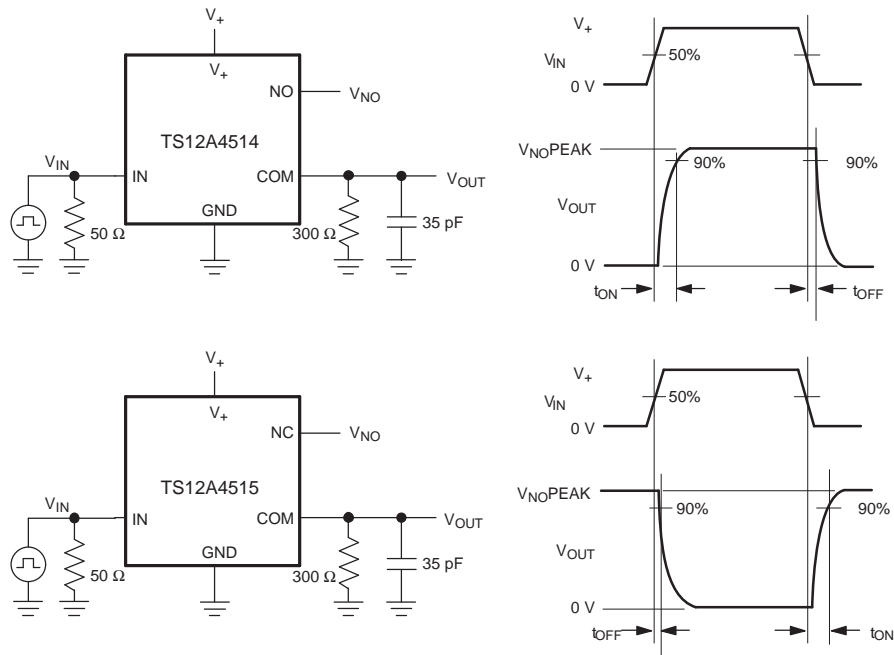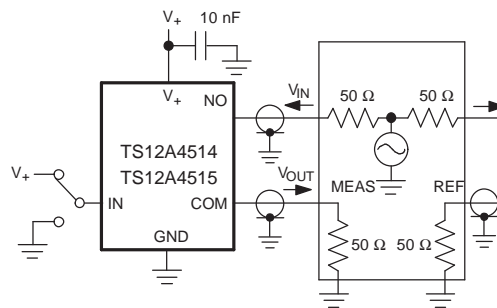Product Folder Link(s): *TS12A4514 TS12A4515*

Figure 2. Switching Times

Measurements are standardized against short at socket terminals. OFF isolation is measured between COM and OFF terminals on each switch. ON loss is measured between COM and ON terminals on each switch. Signal direction through switch is reversed; worst values are recorded.

$$\text{OFF Isolation} = 20\log \frac{V_{OUT}}{V_{IN}}$$

$$\text{ON Loss} = 20\log \frac{V_{OUT}}{V_{IN}}$$

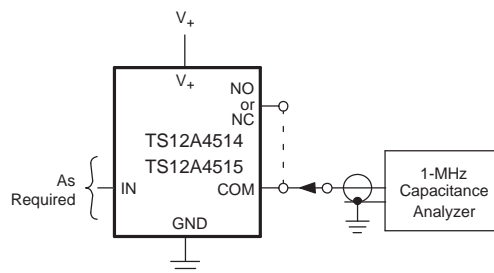**Figure 3. OFF Isolation and ON Loss**

Figure 4. NO, NC, and COM Capacitance

Product Folder Link(s): *TS12A4514 TS12A4515*

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS12A4514D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YD514	Samples
TS12A4514DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	9CJE	Samples
TS12A4514DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YD514	Samples
TS12A4514DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YD514	Samples
TS12A4514DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YD514	Samples
TS12A4514P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TS12A4514P	Samples
TS12A4514PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TS12A4514P	Samples
TS12A4515D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YD515	Samples
TS12A4515DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	9CKE	Samples
TS12A4515DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YD515	Samples
TS12A4515DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YD515	Samples
TS12A4515DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YD515	Samples
TS12A4515P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TS12A4515P	Samples
TS12A4515PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TS12A4515P	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS12A4514DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TS12A4514DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TS12A4515DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TS12A4515DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS12A4514DBVR	SOT-23	DBV	5	3000	203.0	203.0	35.0
TS12A4514DR	SOIC	D	8	2500	367.0	367.0	35.0
TS12A4515DBVR	SOT-23	DBV	5	3000	203.0	203.0	35.0
TS12A4515DR	SOIC	D	8	2500	367.0	367.0	35.0
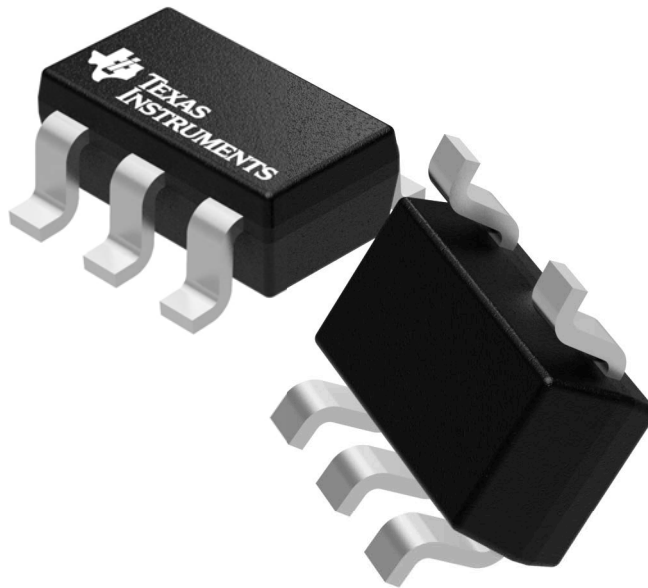
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4073253/P

$\dfrac{3.0}{2.6}$

$\dfrac{1.75}{1.45}$

B

A

PIN 1
INDEX AREA

1

5

2X [0.95]

1.9

3.05
2.75

2

1.9

3

5X $\dfrac{0.5}{0.3}$

$\oplus$ [0.2 Ⓜ] [C] [A] [B]

4

C

[△] [0.1 C]

1.45 MAX

(1.1)

$\dfrac{0.15}{0.00}$ TYP

0.25

GAGE PLANE

$\dfrac{0.22}{0.08}$ TYP

$\dfrac{8°}{0°}$ TYP

$\dfrac{0.6}{0.3}$ TYP

SEATING PLANE

4214839/C   04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.

PKG ℄

5X (1.1)

1

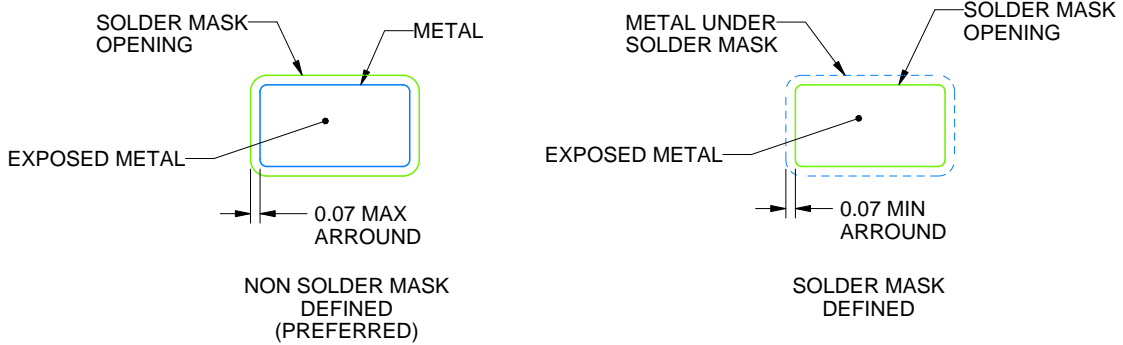5X (0.6)

5

SYMM ℄

2

(1.9)

2X (0.95)

3

4

(R0.05) TYP

(2.6)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.07 MAX
ARROUND

NON SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.07 MIN
ARROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214839/C 04/2017

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
7. Board assembly site may have different recommendations for stencil design.

D (R−PDSO−G8)   PLASTIC SMALL OUTLINE

0.197 (5,00)
0.189 (4,80)
C

8   5

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)
D

Pin 1
Index Area

1   4

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) M

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

Gauge Plane

0.004 (0,10)

Seating Plane

0.010 (0,25)

0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−3/M   06/11

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
              not exceed 0.006 (0,15) each side.
         D.   Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
         E.   Reference JEDEC MS−012 variation AA.

TEXAS
INSTRUMENTS
www.ti.com

D (R−PDSO−G8)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

6x1,27

8x0,55

6x1,27

8x1,50

5,40

5,40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,60

1,55

Example
Solder Mask Opening
(See Note E)

0,07

All Around

4211283−2/E   08/12

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Publication IPC−7351 is recommended for alternate designs.
         D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
             contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
         E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R-PDIP-T8)   PLASTIC DUAL-IN-LINE PACKAGE

0.400 (10,16)
0.355 (9,02)

8   5

0.260 (6,60)
0.240 (6,10)

1   4

0.070 (1,78)
0.045 (1,14)

0.045 (1,14)
0.030 (0,76)

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92)
MAX

4040082/E 04/2010

NOTES: A.   All linear dimensions are in inches (millimeters).
          B.   This drawing is subject to change without notice.
          C.   Falls within JEDEC MS-001 variation BA.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.