

## SINGLE 5-Ω SP3T ANALOG SWITCH 5-V/3.3-V 3:1 MULTIPLEXER/DEMULTIPLEXER

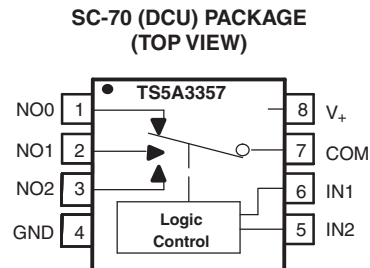
Check for Samples: [TS5A3357-Q1](#)

### FEATURES

- Qualified for Automotive Applications
- Specified Break-Before-Make Switching
- Low ON-State Resistance
- High Bandwidth
- Control Inputs Are 5.5-V Tolerant
- Low Charge Injection
- Excellent ON-State Resistance Matching
- Low Total Harmonic Distortion (THD)
- 1.65-V to 5.5-V Single-Supply Operation
- Latch Up Exceeds 100 mA per JESD78B, Class I

### DESCRIPTION/ORDERING INFORMATION

The TS5A3357 is a high-performance, single-pole triple throw (SP3T) analog switch that is designed to operate from 1.65 V to 5.5 V. The device offers a low ON-state resistance and low input/output capacitance and, thus, causes a very low signal distortion. The break-before-make feature allows transferring of a signal from one port to another, with a minimal signal distortion. This device also offers a low charge injection which makes this device suitable for high-performance audio and data acquisition systems.



**Table 1. Summary of Characteristics<sup>(1)</sup>**

Configuration	Triple 3:1 Multiplexer/ Demultiplexer (1 × SP3T)
Number of channels	1
ON-state resistance ( $r_{on}$ )	5 Ω
ON-state resistance match ( $\Delta r_{on}$ )	0.1 Ω
ON-state resistance flatness ( $r_{on(Flat)}$ )	6.5 Ω
Turn-on/turn-off time ( $t_{ON}/t_{OFF}$ )	6.5 ns/3.7 ns
Break-before-make time ( $t_{BBM}$ ) <sup>(2)</sup>	0.5 ns
Charge injection ( $Q_C$ )	3.4 pC
Bandwidth (BW)	334 MHz
OFF isolation ( $O_{ISO}$ )	-82 dB at 10 MHz
Crosstalk ( $X_{TALK}$ )	-62 dB at 10 MHz
Total harmonic distortion (THD)	0.05%
Leakage current ( $I_{COM(OFF)}$ )	±1 μA
Package option	8-pin DCU (US8)

(1)  $V_+ = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

(2) Specified by designed. Not production tested.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**Table 2. FUNCTION TABLE**

IN1	IN2	COM TO NO0	COM TO NO1	COM TO NO2
L	L	OFF	OFF	OFF
H	L	ON	OFF	OFF
L	H	OFF	ON	OFF
H	H	OFF	OFF	ON

**Table 3. ORDERING INFORMATION<sup>(1)</sup>**

T <sub>A</sub>	PACKAGE <sup>(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	SOT – DCU	Reel of 3000	TS5A3357QDCURQ1	JAVR

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).
- (2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

**ABSOLUTE MINIMUM AND MAXIMUM RATINGS<sup>(1) (2)</sup>**

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>+</sub>	Supply voltage range <sup>(3)</sup>	-0.5	6.5	V
V <sub>NO</sub> V <sub>COM</sub>	Analog voltage range <sup>(3) (4) (5)</sup>	-0.5	V <sub>+</sub> + 0.5	V
I <sub>K</sub>	Analog port diode current	V <sub>NO</sub> , V <sub>COM</sub> < 0 or V <sub>NO</sub> , V <sub>COM</sub> > V <sub>+</sub>		mA
I <sub>NO</sub> I <sub>COM</sub>	On-state switch current	V <sub>NO</sub> , V <sub>COM</sub> = 0 to V <sub>+</sub>		mA
V <sub>I</sub>	Digital input voltage range <sup>(3) (4)</sup>	-0.5	6.5	V
I <sub>IK</sub>	Digital input clamp current	V <sub>I</sub> < 0		mA
I <sub>+</sub>	Continuous current through V <sub>+</sub>		100	mA
I <sub>GND</sub>	Continuous current through GND	-100	100	mA
T <sub>stg</sub>	Storage temperature range	-65	150	°C

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
- (3) All voltages are with respect to ground, unless otherwise specified.
- (4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (5) This value is limited to 5.5 V maximum.

**PACKAGE THERMAL IMPEDANCE**

		MAX	UNIT
θ <sub>JA</sub>	Package thermal impedance <sup>(1)</sup>	165	°C/W

- (1) The package thermal impedance is calculated in accordance with JESD 51-7.

**ELECTRICAL CHARACTERISTICS FOR 5-V SUPPLY<sup>(1)</sup>**
 $V_+ = 4.5\text{ V to }5.5\text{ V}$ ,  $T_A = -40^\circ\text{C to }125^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Analog Switch</b>								
Analog signal range	$V_{COM}, V_{NO}$				0		$V_+$	V
Peak ON resistance	$r_{peak}$	$0 \leq V_{NO} \leq V_+$ , $I_{COM} = -30\text{ mA}$ , Switch ON, See <a href="#">Figure 13</a>	Full	4.5 V			15	$\Omega$
ON-state resistance	$r_{on}$	$V_{NO} = 0$ , $I_{COM} = 30\text{ mA}$	25°C	4.5 V		5	7	$\Omega$
			Full			7		
		$V_{NO} = 2.4\text{ V}$ , $I_{COM} = -30\text{ mA}$	25°C			6	12	
			Full				12	
			25°C			7	15	
Full			15					
ON-state resistance match between channels	$\Delta r_{on}$	$V_{NO} = 3.15\text{ V}$ , $I_{COM} = -30\text{ mA}$ , Switch ON, See <a href="#">Figure 13</a>	25°C	4.5 V		0.1		$\Omega$
ON-state resistance flatness	$r_{on(Flat)}$	$0 \leq V_{NO} \leq V_+$ , $I_{COM} = -30\text{ mA}$ , Switch ON, See <a href="#">Figure 13</a>	25°C	5 V		6.5		$\Omega$
NO OFF leakage current	$I_{NO(OFF)}$	$V_{NO} = 0\text{ to }V_+$ , $V_{COM} = V_+\text{ to }0$ , Switch OFF, See <a href="#">Figure 14</a>	25°C	5.5 V	-0.2		0.2	$\mu\text{A}$
			Full		-1	1		
COM OFF leakage current	$I_{COM(OFF)}$	$V_{COM} = 0\text{ to }V_+$ , $V_{NO} = V_+\text{ to }0$ , Switch OFF, See <a href="#">Figure 14</a>	25°C	0	-0.2		0.2	$\mu\text{A}$
			Full		-1	1		
NO ON leakage current	$I_{NO(ON)}$	$V_{NO} = 0\text{ to }V_+$ , $V_{COM} = \text{Open}$ , Switch ON, See <a href="#">Figure 14</a>	25°C	5.5 V	-0.2		0.2	$\mu\text{A}$
			Full		-1	1		
COM ON leakage current	$I_{COM(ON)}$	$V_{NO} = \text{Open}$ , $V_{COM} = 0\text{ to }V_+$ , Switch ON, See <a href="#">Figure 14</a>	25°C	5.5 V	-0.2		0.2	$\mu\text{A}$
			Full		-1	1		
<b>Digital Control Inputs (IN1, IN2)<sup>(2)</sup></b>								
Input logic high	$V_{IH}$		Full		$V_+ \times 0.7$		5.5	V
Input logic low	$V_{IL}$		Full		0		$V_+ \times 0.3$	V
Input leakage current	$I_{IH}, I_{IL}$	$V_I = 5.5\text{ V or }0$	25°C	5.5 V			0.1	$\mu\text{A}$
			Full			1		

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at  $V_+$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**ELECTRICAL CHARACTERISTICS FOR 5-V SUPPLY <sup>(1)</sup> (continued)**
 $V_+ = 4.5\text{ V to }5.5\text{ V}$ ,  $T_A = -40^\circ\text{C to }125^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Dynamic</b>								
Turn-on time	$t_{ON}$	$V_{NO} = V_+$ or GND, $R_L = 500\ \Omega$ , See <a href="#">Figure 16</a>	25°C	5 V	1.5		10	ns
			Full	4.5 V to 5.5 V	1.5		10	
Turn-off time	$t_{OFF}$	$V_{NO} = V_+$ or GND, $R_L = 500\ \Omega$ , See <a href="#">Figure 16</a>	25°C	5 V	0.8		6.5	ns
			Full	4.5 V to 5.5 V	0.8		7	
Break-before-make time <sup>(3)</sup>	$t_{BBM}$	$V_{NO} = V_+$ , $R_L = 50\ \Omega$ , See <a href="#">Figure 17</a>	25°C	5 V	0.5			ns
			Full	4.5 V to 5.5 V	0.5			
Charge injection	$Q_C$	$V_{GEN} = 0$ , $C_L = 0.1\text{ nF}$ , See <a href="#">Figure 21</a>	25°C	5 V		3.4		pC
NO OFF capacitance	$C_{NO(OFF)}$	$V_{NO} = V_+$ or GND, Switch OFF, See <a href="#">Figure 15</a>	25°C	5 V		4.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	$V_{NO} = V_+$ or GND, Switch OFF, See <a href="#">Figure 15</a>	25°C	5 V		10.5		pF
NO ON capacitance	$C_{NO(ON)}$	$V_{NO} = V_+$ or GND, Switch ON, See <a href="#">Figure 15</a>	25°C	5 V		17		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON, See <a href="#">Figure 15</a>	25°C	5 V		17		pF
Digital input capacitance	$C_I$	$V_I = V_+$ or GND, See <a href="#">Figure 15</a>	25°C	5 V		3		pF
Bandwidth	BW	$R_L = 50\ \Omega$ , Switch ON, See <a href="#">Figure 18</a>	25°C	4.5 V to 5.5 V		334		MHz
OFF isolation	$O_{ISO}$	$R_L = 50\ \Omega$ , $f = 10\text{ MHz}$ , Switch OFF, See <a href="#">Figure 19</a>	25°C	4.5 V to 5.5 V		-82		dB
Crosstalk	$X_{TALK}$	$R_L = 50\ \Omega$ , $f = 10\text{ MHz}$ , Switch ON, See <a href="#">Figure 20</a>	25°C	4.5 V to 5.5 V		-62		dB
<b>Supply</b>								
Positive supply current	$I_+$	$V_I = V_+$ or GND, Switch ON or OFF	25°C	5.5 V			1	$\mu\text{A}$
			Full				10	

(3) Specified by designed. Not production tested.

**ELECTRICAL CHARACTERISTICS FOR 3.3-V SUPPLY<sup>(1)</sup>**
 $V_+ = 3\text{ V to }3.6\text{ V}$ ,  $T_A = -40^\circ\text{C to }125^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT	
<b>Analog Switch</b>									
Analog signal range	$V_{COM}, V_{NO}$				0		$V_+$	V	
Peak ON resistance	$r_{peak}$	$0 \leq V_{NO} \leq V_+$ , $I_{COM} = -24\text{ mA}$ , Switch ON, See <a href="#">Figure 13</a>	Full	3 V			25	$\Omega$	
ON-state resistance	$r_{on}$	$V_{NO} = 0\text{ V}$ , $I_{COM} = 24\text{ mA}$ Switch ON, See <a href="#">Figure 13</a>	25°C	3 V			6.5	9	$\Omega$
			Full				9		
			25°C				9	20	
			Full				20		
ON-state resistance match between channels	$\Delta r_{on}$	$V_{NO} = 2.1\text{ V}$ , $I_{COM} = -24\text{ mA}$ , Switch ON, See <a href="#">Figure 13</a>	25°C	3 V		0.1		$\Omega$	
ON-state resistance flatness	$r_{on(Flat)}$	$0 \leq V_{NO} \leq V_+$ , $I_{COM} = -24\text{ mA}$ , Switch ON, See <a href="#">Figure 13</a>	25°C	3.3 V		13.5		$\Omega$	
NO OFF leakage current	$I_{NO(OFF)}$	$V_{NO} = 0\text{ to }V_+$ , $V_{COM} = V_+\text{ to }0$ , Switch OFF, See <a href="#">Figure 14</a>	25°C	3.6 V			-0.2	0.2	$\mu\text{A}$
			Full				-1	1	
COM OFF leakage current	$I_{COM(OFF)}$	$V_{COM} = 0\text{ to }V_+$ , $V_{NO} = V_+\text{ to }0$ , Switch OFF, See <a href="#">Figure 14</a>	25°C	3.6 V			-0.2	0.2	$\mu\text{A}$
			Full				-1	1	
NO ON leakage current	$I_{NO(ON)}$	$V_{NO} = 0\text{ to }V_+$ , $V_{COM} = V_+\text{ to }0$ , Switch ON, See <a href="#">Figure 14</a>	25°C	3.6 V			-0.2	0.2	$\mu\text{A}$
			Full				-1	1	
COM ON leakage current	$I_{COM(ON)}$	$V_{NO} = \text{Open}$ , $V_{COM} = 0\text{ to }V_+$ , Switch ON, See <a href="#">Figure 14</a>	25°C	3.6 V			-0.2	0.2	$\mu\text{A}$
			Full				-1	1	
<b>Digital Control Inputs (IN1, IN2)<sup>(2)</sup></b>									
Input logic high	$V_{IH}$		Full				$V_+ \times 0.7$	5.5	V
Input logic low	$V_{IL}$		Full			0		$V_+ \times 0.3$	V
Input leakage current	$I_{IH}, I_{IL}$	$V_I = 5.5\text{ V or }0$	25°C	3.6 V			-1	0.1	$\mu\text{A}$
			Full					1	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at  $V_+$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**ELECTRICAL CHARACTERISTICS FOR 3.3-V SUPPLY <sup>(1)</sup> (continued)**
 $V_+ = 3\text{ V to }3.6\text{ V}$ ,  $T_A = -40^\circ\text{C to }125^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Dynamic</b>								
Turn-on time	$t_{ON}$	$V_{NO} = V_+$ or GND, $R_L = 500\ \Omega$ , $C_L = 50\text{ pF}$ , See <a href="#">Figure 16</a>	25°C	3.3 V	2		12	ns
			Full	3 V to 3.6 V	2		12.9	
Turn-off time	$t_{OFF}$	$V_{NO} = V_+$ or GND, $R_L = 500\ \Omega$ , $C_L = 50\text{ pF}$ , See <a href="#">Figure 16</a>	25°C	3.3 V	1.3		8	ns
			Full	3 V to 3.6 V	1.5		8	
Break-before-make time <sup>(3)</sup>	$t_{BBM}$	$V_{NO} = V_+$ , $R_L = 50\ \Omega$ , $C_L = 50\text{ pF}$ , See <a href="#">Figure 17</a>	25°C	3.3 V	0.5			ns
			Full	3 V to 3.6 V	0.5			
Charge injection	$Q_C$	$V_{GEN} = 0$ , $C_L = 0.1\text{ nF}$ , See <a href="#">Figure 21</a>	25°C	3.3 V		1.75		pC
NO OFF capacitance	$C_{NO(OFF)}$	$V_{NO} = V_+$ or GND, Switch OFF, See <a href="#">Figure 15</a>	25°C	3.3 V		4.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	$V_{NO} = V_+$ or GND, Switch OFF, See <a href="#">Figure 15</a>	25°C	3.3 V		10.5		pF
NO ON capacitance	$C_{NO(ON)}$	$V_{NO} = V_+$ or GND, Switch ON, See <a href="#">Figure 15</a>	25°C	3.3 V		17		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON, See <a href="#">Figure 15</a>	25°C	3.3 V		17		pF
Digital input capacitance	$C_I$	$V_I = V_+$ or GND, See <a href="#">Figure 15</a>	25°C	3.3 V		3		pF
Bandwidth	BW	$R_L = 50\ \Omega$ , Switch ON, See <a href="#">Figure 18</a>	25°C	3 V to 3.6 V		327		MHz
OFF isolation	$O_{ISO}$	$R_L = 50\ \Omega$ , $f = 10\text{ MHz}$ , Switch OFF, See <a href="#">Figure 19</a>	25°C	3 V to 3.6 V		-82		dB
Crosstalk	$X_{TALK}$	$R_L = 50\ \Omega$ , $f = 10\text{ MHz}$ , Switch ON, See <a href="#">Figure 20</a>	25°C	3 V to 3.6 V		-62		dB
<b>Supply</b>								
Positive supply current	$I_+$	$V_I = V_+$ or GND, Switch ON or OFF	25°C	3.6 V			1	$\mu\text{A}$
			Full				10	

(3) Specified by designed. Not production tested.

**ELECTRICAL CHARACTERISTICS FOR 2.5-V SUPPLY<sup>(1)</sup>**
 $V_+ = 2.3 \text{ V to } 2.7 \text{ V}$ ,  $T_A = -40^\circ\text{C to } 125^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Analog Switch</b>								
Analog signal range	$V_{COM}, V_{NO}$				0		$V_+$	V
Peak ON resistance	$r_{peak}$	$0 \leq V_{NO} \leq V_+$ , $I_{COM} = -8 \text{ mA}$ , Switch ON, See <a href="#">Figure 13</a>	Full	2.3 V			50	$\Omega$
ON-state resistance	$r_{on}$	$V_{NO} = 0 \text{ V}$ , $I_{COM} = 8 \text{ mA}$ $V_{NO} = 2.3 \text{ V}$ , $I_{COM} = -8 \text{ mA}$ Switch ON, See <a href="#">Figure 13</a>	25°C	2.3 V		8	12	$\Omega$
			Full			12		
			25°C			11	30	
			Full			30		
ON-state resistance match between channels	$\Delta r_{on}$	$V_{NO} = 1.8 \text{ V}$ , $I_{COM} = -8 \text{ mA}$ , Switch ON, See <a href="#">Figure 13</a>	25°C	2.3 V		0.3		$\Omega$
ON-state resistance flatness	$r_{on(Flat)}$	$0 \leq V_{NO} \leq V_+$ , $I_{COM} = -8 \text{ mA}$ , Switch ON, See <a href="#">Figure 13</a>	25°C	2.5 V		39		$\Omega$
NO OFF leakage current	$I_{NO(OFF)}$	$V_{NO} = 0 \text{ to } V_+$ , $V_{COM} = V_+ \text{ to } 0$ , Switch OFF, See <a href="#">Figure 14</a>	25°C	2.7 V	-0.2		0.2	$\mu\text{A}$
			Full		-1	1		
COM OFF leakage current	$I_{COM(OFF)}$	$V_{COM} = 0 \text{ to } V_+$ , $V_{NO} = V_+ \text{ to } 0$ , Switch OFF, See <a href="#">Figure 14</a>	25°C	2.7 V	-0.2		0.2	$\mu\text{A}$
			Full		-1	1		
NO ON leakage current	$I_{NO(ON)}$	$V_{NO} = 0 \text{ to } V_+$ , $V_{COM} = V_+ \text{ to } 0$ , Switch ON, See <a href="#">Figure 14</a>	25°C	2.7 V	-0.2		0.2	$\mu\text{A}$
			Full		-1	1		
COM ON leakage current	$I_{COM(ON)}$	$V_{NO} = \text{Open}$ , $V_{COM} = 0 \text{ to } V_+$ , Switch ON, See <a href="#">Figure 14</a>	25°C	2.7 V	-0.2		0.2	$\mu\text{A}$
			Full		-1	1		
<b>Digital Control Inputs (IN1, IN2)<sup>(2)</sup></b>								
Input logic high	$V_{IH}$		Full		$V_+ \times 0.75$		5.5	V
Input logic low	$V_{IL}$		Full		0		$V_+ \times 0.25$	V
Input leakage current	$I_{IH}, I_{IL}$	$V_I = 5.5 \text{ V or } 0$	25°C	2.7 V			0.1	$\mu\text{A}$
			Full			1		

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at  $V_+$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**ELECTRICAL CHARACTERISTICS FOR 2.5-V SUPPLY <sup>(1)</sup> (continued)**
 $V_+ = 2.3 \text{ V to } 2.7 \text{ V}$ ,  $T_A = -40^\circ\text{C to } 125^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Dynamic</b>								
Turn-on time	$t_{ON}$	$V_{NO} = V_+$ or GND, $R_L = 500 \Omega$ ,	$C_L = 50 \text{ pF}$ , See <a href="#">Figure 16</a>	25°C	2.5 V	3	15	ns
				Full	2.3 V to 2.7 V	3	19.4	
Turn-off time	$t_{OFF}$	$V_{NO} = V_+$ or GND, $R_L = 500 \Omega$ ,	$C_L = 50 \text{ pF}$ , See <a href="#">Figure 16</a>	25°C	2.5 V	2	8.1	ns
				Full	2.3 V to 2.7 V	2	10	
Break-before-make time <sup>(3)</sup>	$t_{BBM}$	$V_{NO} = V_+$ , $R_L = 50 \Omega$ ,	$C_L = 50 \text{ pF}$ , See <a href="#">Figure 17</a>	25°C	2.5 V	0.5		ns
				Full	2.3 V to 2.7 V	0.5		
Charge injection	$Q_C$	$V_{GEN} = 0$ , $C_L = 0.1 \text{ nF}$ ,	See <a href="#">Figure 21</a>	25°C	2.5 V	1.15		pC
NO OFF capacitance	$C_{NO(OFF)}$	$V_{NO} = V_+$ or GND, Switch OFF,	See <a href="#">Figure 15</a>	25°C	2.5 V	4.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	$V_{NO} = V_+$ or GND, Switch OFF,	See <a href="#">Figure 15</a>	25°C	2.5 V	10.5		pF
NO ON capacitance	$C_{NO(ON)}$	$V_{NO} = V_+$ or GND, Switch ON,	See <a href="#">Figure 15</a>	25°C	2.5 V	17		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON,	See <a href="#">Figure 15</a>	25°C	2.5 V	17		pF
Digital input capacitance	$C_I$	$V_I = V_+$ or GND,	See <a href="#">Figure 15</a>	25°C	2.5 V	3		pF
Bandwidth	BW	$R_L = 50 \Omega$ , Switch ON,	See <a href="#">Figure 18</a>	25°C	2.3 V to 2.7 V	320		MHz
OFF isolation	$O_{ISO}$	$R_L = 50 \Omega$ , $f = 10 \text{ MHz}$ ,	Switch OFF, See <a href="#">Figure 19</a>	25°C	2.3 V to 2.7 V	-81		dB
Crosstalk	$X_{TALK}$	$R_L = 50 \Omega$ , $f = 10 \text{ MHz}$ ,	Switch ON, See <a href="#">Figure 20</a>	25°C	2.3 V to 2.7 V	-61		dB
<b>Supply</b>								
Positive supply current	$I_+$	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	2.7 V		1	$\mu\text{A}$
				Full			10	

(3) Specified by design. Not production tested.



**ELECTRICAL CHARACTERISTICS FOR 1.8-V SUPPLY<sup>(1)</sup>**
 $V_+ = 1.65\text{ V to }1.95\text{ V}$ ,  $T_A = -40^\circ\text{C to }125^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT	
<b>Analog Switch</b>									
Analog signal range	$V_{COM}, V_{NO}$				0		$V_+$	V	
Peak ON resistance	$r_{peak}$	$0 \leq V_{NO} \leq V_+$ , $I_{COM} = -4\text{ mA}$ , Switch ON, See <a href="#">Figure 13</a>	Full	1.65 V			150	$\Omega$	
ON-state resistance	$r_{on}$	$V_{NO} = 0\text{ V}$ , $I_{COM} = 4\text{ mA}$  $V_{NO} = 1.8\text{ V}$ , $I_{COM} = -4\text{ mA}$	Switch ON, See <a href="#">Figure 13</a>	25°C	1.65 V		10	20	$\Omega$
				Full			20		
				25°C			17	50	
				Full			50		
ON-state resistance match between channels	$\Delta r_{on}$	$V_{NO} = 1.15\text{ V}$ , $I_{COM} = -4\text{ mA}$ , Switch ON, See <a href="#">Figure 13</a>	25°C	1.65 V		0.3		$\Omega$	
ON-state resistance flatness	$r_{on(flat)}$	$0 \leq V_{NO} \leq V_+$ , $I_{COM} = -4\text{ mA}$ , Switch ON, See <a href="#">Figure 13</a>	25°C	1.8 V		140		$\Omega$	
NO OFF leakage current	$I_{NO(OFF)}$	$V_{NO} = 0\text{ to }V_+$ , $V_{COM} = V_+ \text{ to } 0$ , Switch OFF, See <a href="#">Figure 14</a>	25°C	1.95 V	-0.2		0.2	$\mu\text{A}$	
			Full		-1	1			
COM OFF leakage current	$I_{COM(OFF)}$	$V_{COM} = 0\text{ to }V_+$ , $V_{NO} = V_+ \text{ to } 0$ , Switch OFF, See <a href="#">Figure 14</a>	25°C	1.95 V	-0.2		0.2	$\mu\text{A}$	
			Full		-1	1			
NO ON leakage current	$I_{NO(ON)}$	$V_{NO} = 0\text{ to }V_+$ , $V_{COM} = V_+ \text{ to } 0$ , Switch ON, See <a href="#">Figure 14</a>	25°C	1.95 V	-0.2		0.2	$\mu\text{A}$	
			Full		-1	1			
COM ON leakage current	$I_{COM(ON)}$	$V_{NO} = \text{Open}$ , $V_{COM} = 0\text{ to }V_+$ , Switch ON, See <a href="#">Figure 14</a>	25°C	1.95 V	-0.2		0.2	$\mu\text{A}$	
			Full		-1	1			
<b>Digital Control Inputs (IN1, IN2)<sup>(2)</sup></b>									
Input logic high	$V_{IH}$		Full		$V_+ \times 0.75$		5.5	V	
Input logic low	$V_{IL}$		Full		0		$V_+ \times 0.25$	V	
Input leakage current	$I_{IH}, I_{IL}$	$V_I = 5.5\text{ V or } 0$	25°C	1.95 V			0.1	$\mu\text{A}$	
			Full			1			

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at  $V_+$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**ELECTRICAL CHARACTERISTICS FOR 1.8-V SUPPLY <sup>(1)</sup> (continued)**
 $V_+ = 1.65\text{ V to }1.95\text{ V}$ ,  $T_A = -40^\circ\text{C to }125^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Dynamic</b>								
Turn-on time	$t_{ON}$	$V_{NO} = V_+$ or GND, $R_L = 500\ \Omega$ , $C_L = 50\text{ pF}$ , See <a href="#">Figure 16</a>	25°C	1.8 V	5		32	ns
			Full	1.65 V to 1.95 V	5		40	
Turn-off time	$t_{OFF}$	$V_{NO} = V_+$ or GND, $R_L = 500\ \Omega$ , $C_L = 50\text{ pF}$ , See <a href="#">Figure 16</a>	25°C	1.8 V	3		14	ns
			Full	1.65 V to 1.95 V	3		17.6	
Break-before-make time <sup>(3)</sup>	$t_{BBM}$	$V_{NO} = V_+$ , $R_L = 50\ \Omega$ , $C_L = 50\text{ pF}$ , See <a href="#">Figure 17</a>	25°C	1.8 V	0.5			ns
			Full	1.65 V to 1.95 V	0.5			
Charge injection	$Q_C$	$V_{GEN} = 0$ , $C_L = 0.1\text{ nF}$ , See <a href="#">Figure 21</a>	25°C	1.8 V		0.3		pC
NO OFF capacitance	$C_{NO(OFF)}$	$V_{NO} = V_+$ or GND, Switch OFF, See <a href="#">Figure 15</a>	25°C	1.8 V		4.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	$V_{NO} = V_+$ or GND, Switch OFF, See <a href="#">Figure 15</a>	25°C	1.8 V		10.5		pF
NO ON capacitance	$C_{NO(ON)}$	$V_{NO} = V_+$ or GND, Switch ON, See <a href="#">Figure 15</a>	25°C	1.8 V		17		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON, See <a href="#">Figure 15</a>	25°C	1.8 V		17		pF
Digital input capacitance	$C_I$	$V_I = V_+$ or GND, See <a href="#">Figure 15</a>	25°C	1.8 V		3		pF
Bandwidth	BW	$R_L = 50\ \Omega$ , Switch ON, See <a href="#">Figure 18</a>	25°C	1.65 V to 1.95 V		341		MHz
OFF isolation	$O_{ISO}$	$R_L = 50\ \Omega$ , $f = 10\text{ MHz}$ , Switch OFF, See <a href="#">Figure 19</a>	25°C	1.65 V to 1.95 V		-81		dB
Crosstalk	$X_{TALK}$	$R_L = 50\ \Omega$ , $f = 10\text{ MHz}$ , Switch ON, See <a href="#">Figure 20</a>	25°C	1.65 V to 1.95 V		-61		dB
<b>Supply</b>								
Positive supply current	$I_+$	$V_I = V_+$ or GND, Switch ON or OFF	25°C	1.95 V			1	$\mu\text{A}$
			Full				10	

(3) Specified by design. Not production tested.

TYPICAL PERFORMANCE

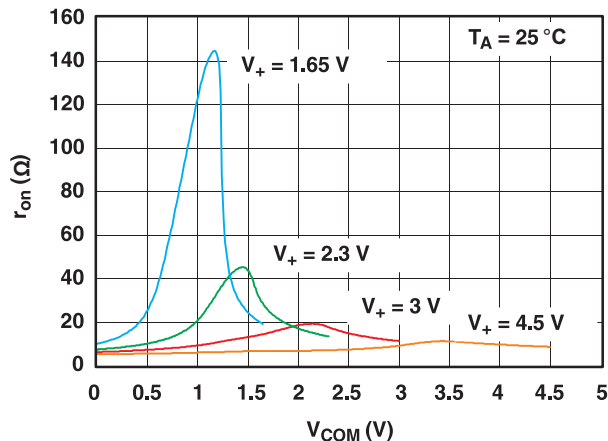


Figure 1.  $r_{on}$  vs  $V_{COM}$

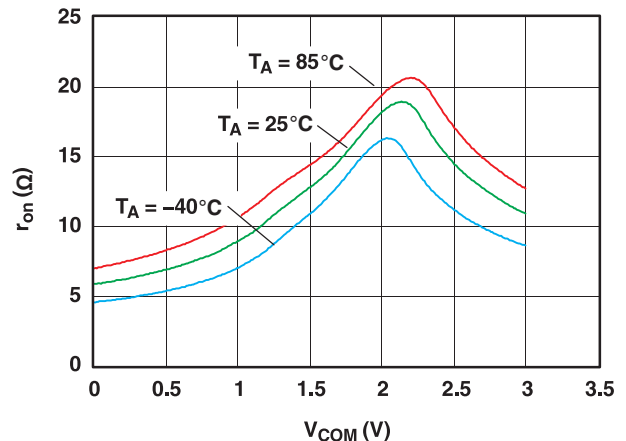


Figure 2.  $r_{on}$  vs  $V_{COM}$  ( $V_+ = 3\text{ V}$ )

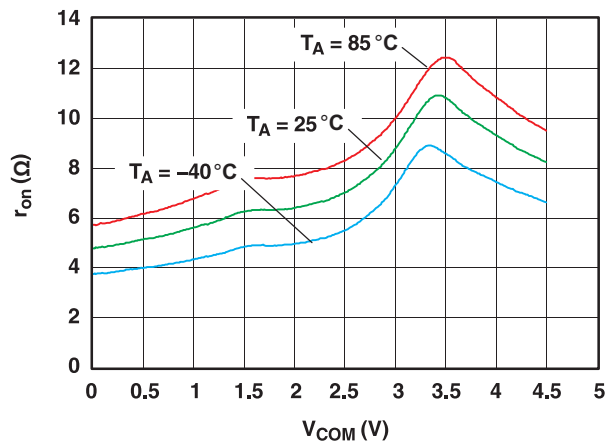


Figure 3.  $r_{on}$  vs  $V_{COM}$  ( $V_+ = 4.5\text{ V}$ )

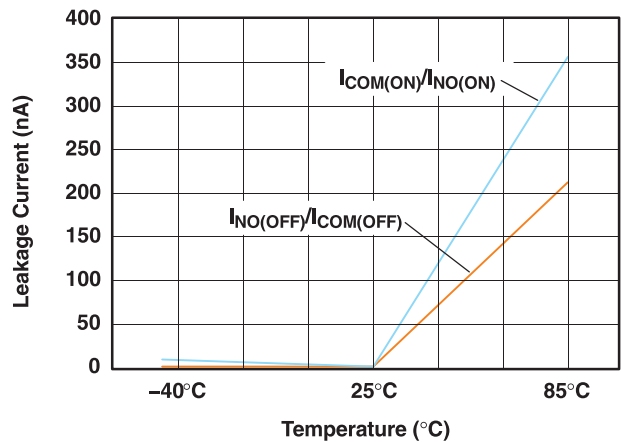


Figure 4. Leakage Current vs Temperature ( $V_+ = 5.5\text{ V}$ )

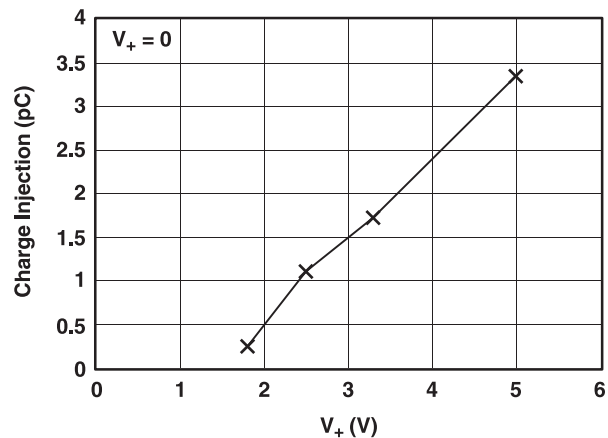


Figure 5. Charge Injection ( $Q_C$ ) vs  $V_{COM}$

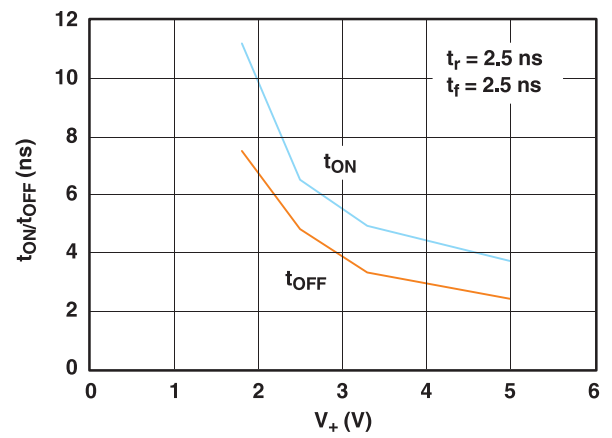


Figure 6.  $t_{ON}$  and  $t_{OFF}$  vs  $V_+$

TYPICAL PERFORMANCE (continued)

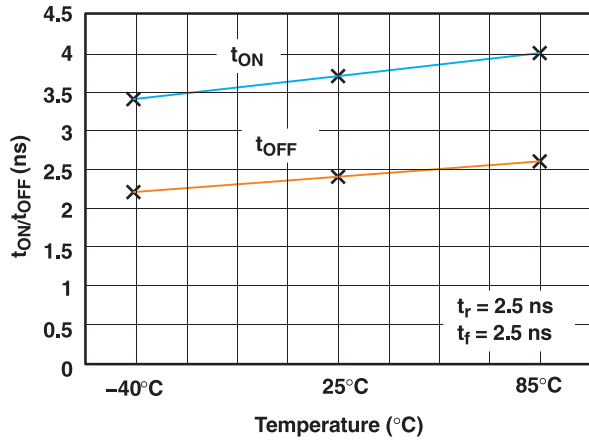


Figure 7. t<sub>ON</sub> and t<sub>OFF</sub> vs Temperature (V<sub>+</sub> = 5 V)

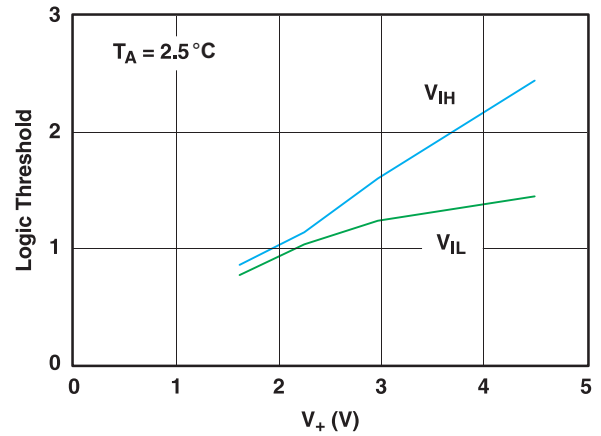


Figure 8. Logic-Level Threshold vs V<sub>+</sub>

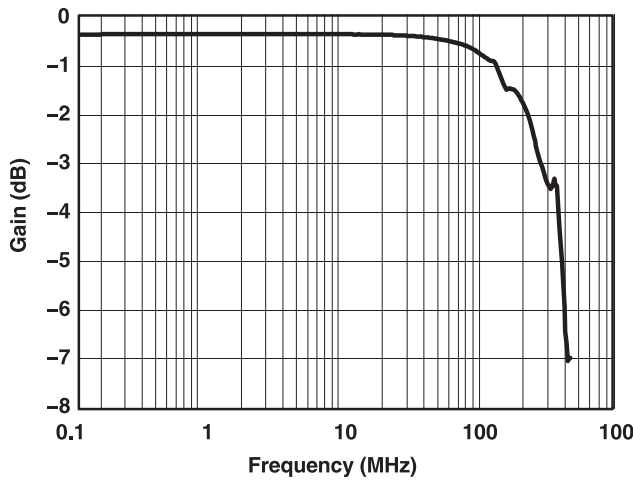


Figure 9. Frequency Response (V<sub>+</sub> = 3 V)

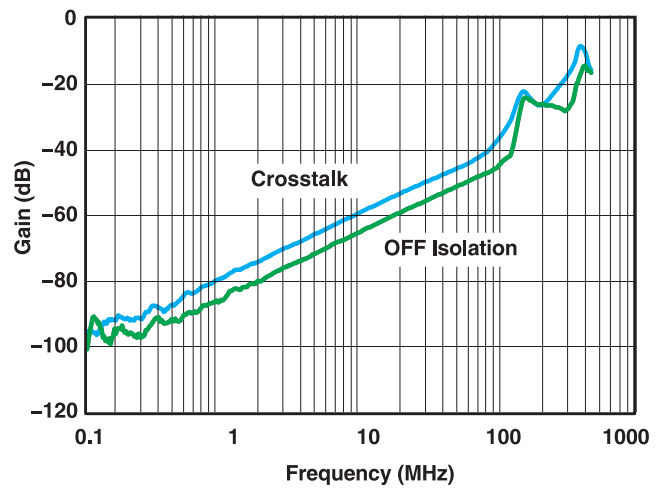


Figure 10. OFF Isolation and Crosstalk vs Frequency (V<sub>+</sub> = 3 V)

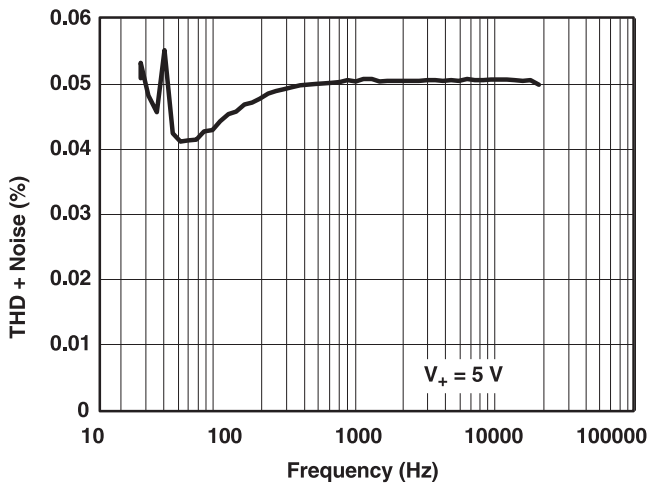


Figure 11. Total Harmonic Distortion vs Frequency (V<sub>+</sub> = 5 V)

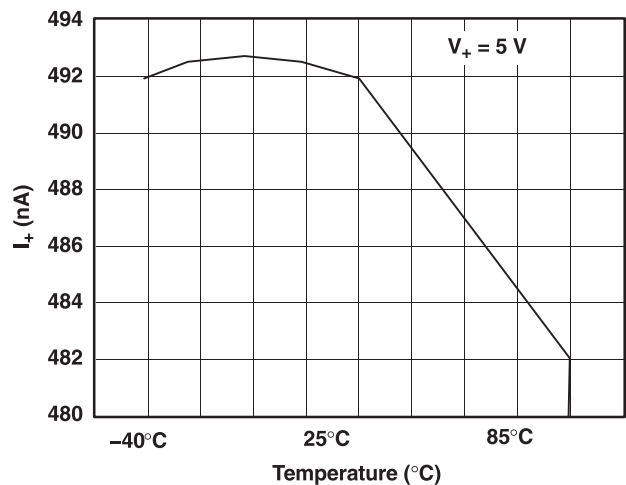


Figure 12. Power-Supply Current vs Temperature (V<sub>+</sub> = 5 V)

**Table 4. PIN DESCRIPTION**

PIN NO.	NAME	DESCRIPTION
1	NO0	Normally open
2	NO1	Normally open
3	NO2	Normally open
4	GND	Digital ground
5	IN2	Digital control to connect COM to NO
6	IN1	Digital control to connect COM to NO
7	COM	Common
8	V <sub>+</sub>	Power supply

**Table 5. PARAMETER DESCRIPTION**

SYMBOL	DESCRIPTION
V <sub>COM</sub>	Voltage at COM
V <sub>NO</sub>	Voltage at NO
r <sub>on</sub>	Resistance between COM and NC or COM and NO ports when the channel is ON
r <sub>peak</sub>	Peak on-state resistance over a specified voltage range
Δr <sub>on</sub>	Difference of r <sub>on</sub> between channels in a specific device
r <sub>on(flat)</sub>	Difference between the maximum and minimum value of r <sub>on</sub> in a channel over the specified range of conditions
I <sub>NO(OFF)</sub>	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state
I <sub>NO(ON)</sub>	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open
I <sub>COM(ON)</sub>	Leakage current measured at the COM port, with the corresponding channel (COM to NO or COM to NC) in the ON state and the output (NC or NO) open
I <sub>COM(OFF)</sub>	Leakage current measured at the COM port during the power-down condition, V <sub>+</sub> = 0
V <sub>IH</sub>	Minimum input voltage for logic high for the control input (IN)
V <sub>IL</sub>	Maximum input voltage for logic low for the control input (IN)
V <sub>i</sub>	Voltage at the control input (IN)
I <sub>IH</sub> , I <sub>IL</sub>	Leakage current measured at the control input (IN)
t <sub>ON</sub>	Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning ON.
t <sub>OFF</sub>	Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning OFF.
t <sub>BBM</sub>	Break-before-make time. This parameter is measured under the specified range of conditions and by the propagation delay between the output of two adjacent analog channels (NC and NO) when the control signal changes state.
Q <sub>C</sub>	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NO or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, Q <sub>C</sub> = C <sub>L</sub> × ΔV <sub>COM</sub> , C <sub>L</sub> is the load capacitance and ΔV <sub>COM</sub> is the change in analog output voltage.
C <sub>NO(OFF)</sub>	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF
C <sub>NO(ON)</sub>	Capacitance at the NO port when the corresponding channel (NO to COM) is ON
C <sub>COM(ON)</sub>	Capacitance at the COM port when the corresponding channel (COM to NO) is ON
C <sub>COM(OFF)</sub>	Capacitance at the COM port when the corresponding channel (COM to NO) is OFF
C <sub>i</sub>	Capacitance of control input (IN)
O <sub>ISO</sub>	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM or NO to COM) in the OFF state.
X <sub>TALK</sub>	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC to NO or NO to NC). This is measured in a specific frequency and in dB.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is –3 dB below the DC gain.
I <sub>+</sub>	Static power-supply current with the control (IN) pin at V <sub>+</sub> or GND

PARAMETER MEASUREMENT INFORMATION

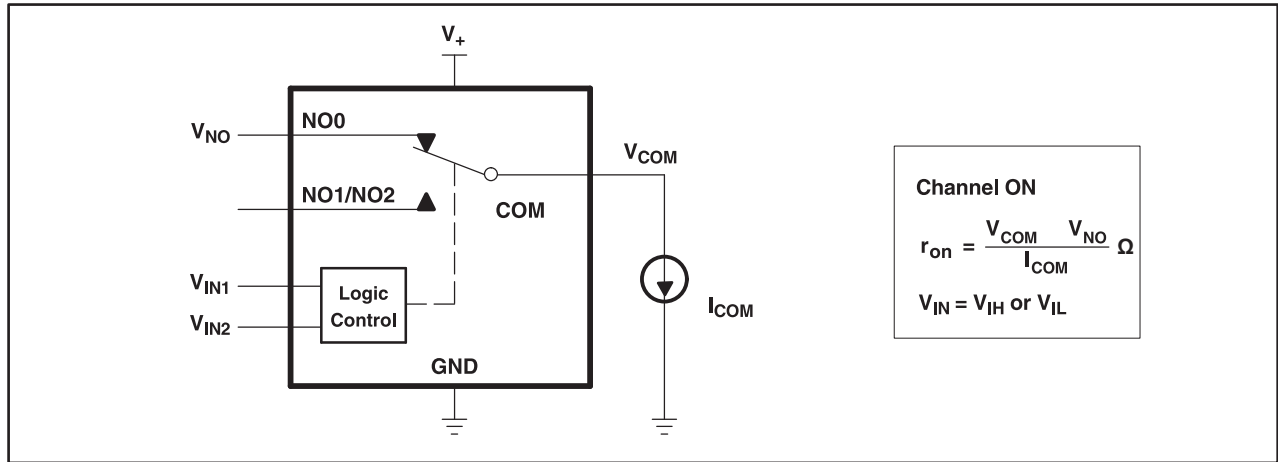


Figure 13. ON-State Resistance ( $r_{on}$ )

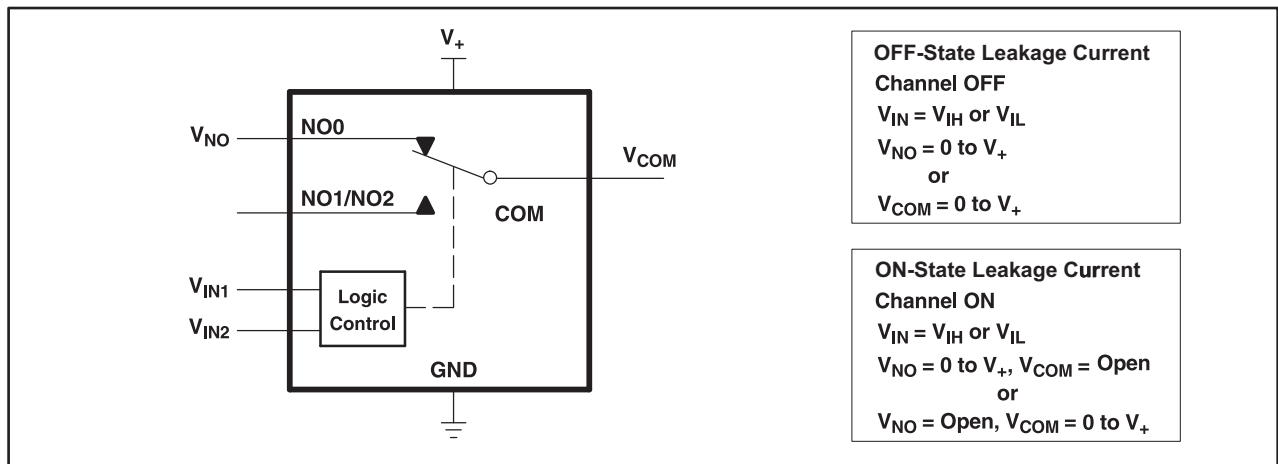


Figure 14. ON- and OFF-State Leakage Current ( $I_{COM(ON)}$ ,  $I_{COM(OFF)}$ ,  $I_{NO(ON)}$ ,  $I_{NO(OFF)}$ )

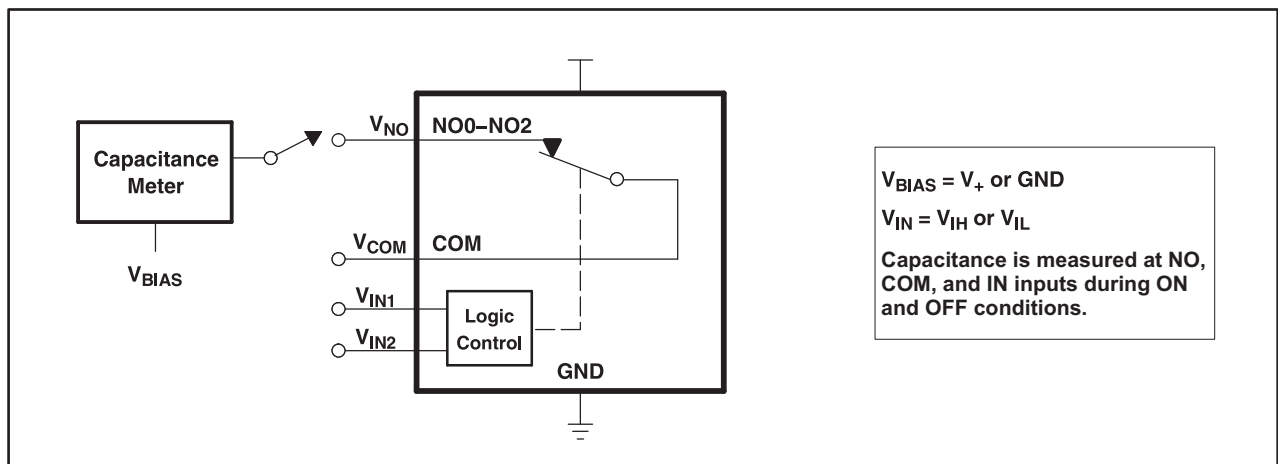


Figure 15. Capacitance ( $C_I$ ,  $C_{COM(ON)}$ ,  $C_{NO(OFF)}$ ,  $C_{COM(OFF)}$ ,  $C_{NO(ON)}$ )

- A. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_r < 5$  ns,  $t_f < 5$  ns.
- B.  $C_L$  includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION (continued)

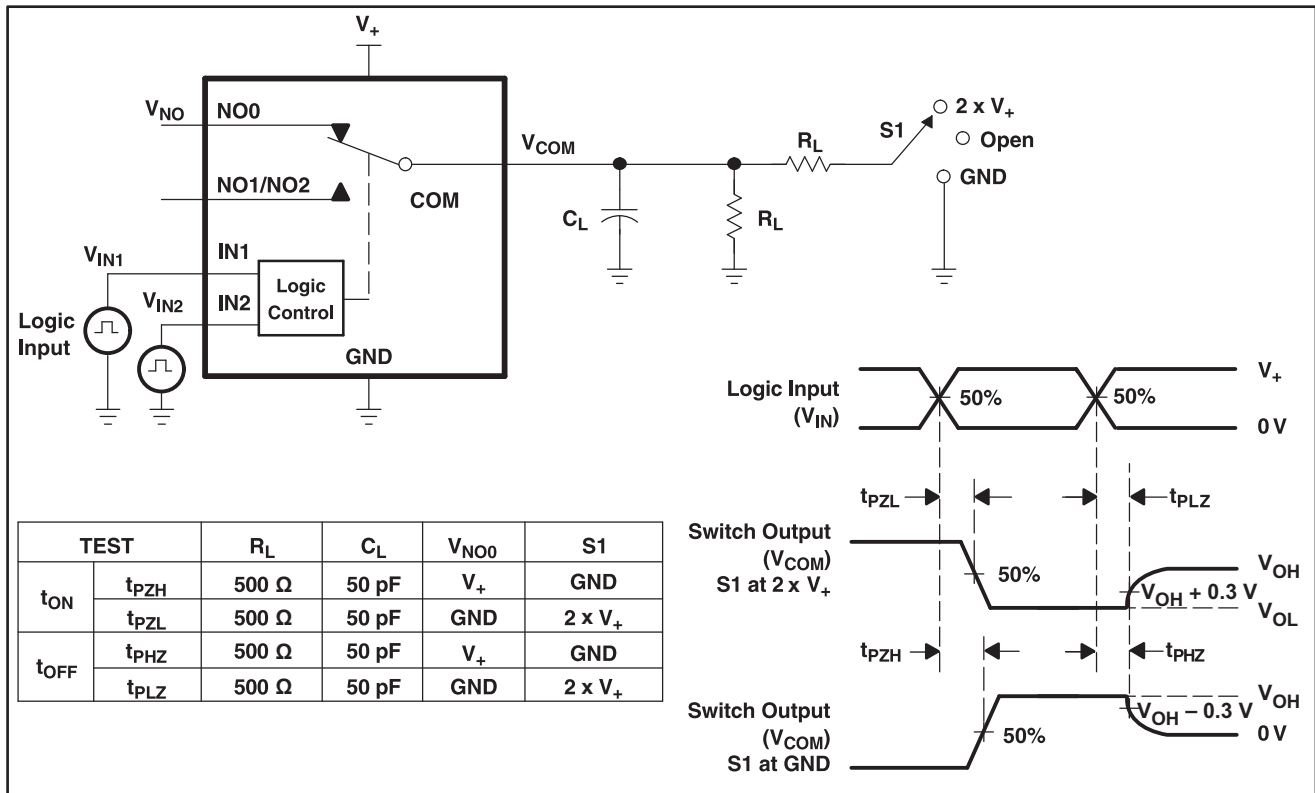


Figure 16. Turn-On ( $t_{ON}$ ) and Turn-Off Time ( $t_{OFF}$ )

- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_r < 5$  ns,  $t_f < 5$  ns.
- D.  $C_L$  includes probe and jig capacitance.

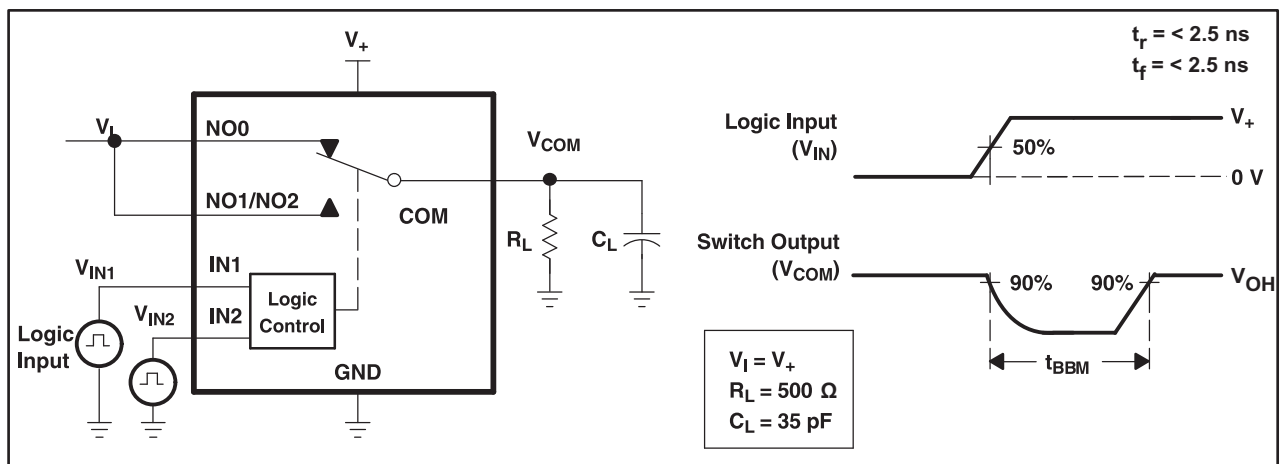


Figure 17. Break-Before-Make Time ( $t_{BBM}$ )

PARAMETER MEASUREMENT INFORMATION (continued)

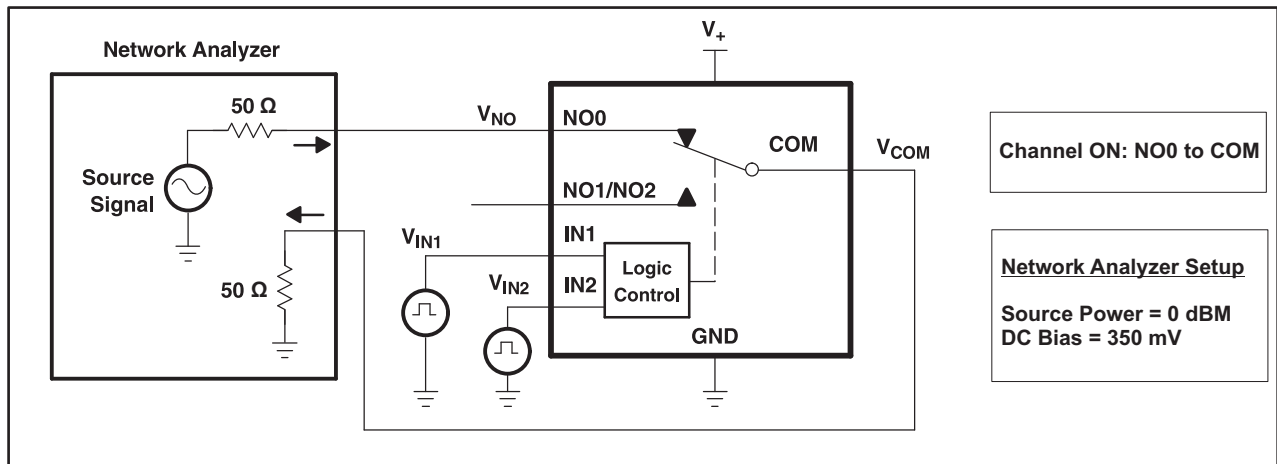


Figure 18. Bandwidth (BW)

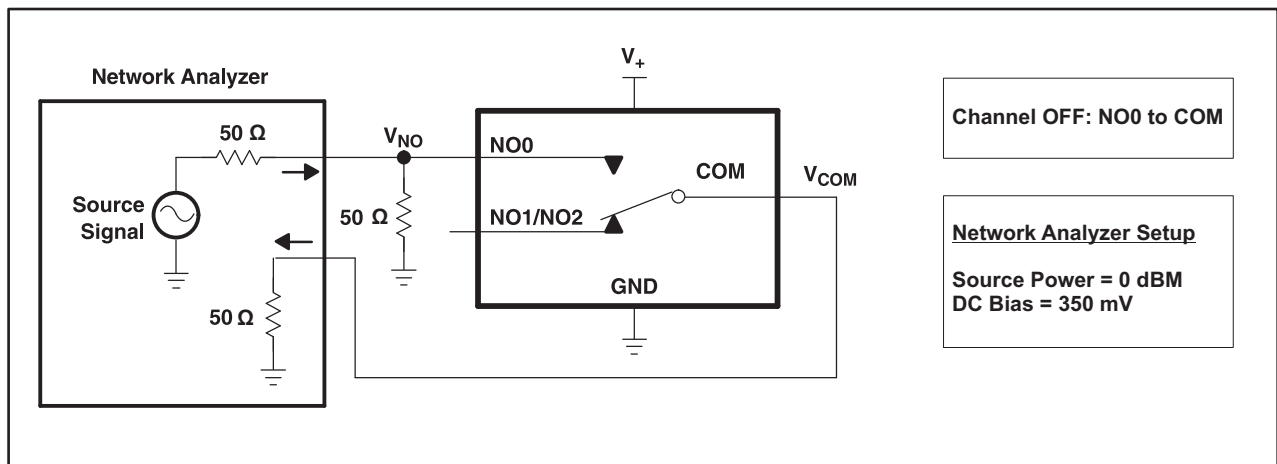


Figure 19. OFF Isolation ( $O_{ISO}$ )

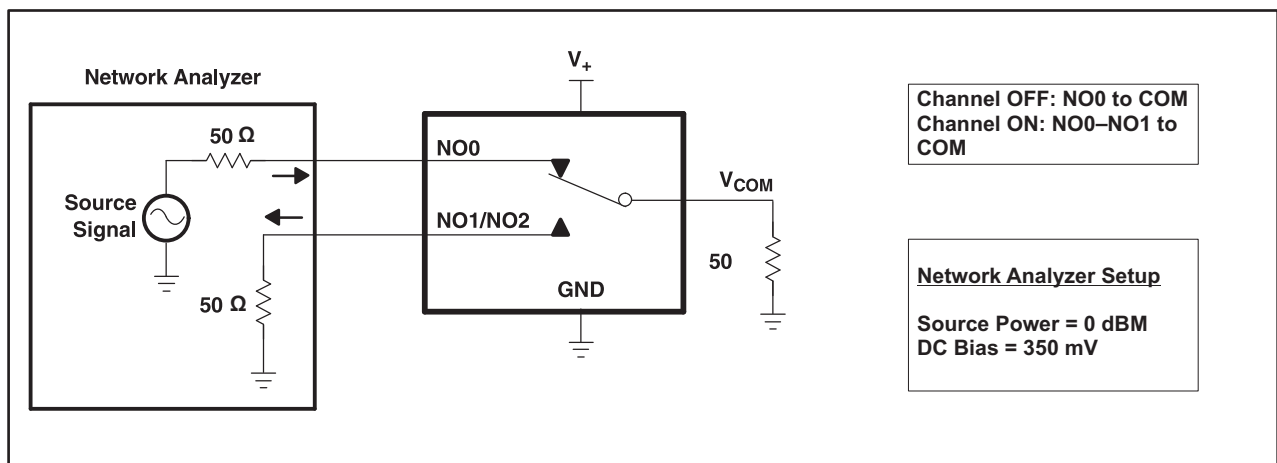


Figure 20. Crosstalk ( $X_{TALK}$ )

- E. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_0 = 50 \Omega$ ,  $t_r < 5$  ns,  $t_f < 5$  ns.
- F.  $C_L$  includes probe and jig capacitance.



PARAMETER MEASUREMENT INFORMATION (continued)

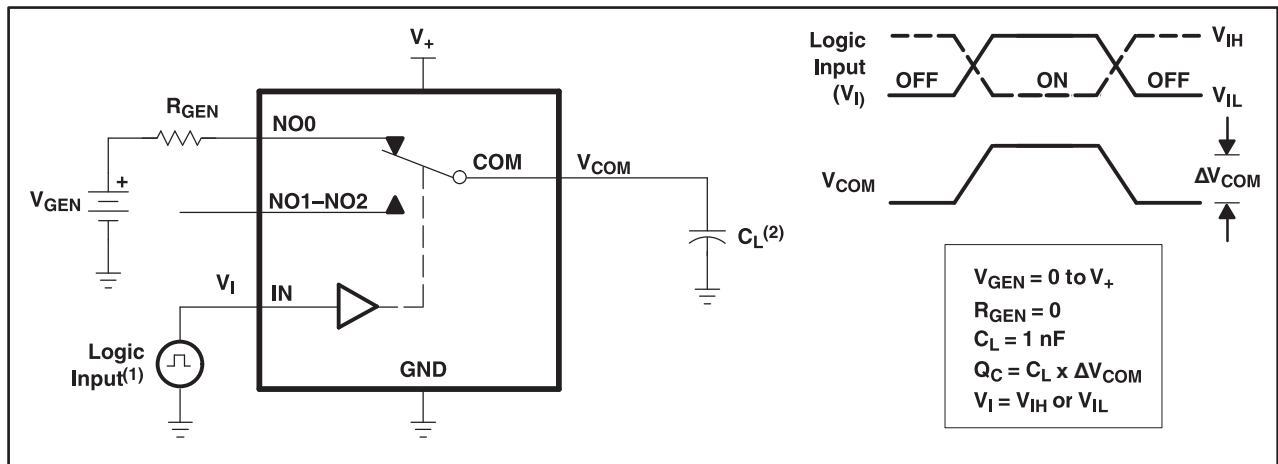


Figure 21. Charge Injection ( $Q_C$ )

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS5A3357QDCURQ1	ACTIVE	VSSOP	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	JAVR	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF TS5A3357-Q1 :**

- Catalog: [TS5A3357](#)

## NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A3357QDCURQ1	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

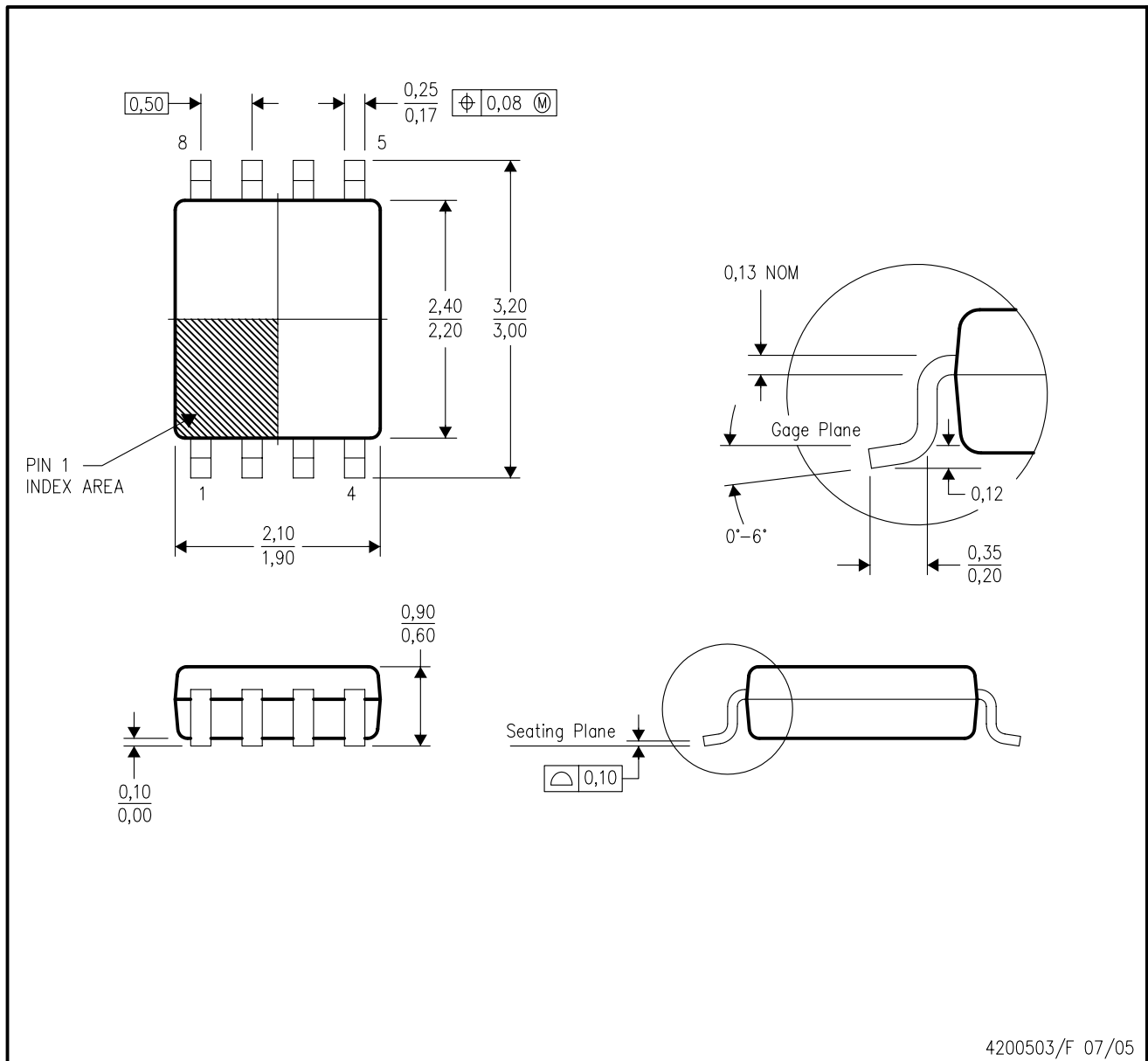


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A3357QDCURQ1	VSSOP	DCU	8	3000	202.0	201.0	28.0

DCU (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-187 variation CA.

DCU (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



4210064/C 04/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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