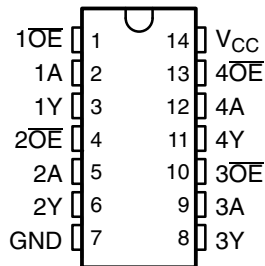


SN54AHCT125, SN74AHCT125 QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

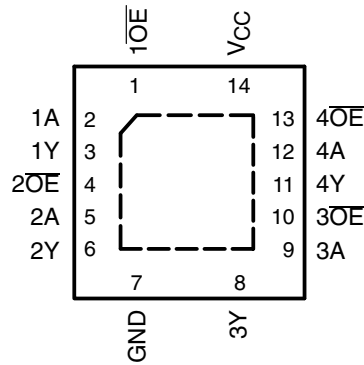
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- Inputs Are TTL-Voltage Compatible
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

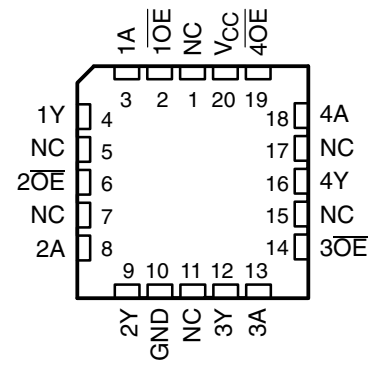
SN54AHCT125 . . . J OR W PACKAGE
SN74AHCT125 . . . D, DB, DGV, N, NS,
OR PW PACKAGE
(TOP VIEW)



SN74AHCT125 . . . RGY PACKAGE
(TOP VIEW)



SN54AHCT125 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The 'AHCT125 devices are quadruple bus buffer gates featuring independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (\overline{OE}) input is high. When \overline{OE} is low, the respective gate passes the data from the A input to its Y output.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

| T_A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|-------------|----------------|-----------------------|------------------|
| –40°C to 85°C | QFN – RGY | Tape and reel | SN74AHCT125RGYR | HB125 |
| | PDIP – N | Tube | SN74AHCT125N | SN74AHCT125N |
| | SOIC – D | Tube | SN74AHCT125D | AHCT125 |
| | | Tape and reel | SN74AHCT125DR | |
| | SOP – NS | Tape and reel | SN74AHCT125NSR | AHCT125 |
| | SSOP – DB | Tape and reel | SN74AHCT125DBR | HB125 |
| | TSSOP – PW | Tube | SN74AHCT125PW | HB125 |
| Tape and reel | | SN74AHCT125PWR | | |
| –55°C to 125°C | TVSOP – DGV | Tape and reel | SN74AHCT125DGVR | HB125 |
| | CDIP – J | Tube | SNJ54AHCT125J | SNJ54AHCT125J |
| | CFP – W | Tube | SNJ54AHCT125W | SNJ54AHCT125W |
| | LCCC – FK | Tube | SNJ54AHCT125FK | SNJ54AHCT125FK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

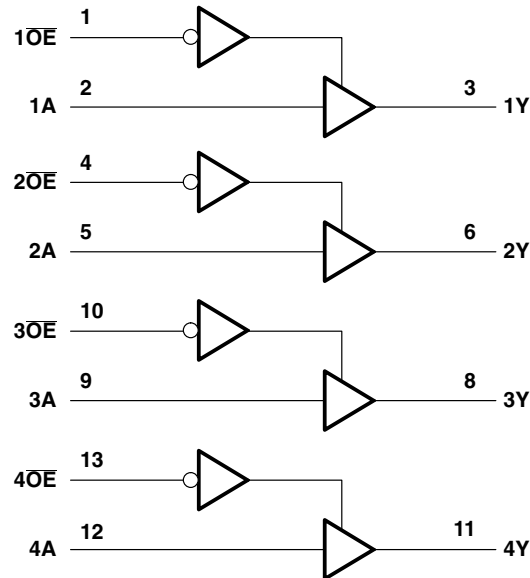
SN54AHCT125, SN74AHCT125 QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

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FUNCTION TABLE
(each buffer)

| INPUTS | | OUTPUT |
|--------|---|--------|
| OE | A | Y |
| L | H | H |
| L | L | L |
| H | X | Z |

logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, J, N, NS, PW, RGY, and W packages.

SN54AHCT125, SN74AHCT125 QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--|----------------------------|
| Supply voltage range, V_{CC} | –0.5 V to 7 V |
| Input voltage range, V_I (see Note 1) | –0.5 V to 7 V |
| Output voltage range, V_O (see Note 1) | –0.5 V to $V_{CC} + 0.5$ V |
| Input clamp current, I_{IK} ($V_I < 0$) | –20 mA |
| Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) | ±20 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) | ±25 mA |
| Continuous current through V_{CC} or GND | ±50 mA |
| Package thermal impedance, θ_{JA} (see Note 2): D package | 86°C/W |
| (see Note 2): DB package | 96°C/W |
| (see Note 2): DGV package | 127°C/W |
| (see Note 2): N package | 80°C/W |
| (see Note 2): NS package | 76°C/W |
| (see Note 2): PW package | 113°C/W |
| (see Note 3): RGY package | 47°C/W |
| Storage temperature range, T_{stg} | –65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51-7.
 3. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 4)

| | SN54AHCT125 | | SN74AHCT125 | | UNIT |
|--|-------------|----------|-------------|----------|------|
| | MIN | MAX | MIN | MAX | |
| V_{CC} Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| V_{IH} High-level input voltage | 2 | | 2 | | V |
| V_{IL} Low-level input voltage | | 0.8 | | 0.8 | V |
| V_I Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| V_O Output voltage | 0 | V_{CC} | 0 | V_{CC} | V |
| I_{OH} High-level output current | | –8 | | –8 | mA |
| I_{OL} Low-level output current | | 8 | | 8 | mA |
| $\Delta t/\Delta v$ Input transition rise or fall rate | | 20 | | 20 | ns/V |
| T_A Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN54AHCT125, SN74AHCT125 QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | T _A = 25°C | | | SN54AHCT125 | | SN74AHCT125 | | UNIT |
|--------------------|---|-----------------|-----------------------|-----|-------|-------------|------|-------------|-----|------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| V _{OH} | I _{OH} = -50 μA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | V | |
| | I _{OH} = -8 mA | | 3.94 | | | 3.8 | | 3.8 | | |
| V _{OL} | I _{OL} = 50 μA | 4.5 V | | | 0.1 | | | 0.1 | V | |
| | I _{OL} = 8 mA | | | | 0.36 | | 0.44 | 0.44 | | |
| I _I | V _I = 5.5 V or GND | 0 V to 5.5 V | | | ±0.1 | | ±1* | ±1 | μA | |
| I _{OZ} | V _O = V _{CC} or GND | 5.5 V | | | ±0.25 | | ±2.5 | ±2.5 | μA | |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | 5.5 V | | | 2 | | 20 | 20 | μA | |
| ΔI _{CC} † | One input at 3.4 V, Other inputs at V _{CC} or GND | 5.5 V | | | 1.35 | | 1.5 | 1.5 | mA | |
| C _i | V _I = V _{CC} or GND | 5 V | | | 4 | 10 | | 10 | pF | |
| C _o | V _O = V _{CC} or GND | 5 V | | | 15 | | | | pF | |

* On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

† This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | T _A = 25°C | | | SN54AHCT125 | | SN74AHCT125 | | UNIT |
|--------------------|--------------|-------------|------------------------|-----------------------|-------|-------|-------------|-------|-------------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t _{PLH} | A | Y | C _L = 15 pF | | 3.8** | 5.5** | 1** | 6.5** | 1 | 6.5 | ns |
| t _{PHL} | | | | | 3.8** | 5.5** | 1** | 6.5** | 1 | 6.5 | |
| t _{PZH} | OE | Y | C _L = 15 pF | | 3.6** | 5.1** | 1** | 6** | 1 | 6 | ns |
| t _{PZL} | | | | | 3.6** | 5.1** | 1** | 6** | 1 | 6 | |
| t _{PHZ} | OE | Y | C _L = 15 pF | | 4.6** | 6.8** | 1** | 8** | 1 | 8 | ns |
| t _{PLZ} | | | | | 4.6** | 6.8** | 1** | 8** | 1 | 8 | |
| t _{PLH} | A | Y | C _L = 50 pF | | 5.3 | 7.5 | 1 | 8.5 | 1 | 8.5 | ns |
| t _{PHL} | | | | | 5.3 | 7.5 | 1 | 8.5 | 1 | 8.5 | |
| t _{PZH} | OE | Y | C _L = 50 pF | | 5.1 | 7.1 | 1 | 8 | 1 | 8 | ns |
| t _{PZL} | | | | | 5.1 | 7.1 | 1 | 8 | 1 | 8 | |
| t _{PHZ} | OE | Y | C _L = 50 pF | | 6.1 | 8.8 | 1 | 10 | 1 | 10 | ns |
| t _{PLZ} | | | | | 6.1 | 8.8 | 1 | 10 | 1 | 10 | |
| t _{sk(o)} | | | C _L = 50 pF | | | 1*** | | | 1 | ns | |

** On products compliant to MIL-PRF-38535, this parameter is not production tested.

*** On products compliant to MIL-PRF-38535, this parameter does not apply.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

| PARAMETER | | SN74AHCT125 | | UNIT |
|--------------------|---|-------------|------|------|
| | | MIN | MAX | |
| V _{OL(P)} | Quiet output, maximum dynamic V _{OL} | | 0.8 | V |
| V _{OL(V)} | Quiet output, minimum dynamic V _{OL} | | -0.8 | V |
| V _{OH(V)} | Quiet output, minimum dynamic V _{OH} | 4.4 | | V |
| V _{IH(D)} | High-level dynamic input voltage | 2 | | V |
| V _{IL(D)} | Low-level dynamic input voltage | | 0.8 | V |

NOTE 5: Characteristics are for surface-mount packages only.



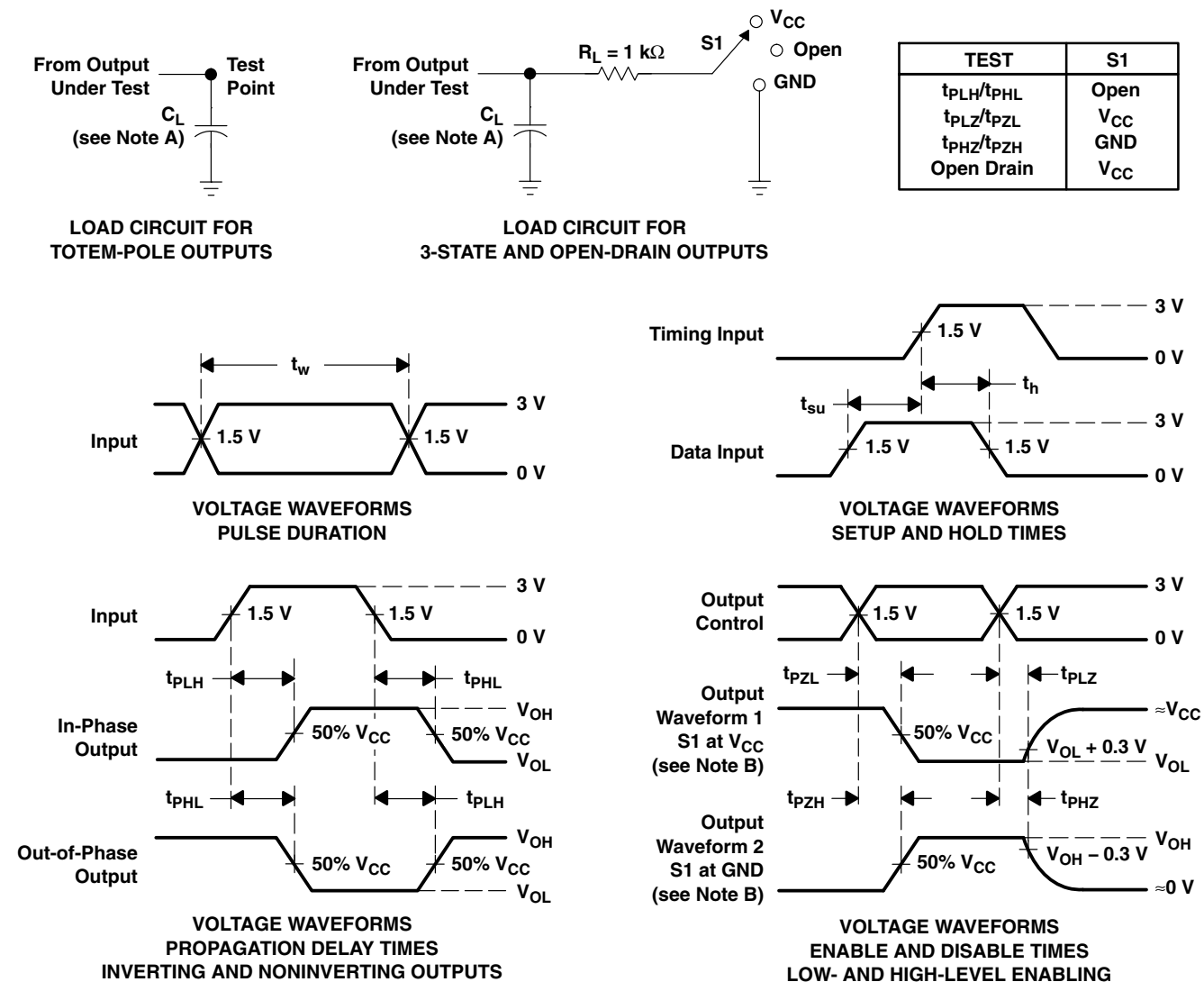
SN54AHCT125, SN74AHCT125 QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

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operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|--|-----------------------------|-----|------|
| C_{pd} Power dissipation capacitance | No load, $f = 1\text{ MHz}$ | 14 | pF |

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|---|-------------------------|
| 5962-9686901Q2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962- 9686901Q2A SNJ54AHCT 125FK | Samples |
| 5962-9686901QCA | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9686901QC A SNJ54AHCT125J | Samples |
| 5962-9686901QDA | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9686901QD A SNJ54AHCT125W | Samples |
| SN74AHCT125D | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHCT125 | Samples |
| SN74AHCT125DBLE | OBSOLETE | SSOP | DB | 14 | | TBD | Call TI | Call TI | -40 to 85 | | |
| SN74AHCT125DBR | ACTIVE | SSOP | DB | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HB125 | Samples |
| SN74AHCT125DG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHCT125 | Samples |
| SN74AHCT125DGVR | ACTIVE | TVSOP | DGV | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HB125 | Samples |
| SN74AHCT125DR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU CU SN | Level-1-260C-UNLIM | -40 to 125 | AHCT125 | Samples |
| SN74AHCT125DRE4 | ACTIVE | SOIC | D | 14 | | TBD | Call TI | Call TI | -40 to 125 | | Samples |
| SN74AHCT125DRG4 | OBSOLETE | SOIC | D | 14 | | TBD | Call TI | Call TI | -40 to 85 | | |
| SN74AHCT125N | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | SN74AHCT125N | Samples |
| SN74AHCT125NE4 | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | SN74AHCT125N | Samples |
| SN74AHCT125NSR | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHCT125 | Samples |
| SN74AHCT125NSRE4 | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHCT125 | Samples |
| SN74AHCT125PW | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HB125 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|---|-------------------------|
| SN74AHCT125PWE4 | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HB125 | Samples |
| SN74AHCT125PWG4 | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HB125 | Samples |
| SN74AHCT125PWLE | OBSOLETE | TSSOP | PW | 14 | | TBD | Call TI | Call TI | -40 to 85 | | |
| SN74AHCT125PWR | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HB125 | Samples |
| SN74AHCT125PWRE4 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HB125 | Samples |
| SN74AHCT125PWRG4 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HB125 | Samples |
| SN74AHCT125RGYR | ACTIVE | VQFN | RGY | 14 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | HB125 | Samples |
| SNJ54AHCT125FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962- 9686901Q2A SNJ54AHCT 125FK | Samples |
| SNJ54AHCT125J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9686901QC A SNJ54AHCT125J | Samples |
| SNJ54AHCT125W | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9686901QD A SNJ54AHCT125W | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54AHCT125, SN74AHCT125 :

- Catalog: [SN74AHCT125](#)
- Automotive: [SN74AHCT125-Q1](#), [SN74AHCT125-Q1](#)
- Enhanced Product: [SN74AHCT125-EP](#), [SN74AHCT125-EP](#)
- Military: [SN54AHCT125](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74AHCT125DBR | SSOP | DB | 14 | 2000 | 330.0 | 16.4 | 8.2 | 6.6 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74AHCT125DGVR | TVSOP | DGV | 14 | 2000 | 330.0 | 12.4 | 6.8 | 4.0 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74AHCT125DR | SOIC | D | 14 | 2500 | 330.0 | 16.8 | 6.5 | 9.5 | 2.3 | 8.0 | 16.0 | Q1 |
| SN74AHCT125DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74AHCT125DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74AHCT125NSR | SO | NS | 14 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74AHCT125PWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74AHCT125RGYR | VQFN | RGY | 14 | 3000 | 330.0 | 12.4 | 3.75 | 3.75 | 1.15 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74AHCT125DBR | SSOP | DB | 14 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74AHCT125DGVR | TVSOP | DGV | 14 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74AHCT125DR | SOIC | D | 14 | 2500 | 364.0 | 364.0 | 27.0 |
| SN74AHCT125DR | SOIC | D | 14 | 2500 | 333.2 | 345.9 | 28.6 |
| SN74AHCT125DR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| SN74AHCT125NSR | SO | NS | 14 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74AHCT125PWR | TSSOP | PW | 14 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74AHCT125RGYR | VQFN | RGY | 14 | 3000 | 367.0 | 367.0 | 35.0 |

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |

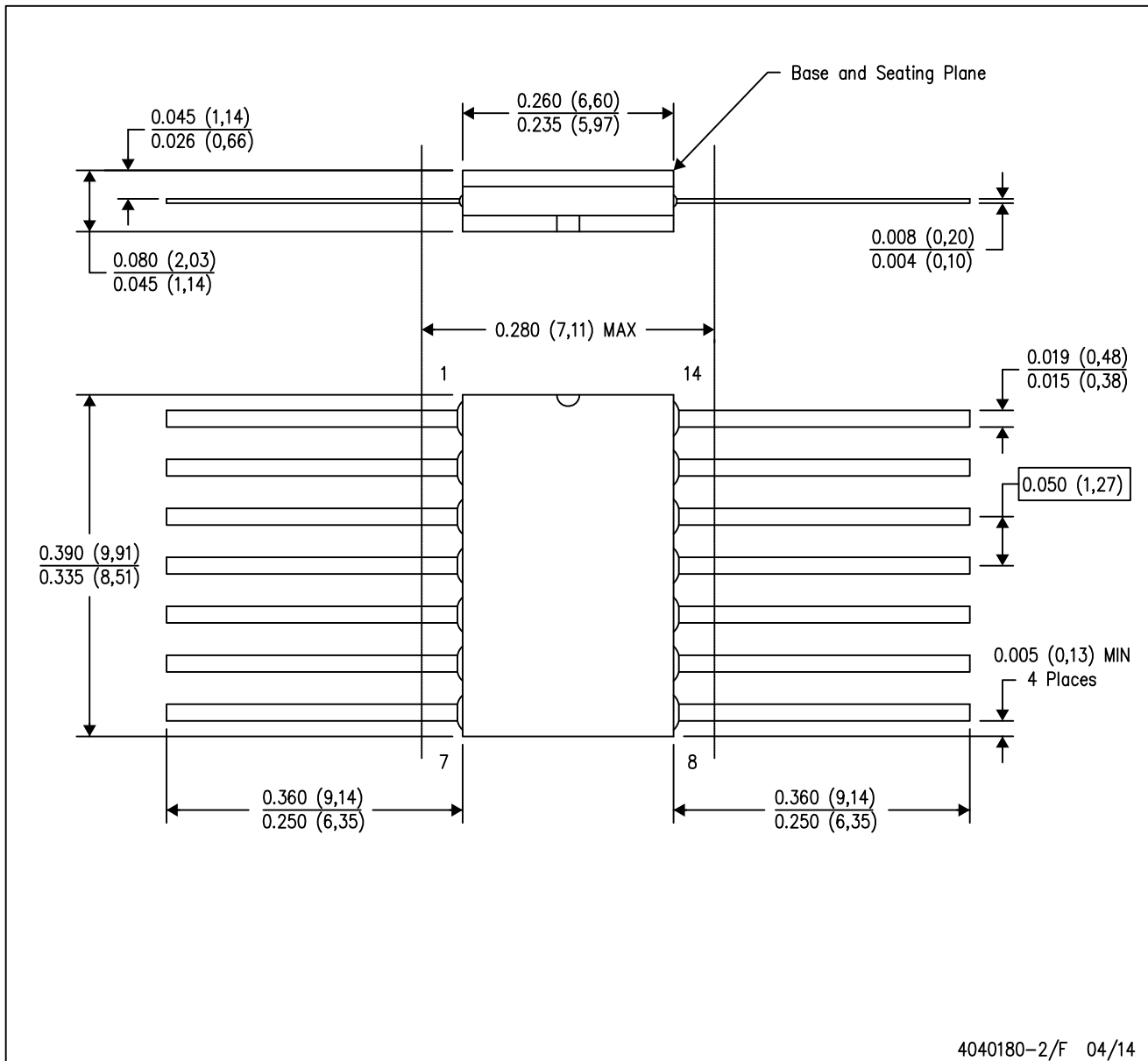


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- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF TERMINALS ** | A | | B | |
|---------------------|------------------|------------------|------------------|------------------|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

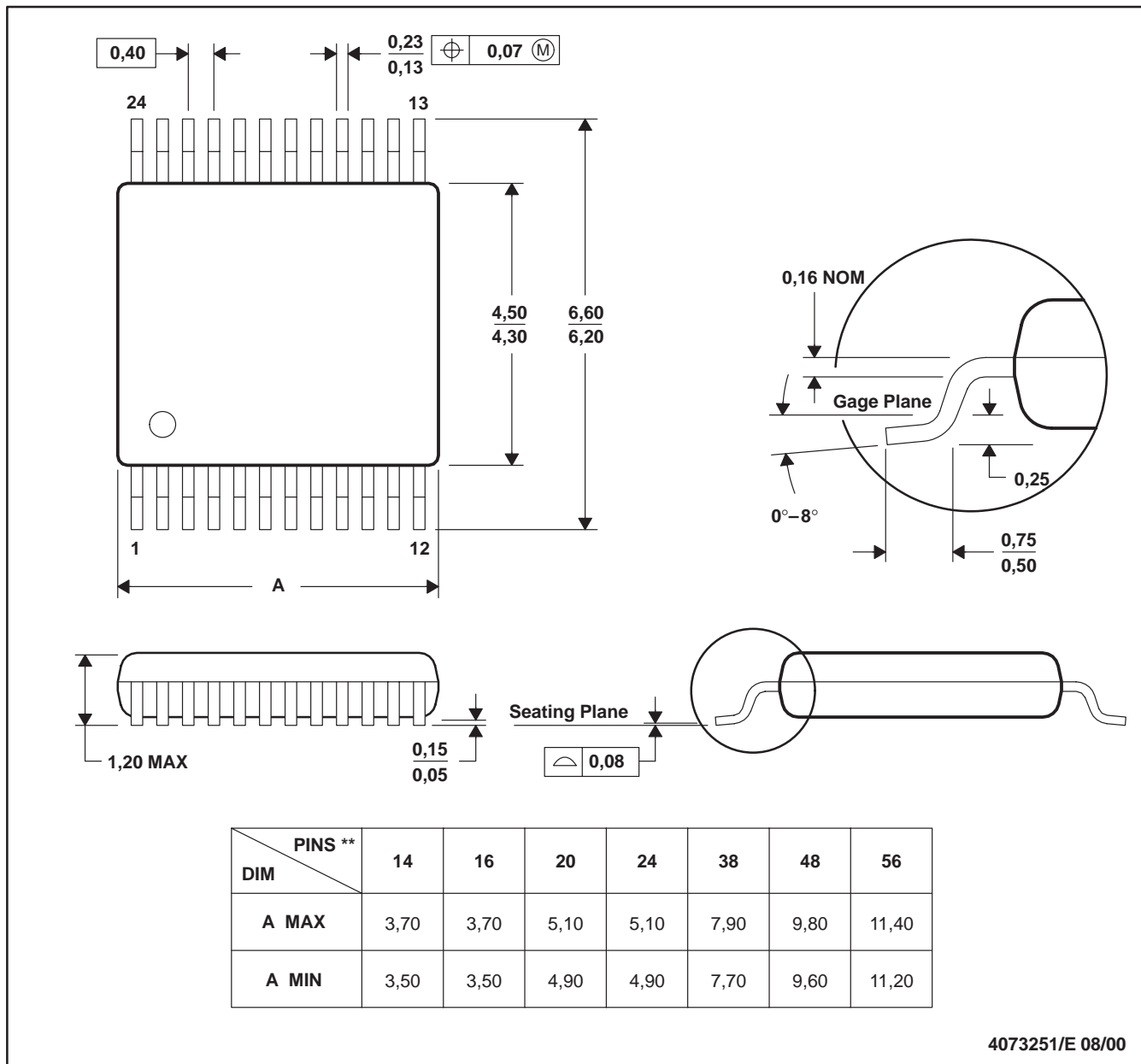


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

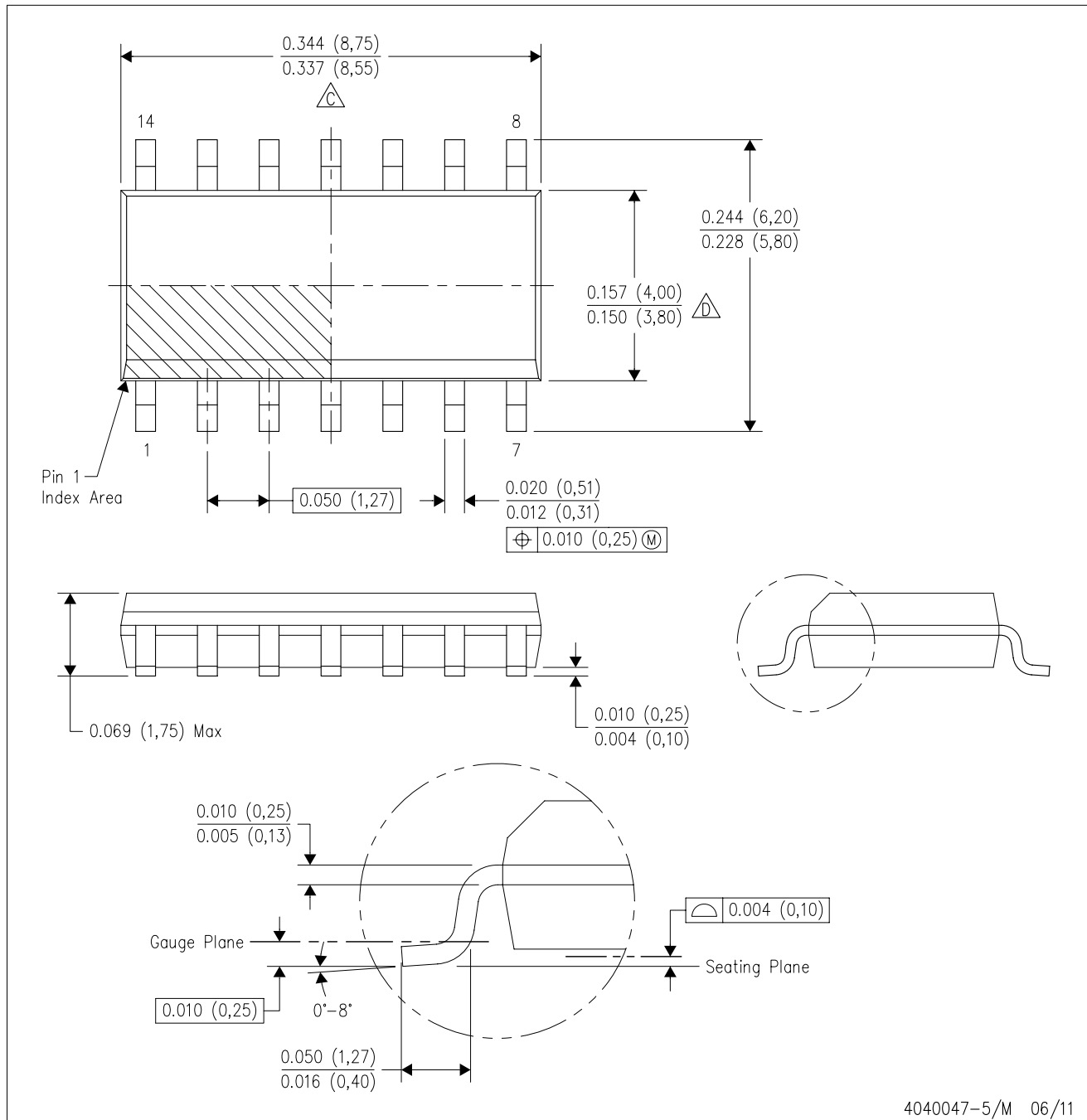




4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

D (R-PDSO-G14)

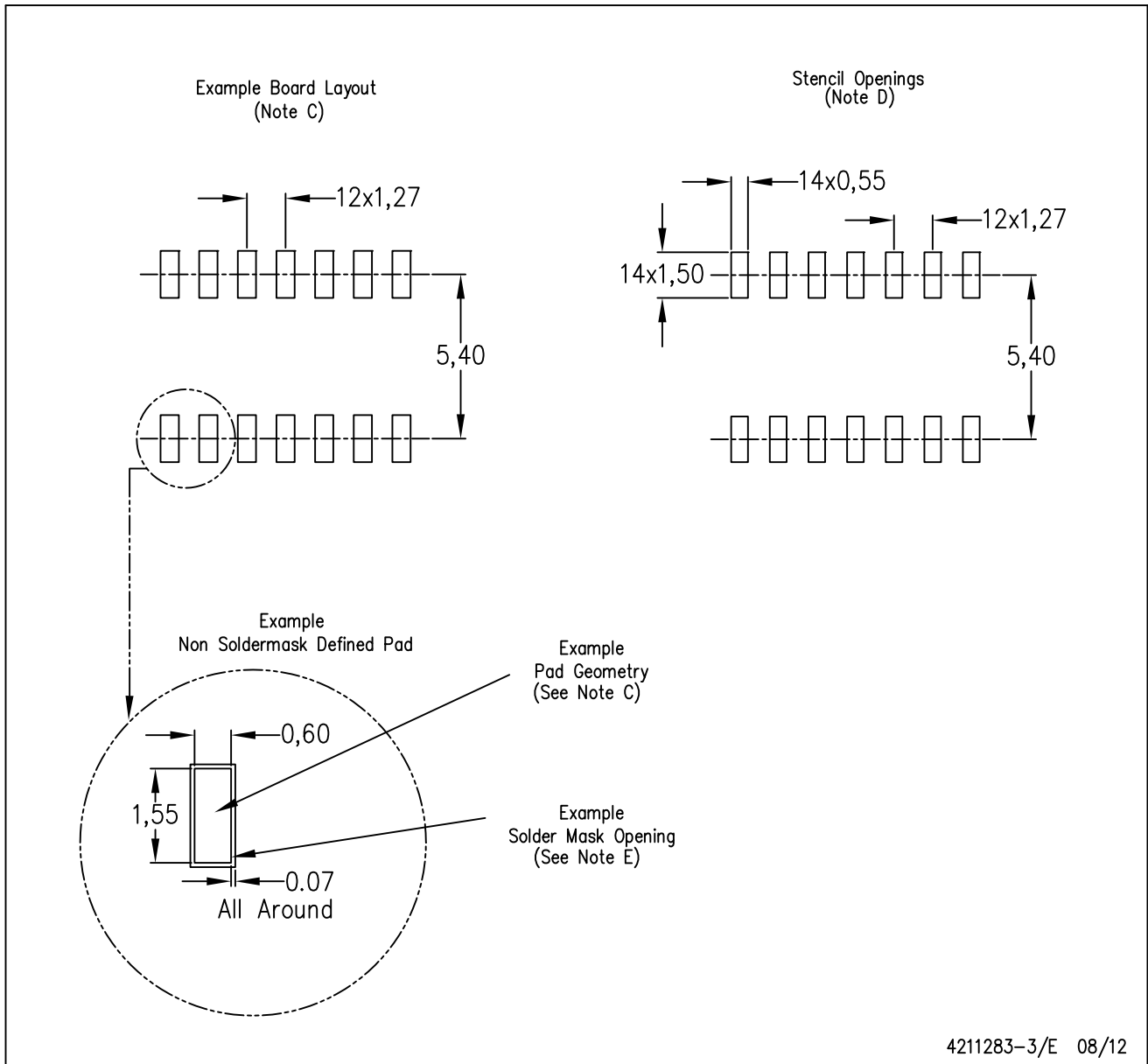
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

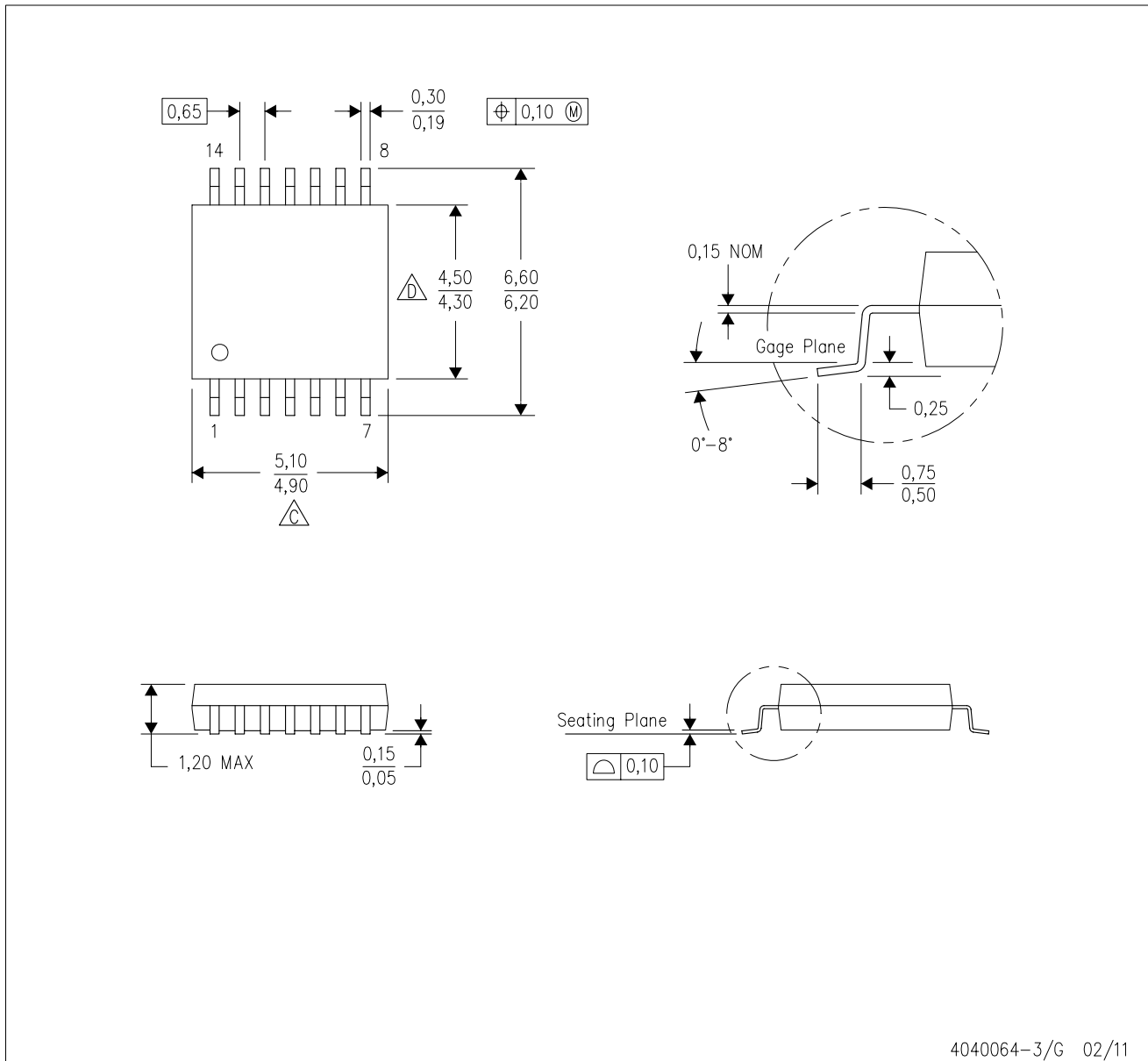


4211283-3/E 08/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

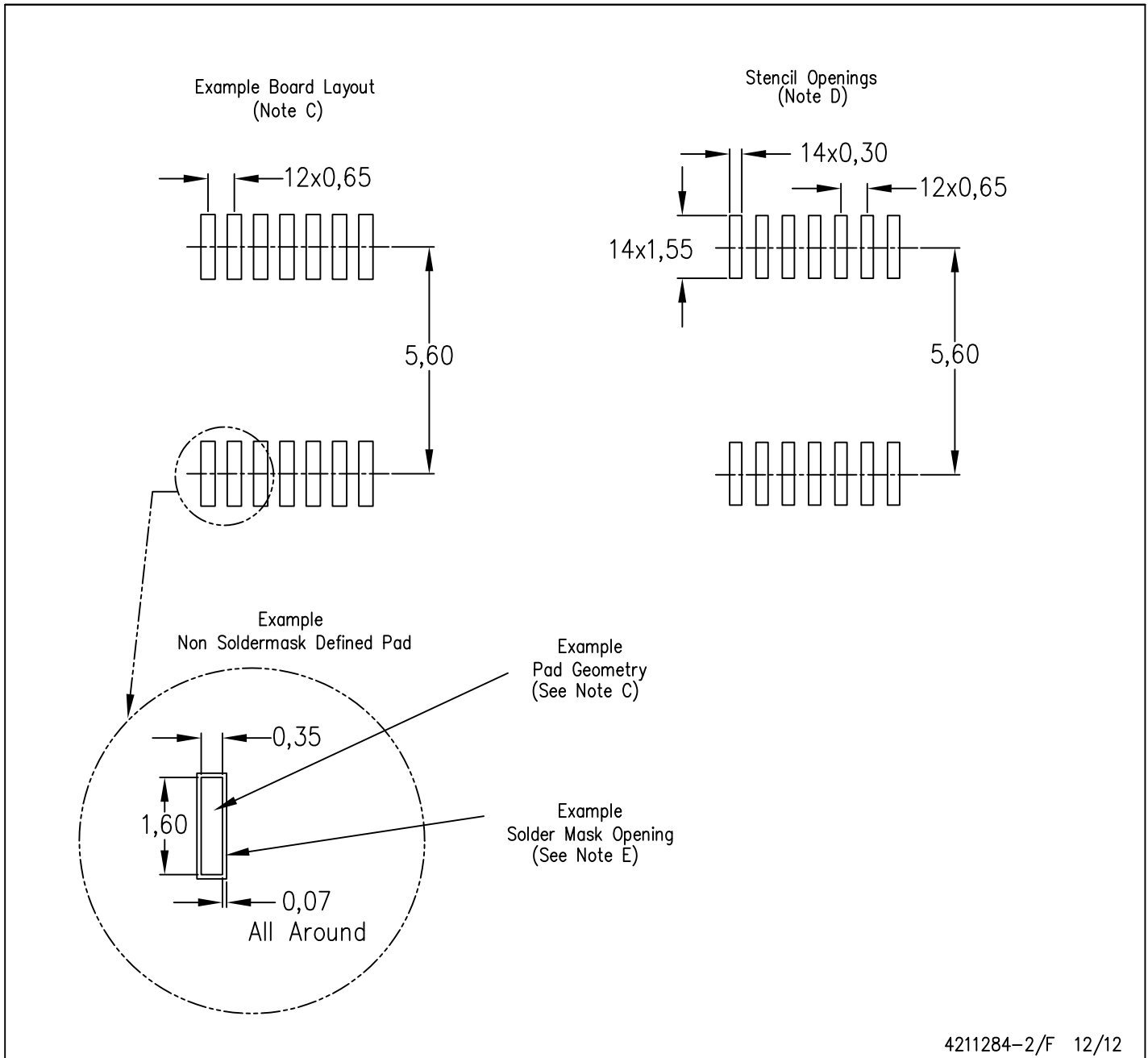
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RGY (S-PVQFN-N14)

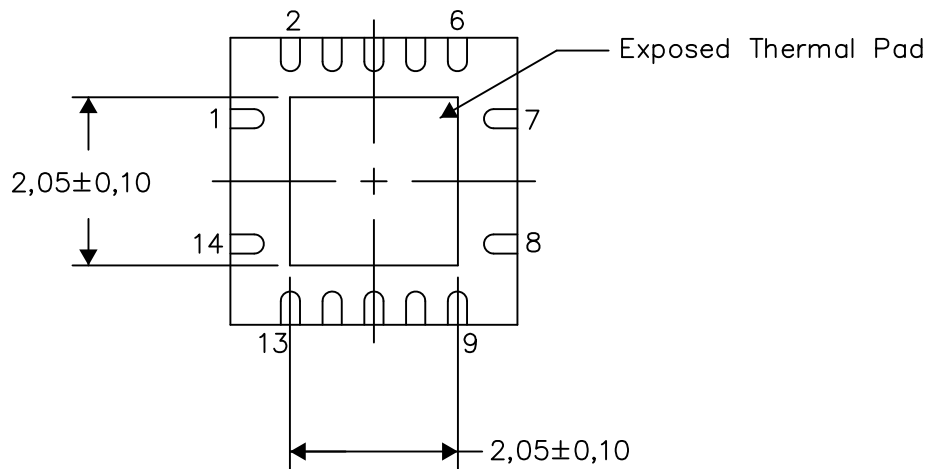
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

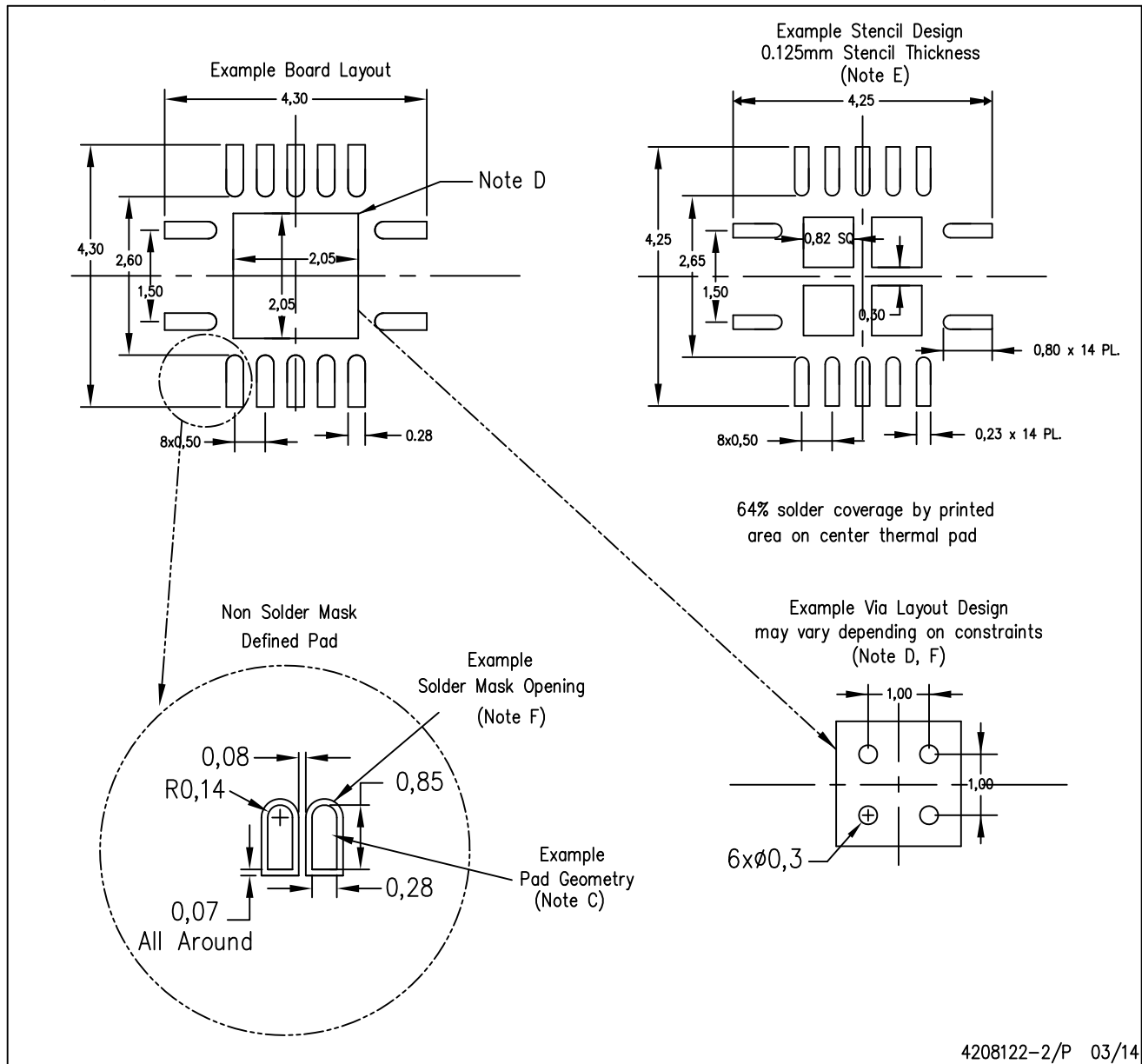
Exposed Thermal Pad Dimensions

4206353-2/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



4208122-2/P 03/14

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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