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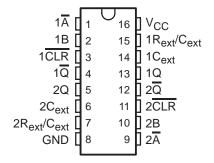
- Operating Range 2-V to 5.5-V V_{CC}
- Schmitt-Trigger Circuitry On A, B, and CLR Inputs for Slow Input Transition Rates
- Edge Triggered From Active-High or Active-Low Gated Logic Inputs
- Retriggerable for Very Long Output Pulses
- Overriding Clear Terminates Output Pulse
- Glitch-Free Power-Up Reset On Outputs
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

description/ordering information

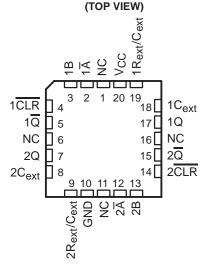
The 'AHC123A devices are dual retriggerable monostable multivibrators designed for 2-V to $5.5\text{-V}\ \text{V}_{CC}$ operation.

These edge-triggered multivibrators feature output pulse-duration control by three methods. In the first method, the \overline{A} input is low, and the B input goes high. In the second method, the B input is high, and the \overline{A} input goes low. In the third method, the \overline{A} input is low, the B input is high, and the clear (\overline{CLR}) input goes high.

SN54AHC123A . . . J OR W PACKAGE SN74AHC123A . . . D, DB, DGV, N, OR PW PACKAGE (TOP VIEW)



SN54AHC123A . . . FK PACKAGE



NC - No internal connection

ORDERING INFORMATION

TA	PACK	AGE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	PDIP – N	Tube	SN74AHC123AN	SN74AHC123AN
	colo p	Tube	SN74AHC123AD	ALICA00A
400C to 050C	SOIC - D	Tape and reel	SN74AHC123ADR	AHC123A
–40°C to 85°C	SSOP – DB	Tape and reel	SN74AHC123ADBR	HA123A
	TSSOP - PW	Tape and reel	SN74AHC123APWR	HA123A
	TVSOP - DGV	Tape and reel	SN74AHC123ADGVR	HA123A
	CDIP – J	Tube	SNJ54AHC123AJ	SNJ54AHC123AJ
−55°C to 125°C	CFP – W	Tube	SNJ54AHC123AW	SNJ54AHC123AW
	LCCC – FK	Tube	SNJ54AHC123AFK	SNJ54AHC123AFK

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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description/ordering information (continued)

The output pulse duration is programmed by selecting external resistance and capacitance values. The external timing capacitor must be connected between C_{ext} and R_{ext}/C_{ext} (positive) and an external resistor connected between R_{ext}/C_{ext} and V_{CC} . To obtain variable pulse durations, connect an external variable resistance between R_{ext}/C_{ext} and V_{CC} . The output pulse duration also can be reduced by taking \overline{CLR} low.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. The \overline{A} , B, and \overline{CLR} inputs have Schmitt triggers with sufficient hysteresis to handle slow input transition rates with jitter-free triggering at the outputs.

Once triggered, the basic pulse duration can be extended by retriggering the gated low-level-active (A) or high-level-active (B) input. Pulse duration can be reduced by taking CLR low. CLR input can be used to override A or B inputs. The input/output timing diagram illustrates pulse control by retriggering the inputs and early clearing.

The variance in output pulse duration from device to device typically is less than $\pm 0.5\%$ for given external timing components. An example of this distribution for the 'AHC123A is shown in Figure 10. Variations in output pulse duration versus supply voltage and temperature are shown in Figure 6.

During power up, Q outputs are in the low state, and \overline{Q} outputs are in the high state. The outputs are glitch free, without applying a reset pulse.

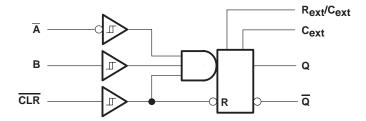
For additional application information on multivibrators, see the application report *Designing With the SN74AHC123A and SN74AHCT123A*, literature number SCLA014.

FUNCTION TABLE (each multivibrator)

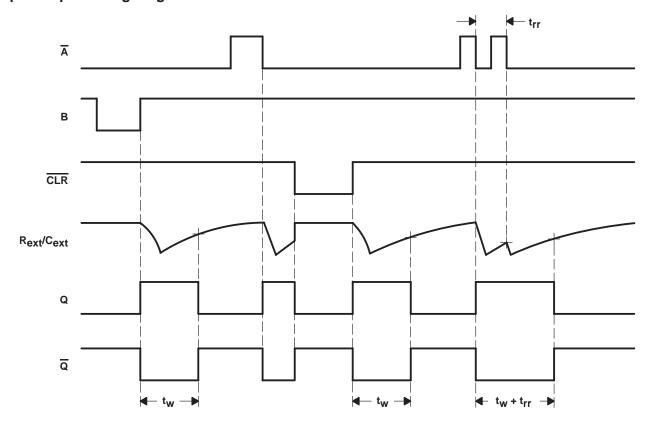
	NPUTS	i	OUT	PUTS
CLR	Ā	В	Q	Q
L	Χ	Х	L	Н
X	Н	X	լ†	H [†]
X	Χ	L	∟†	H [†]
Н	L	\uparrow	Л	T
Н	\downarrow	Н	Л	Т
\uparrow	L	Н	Л	П

[†]These outputs are based on the assumption that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the setup.

logic diagram, each multivibrator (positive logic)



input/output timing diagram



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absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V _{CC} (see Note 1)		0.5 V to 7 V
Input voltage range, V _I (see Note 2)		–0.5 V to 7 V
Output voltage range in high or low state, VO (s	see Note 1)	-0.5 V to V _{CC} + 0.5 V
Output voltage range in power-off state, VO (se	e Note 1)	0.5 V to 7 V
Input clamp current, $I_{IK}(V_I < 0)$		–20 mA
Output clamp current, IOK (VO < 0 or VO > VCC	c)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})		±25 mA
Continuous current through V _{CC} or GND		±50 mA
Package thermal impedance, θ_{JA} (see Note 3):	D package	73°C/W
	DB package	82°C/W
	DGV package	120°C/W
	N package	67°C/W
	PW package	108°C/W
Storage temperature range, T _{stg}		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. Voltage values are with respect to the network ground terminal.
 - 2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

			SN54AH	C123A	SN74AH	C123A	
			MIN	MAX	MIN	MAX	UNIT
VCC	Supply voltage		2	5.5	2	5.5	V
		V _{CC} = 2 V	1.5		1.5		
V_{IH}	High-level input voltage	V _{CC} = 3 V	2.1		2.1		V
		V _{CC} = 5.5 V	3.85		3.85		
		V _{CC} = 2 V		0.5		0.5	
V_{IL}	Low-level input voltage	V _{CC} = 3 V		0.9		0.9	V
		V _{CC} = 5.5 V		1.65		1.65	
VI	Input voltage		0	5.5	0	5.5	V
VO	Output voltage		0	Vcc	0	Vcc	V
		V _{CC} = 2 V		-50		-50	μΑ
lOH	High-level output current	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		-4		-4	4
		$V_{CC} = 5 V \pm 0.5 V$		-8		-8	mA
		V _{CC} = 2 V		50		50	μΑ
lOL	Low-level output current	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		4		4	4
		$V_{CC} = 5 V \pm 0.5 V$		8		8	mA
		V _{CC} = 2 V	5k		5k		
R _{ext}	External timing resistance	V _{CC} > 3 V	1k		1k		Ω
Δt/ΔV _{CC}	Power-up ramp rate		1		1		ms/V
T _A	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: Unused R_{ext}/C_{ext} terminals should be left unconnected. All remaining unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	DAMETER	TEST CONDITIONS	.,	T,	չ = 25°0	;	SN54AH	C123A	SN74AH	C123A	LINUT	
PA	ARAMETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT	
			2 V	1.9	2		1.9		1.9			
		I _{OH} = -50 μA	3 V	2.9	3		2.9		2.9			
۷он			4.5 V	4.4	4.5		4.4		4.4		V	
		$I_{OH} = -4 \text{ mA}$	3 V	2.58			2.48		2.48			
		$I_{OH} = -8 \text{ mA}$	4.5 V	3.94			3.8		3.8			
			2 V			0.1		0.1		0.1		
		I _{OL} = 50 μA	3 V			0.1		0.1		0.1		
VOL			4.5 V			0.1		0.1		0.1	V	
		I _{OL} = 4 mA	3 V			0.36		0.5		0.44		
		I _{OL} = 8 mA	4.5 V			0.36		0.5		0.44		
	R _{ext} /C _{ext} †	V _I = V _{CC} or GND	5.5 V			±0.25		±2.5		±2.5	•	
I _I	\overline{A} , B, and \overline{CLR}	$V_I = V_{CC}$ or GND	0 V to 5.5 V			±0.1		±1*		±1	μΑ	
ICC	Quiescent	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			4		40		40	μΑ	
			3 V		160	250		280		280		
ICC		$V_I = V_{CC}$ or GND, $R_{ext}/C_{ext} = 0.5 V_{CC}$	4.5 V		280	500		650		650	μΑ	
		Next/ Sext = 5.5 VCC	5.5 V		360	750		975		975		
Ci		$V_I = V_{CC}$ or GND	5 V		1.9	10				10	pF	

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested at $V_{CC} = 0 \text{ V}$.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V \pm 0.3 V (unless otherwise noted) (see Figure 1)

			TEST COMPITIONS	T,	λ = 25°C	;	SN54AH	C123A	SN74AH	LINUT	
			TEST CONDITIONS	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
_	Pulse	CLR		5			5		5		
t _W	duration	A or B trigger		5			5		5		ns
_	Dulas natrias		$R_{ext} = 1 k\Omega$, $C_{ext} = 100 pF$	‡	76		‡		‡		ns
^T rr	Pulse retrigg	Pulse retrigger time	$R_{ext} = 1 \text{ k}\Omega, C_{ext} = 0.01 \mu\text{F}$	‡	1.8		‡		‡		μs

[‡] See retriggering data in the application information section.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

			TEST COMPITIONS	T,	λ = 25°C	;	SN54AHC123A		SN74AHC123A		LINIT
			TEST CONDITIONS	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
_	Pulse	CLR		5			5		5		
^I W	duration	A or B trigger		5			5		5		ns
	Dulas natria		$R_{ext} = 1 k\Omega$, $C_{ext} = 100 pF$	‡	59		‡		‡		ns
t _{rr}	Pulse retrigger time	$R_{ext} = 1 \text{ k}\Omega, C_{ext} = 0.01 \mu\text{F}$	‡	1.5		‡		‡		μS	

[‡] See retriggering data in the application information section.



[†] This test is performed with the terminal in the off-state condition.

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switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V \pm 0.3 V (unless otherwise noted) (see Figure 1)

DADAMETED	FROM	то	TEST	T,	ղ = 25°C	;	SN54AH	C123A	SN74AH	C123A	LINUT
PARAMETER	(INPUT)	(OUTPUT)	CONDITIONS	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
^t PLH	A or B	0 0	C: 15 pF		9.5*	20.6*	1*	24*	1	24	20
^t PHL	Aorb	Q or Q	C _L = 15 pF		10.2*	20.6*	1*	24*	1	24	ns
^t PLH	CLD	0 *** 0	C: 15 pF		7.5*	15.8*	1*	18.5*	1	18.5	20
^t PHL	CLR	Q or Q	C _L = 15 pF		9.3*	15.8*	1*	18.5*	1	18.5	ns
^t PLH	CLD trimmer	0 0 7 0	0. 45.5		10*	22.4*	1*	26*	1	26	
^t PHL	CLR trigger	Q or Q	C _L = 15 pF		10.6*	22.4*	1*	26*	1	26	ns
^t PLH	A or B	Q or Q	C		10.5	24.1	1	27.5	1	27.5	20
^t PHL	Aorb	Q or Q	$C_L = 50 pF$		11.8	24.1	1	27.5	1	27.5	ns
^t PLH	CLR	0 0	C: F0.5F		8.9	19.3	1	22	1	22	20
^t PHL	CLR	Q or Q	C _L = 50 pF		10.5	19.3	1	22	1	22	ns
^t PLH	CLR trigger	Q or $\overline{\mathbb{Q}}$	C: F0 pF		11	25.9	1	29.5	1	29.5	20
t _{PHL}	CLK (ligger	QUQ	C _L = 50 pF		12.3	25.9	1	29.5	1	29.5	ns
			$C_L = 50 \text{ pF},$ $C_{ext} = 28 \text{ pF},$ $R_{ext} = 2 \text{ k}\Omega$		182	240		300		300	ns
t _W †		Q or $\overline{\mathbb{Q}}$	$C_L = 50 \text{ pF},$ $C_{ext} = 0.01 \mu\text{F},$ $R_{ext} = 10 k\Omega$	90	100	110	90	110	90	110	μs
			$C_L = 50 \text{ pF},$ $C_{ext} = 0.1 \mu\text{F},$ $R_{ext} = 10 k\Omega$	0.9	1	1.1	0.9	1.1	0.9	1.1	ms
$_{\Delta t_{W}}$ ‡					±1						%

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.
† t_W = Pulse duration at Q and \overline{Q} outputs
‡ Δt_W = Output pulse-duration variation (Q and \overline{Q}) between circuits in same package

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switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

DADAMETED	FROM	то	TEST	Τμ	λ = 25°C	;	SN54AH	C123A	SN74AH	C123A	
PARAMETER	(NPUT)	(OUTPUT)	CONDITIONS	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
t _{PLH}	B	0	0. 45.5		6.5*	12*	1*	14*	1	14	
t _{PHL}	A or B	Q or Q	C _L = 15 pF		7.1*	12*	1*	14*	1	14	ns
^t PLH	CLR	Q or Q	C: 15 pF		5.3*	9.4*	1*	11*	1	11	20
^t PHL	CLR	Q or Q	C _L = 15 pF		6.5*	9.4*	1*	11*	1	11	ns
^t PLH	CLR trigger	Q or Q	C: 15 pF		6.9*	12.9*	1*	15*	1	15	20
^t PHL	CLR ingger	QOIQ	C _L = 15 pF		7.4*	12.9*	1*	15*	1	15	ns
^t PLH	A or B	Q or Q	C _L = 50 pF		7.3	14	1	16	1	16	no
^t PHL	AOIB	QOIQ	CL = 50 pr		8.3	14	1	16	1	16	ns
^t PLH	CLR	Q or Q	C 50 pF		6.3	11.4	1	13	1	13	no
^t PHL	CLK	QOIQ	C _L = 50 pF		7.4	11.4	1	13	1	13	ns
^t PLH	CLR trigger	Q or $\overline{\mathbb{Q}}$	C 50 pF		7.6	14.9	1	17	1	17	no
^t PHL	CLR ingger	QOIQ	C _L = 50 pF		8.7	14.9	1	17	1	17	ns
			$C_L = 50 \text{ pF},$ $C_{ext} = 28 \text{ pF},$ $R_{ext} = 2 \text{ k}\Omega$		167	200		240		240	ns
t _W †		Q or $\overline{\mathbb{Q}}$	$C_L = 50 \text{ pF},$ $C_{ext} = 0.01 \mu\text{F},$ $R_{ext} = 10 k\Omega$	90	100	110	90	110	90	110	μs
			$C_L = 50 \text{ pF},$ $C_{ext} = 0.1 \mu\text{F},$ $R_{ext} = 10 k\Omega$	0.9	1	1.1	0.9	1.1	0.9	1.1	ms
$_{\Delta t_{W}}$ ‡					±1						%

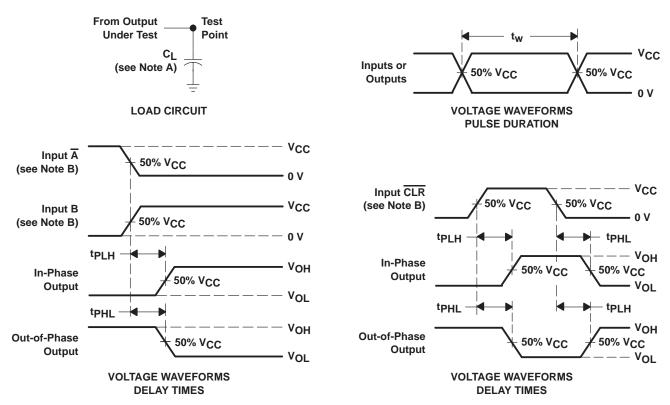
^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.

operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

		PARAMETER	TEST CONDITIONS	TYP	UNIT
ſ	C _{pd}	Power dissipation capacitance	No load	29	pF

[†] t_W = Pulse duration at Q and \overline{Q} outputs ‡ Δt_W = Output pulse-duration variation (Q and \overline{Q}) between circuits in same package

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: $Z_0 = 50 \Omega$, $t_f = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.
- C. The outputs are measured one at a time, with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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APPLICATION INFORMATION

caution in use

To prevent malfunctions due to noise, connect a high-frequency capacitor between V_{CC} and GND, and keep the wiring between the external components and C_{ext} and R_{ext}/C_{ext} terminals as short as possible.

power-down considerations

Large values of C_{ext} can cause problems when powering down the 'AHC123A devices because of the amount of energy stored in the capacitor. When a system containing this device is powered down, the capacitor can discharge from V_{CC} through the protection diodes at pin 2 or pin 14. Current through the input protection diodes must be limited to 30 mA; therefore, the turn-off time of the V_{CC} power supply must not be faster than $t = V_{CC} \times C_{ext}/30$ mA. For example, if $V_{CC} = 5$ V and $C_{ext} = 15$ pF, the V_{CC} supply must turn off no faster than $t = (5 \text{ V}) \times (15 \text{ pF})/30$ mA = 2.5 ns. Usually, this is not a problem because power supplies are heavily filtered and cannot discharge at this rate. When a more rapid decrease of V_{CC} to zero occurs, the 'AHC123A devices can sustain damage. To avoid this possibility, use external clamping diodes.

output pulse duration

The output pulse duration, t_W , is determined primarily by the values of the external capacitance (C_T) and timing resistance (R_T). The timing components are connected as shown in Figure 2.

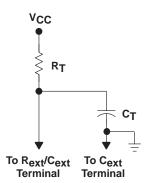


Figure 2. Timing-Component Connections

The pulse duration is given by:

$$t_w = K \times R_T \times C_T$$
 (1) if C_T is ≥ 1000 pF, $K = 1.0$ or if C_T is < 1000 pF, K can be determined from Figure 9

where:

tw = pulse duration in ns

 R_T = external timing resistance in $k\Omega$

C_T = external capacitance in pF

K = multiplier factor

Equation 1 and Figure 3 can be used to determine values for pulse duration, external resistance, and external capacitance.



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APPLICATION INFORMATION

retriggering data

The minimum input retriggering time (t_{MIR}) is the minimum time required after the initial signal before retriggering the input. After t_{MIR} , the device retriggers the output. Experimentally, it also can be shown that to retrigger the output pulse, the two adjacent input signals should be t_{MIR} apart, where $t_{MIR} = 0.30 \times t_{w}$. The retrigger pulse duration is calculated as shown in Figure 3.

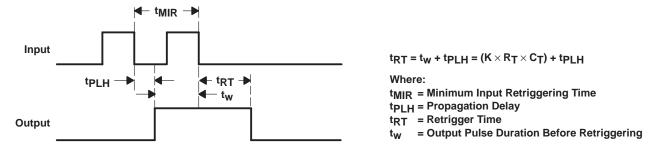
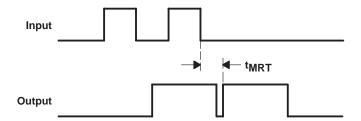


Figure 3. Retrigger Pulse Duration

The minimum value from the end of the input pulse to the beginning of the retriggered output should be approximately 15 ns to ensure a retriggered output (see Figure 4).



 t_{MRT} = Minimum Time Between the End of the Second Input Pulse and the Beginning of the Retriggered Output t_{MRT} = 15 ns

Figure 4. Input/Output Requirements

APPLICATION INFORMATION[†]

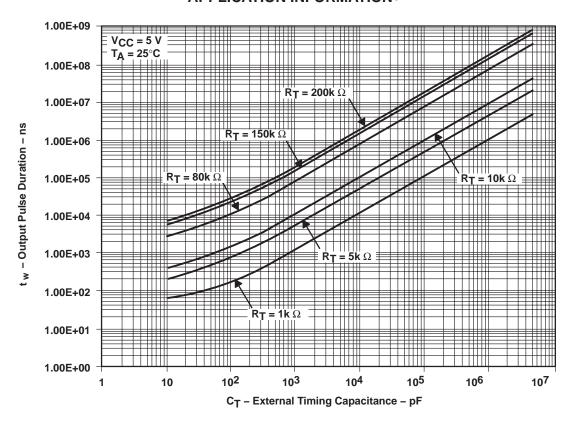


Figure 5. Output Pulse Duration vs External Timing Capacitance

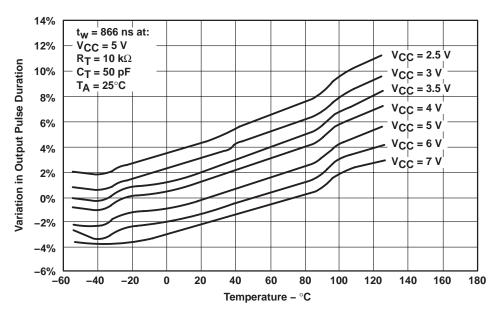
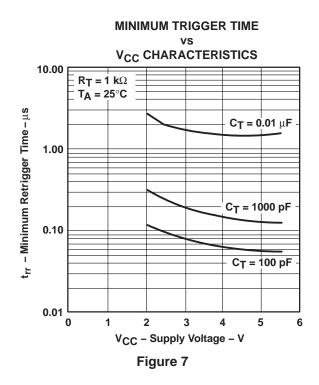


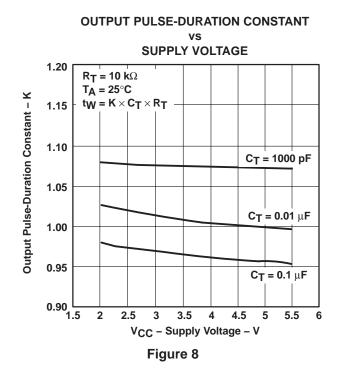
Figure 6. Variations in Output Pulse Duration vs Temperature

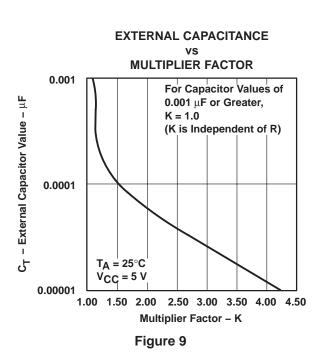
[†] Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

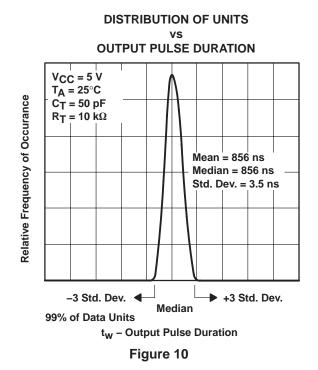


APPLICATION INFORMATION[†]









[†] Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.







10-Jun-2014

PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish (6)	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9860801Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9860801Q2A SNJ54AHC 123AFK	Samples
5962-9860801QEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9860801QE A SNJ54AHC123AJ	Samples
5962-9860801QFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9860801QF A SNJ54AHC123AW	Samples
SN74AHC123AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC123A	Samples
SN74AHC123ADBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA123A	Samples
SN74AHC123ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC123A	Samples
SN74AHC123ADGVR	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA123A	Samples
SN74AHC123ADGVRE4	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA123A	Samples
SN74AHC123ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC123A	Samples
SN74AHC123ADRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC123A	Samples
SN74AHC123ADRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC123A	Samples
SN74AHC123AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74AHC123AN	Samples
SN74AHC123APWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-40 to 85	HA123A	Samples
SN74AHC123APWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA123A	Samples
SN74AHC123APWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA123A	Samples



PACKAGE OPTION ADDENDUM

10-Jun-2014

Orderable Device	Status	Package Type	_	Pins	Package	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
SNJ54AHC123AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9860801Q2A SNJ54AHC 123AFK	Samples
SNJ54AHC123AJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9860801QE A SNJ54AHC123AJ	Samples
SNJ54AHC123AW	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9860801QF A SNJ54AHC123AW	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.



PACKAGE OPTION ADDENDUM

10-Jun-2014

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OTHER QUALIFIED VERSIONS OF SN54AHC123A, SN74AHC123A:

Catalog: SN74AHC123A

● Enhanced Product: SN74AHC123A-EP

Military: SN54AHC123A

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Enhanced Product Supports Defense, Aerospace and Medical Applications
- Military QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

www.ti.com 29-Apr-2014

TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC123ADBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74AHC123ADGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AHC123ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74AHC123APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC123APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC123APWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
SN74AHC123ADBR	SSOP	DB	16	2000	367.0	367.0	38.0	
SN74AHC123ADGVR	TVSOP	DGV	16	2000	367.0	367.0	35.0	
SN74AHC123ADR	SOIC	D	16	2500	333.2	345.9	28.6	
SN74AHC123APWR	TSSOP	PW	16	2000	364.0	364.0	27.0	
SN74AHC123APWR	TSSOP	PW	16	2000	367.0	367.0	35.0	
SN74AHC123APWRG4	TSSOP	PW	16	2000	367.0	367.0	35.0	

14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP2-F16



FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



DGV (R-PDSO-G**)

24 PINS SHOWN

PLASTIC SMALL-OUTLINE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194

D (R-PDS0-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150

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