Silicon N-Channel Power MOSFET

CS16N65F A9H

V_{DSS}	650	V
I_D	16	A
$P_D(T_C=25℃)$	70	W
$R_{DS(ON)Typ}$	0.49	Ω

General Description：

CS16N65F A9H, the silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency. The package form is TO-220F, which accords with the RoHS standard..

TO-220F

1. Gate   2. Drain   3. Source

Features：

- **Fast Switching**
- **Low ON Resistance(Rdson≤0.55Ω)**
- **Low Gate Charge   (Typical Data:54nC)**
- **Low Reverse transfer capacitances(Typical: 18.5pF)**
- **100% Single Pulse avalanche energy Test**

Applications：

Power switch circuit of adaptor and charger.

Inner Equivalent Principium Chart

Absolute （Tc= 25℃ unless otherwise specified）：

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	650	V
I_D	Continuous Drain Current	16	A
	Continuous Drain Current $T_C = 100$ °C	11.5	A
I_{DM} [a1]	Pulsed Drain Current	64	A
V_{GS}	Gate-to-Source Voltage	±30	V
E_{AS} [a2]	Single Pulse Avalanche Energy	800	mJ
E_{AR} [a1]	Avalanche Energy ,Repetitive	90	mJ
I_{AR} [a1]	Avalanche Current	4.2	A
dv/dt [a3]	Peak Diode Recovery dv/dt	5.0	V/ns
P_D	Power Dissipation	70	W
	Derating Factor above 25°C	0.56	W/℃
T_J，T_{stg}	Operating Junction and Storage Temperature Range	150，−55 to 150	℃
T_L	Maximum Temperature for Soldering	300	℃
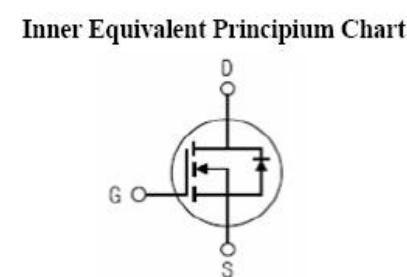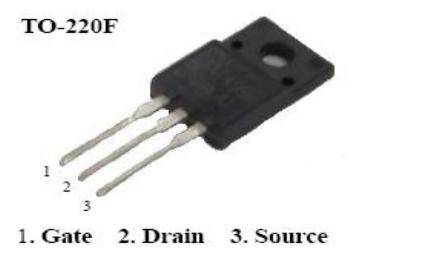
Electrical Characteristics（Tc= 25℃　unless otherwise specified）：

OFF Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	$V_{GS}=0V$, $I_D=250\mu A$	650	--	--	V
$\Delta BV_{DSS}/\Delta T_J$	Bvdss Temperature Coefficient	ID=250uA,Reference2**5**℃	--	0.65	--	V/℃
I_{DSS}	Drain to Source Leakage Current	V_{DS} = 650V, V_{GS}= 0V, T_a = 25℃	--	--	10	μA
		V_{DS} =520V, V_{GS}= 0V, T_a = 125℃			100	
$I_{GSS(F)}$	Gate to Source Forward Leakage	V_{GS}= 30V	--	--	100	nA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	V_{GS} =-30V	--	--	-100	nA

ON Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$	Drain-to-Source On-Resistance	$V_{GS}=10V$,$I_D=8A$	--	0.49	0.55	Ω
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250\mu A$	2.0	--	4.0	V
Pulse width tp≤300μs, δ ≤2%						

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
g_{fs}	Forward Trans conductance	$V_{DS}=15V$, $I_D =8A$	--	15	--	S
C_{iss}	Input Capacitance	$V_{GS} = 0V$ $V_{DS} = 25V$ f = 1.0MHz	--	2450		pF
C_{oss}	Output Capacitance		--	218		
C_{rss}	Reverse Transfer Capacitance		--	18.5		

Resistive Switching Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	$I_D =16A$ $V_{DD} = 325V$ $R_G = 25\Omega$	--	30		ns
tr	Rise Time		--	70		
$t_{d(OFF)}$	Turn-Off Delay Time		--	145		
t_f	Fall Time		--	74		
Q_g	Total Gate Charge	$I_D =16A$ $V_{DD} =325V$ $V_{GS} = 10V$	--	54		nC
Q_{gs}	Gate to Source Charge		--	10	--	
Q_{gd}	Gate to Drain ("Miller")Charge		--	21	--	

Source-Drain Diode Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_S	Continuous Source Current (Body Diode)		--	--	16	A
I_{SM}	Maximum Pulsed Current (Body Diode)		--	--	64	A
V_{SD}	Diode Forward Voltage	I_S=16A,V_{GS}=0V	--	--	1.5	V
trr	Reverse Recovery Time	I_S=16A,T_j = 25°C	--	410	--	ns
Qrr	Reverse Recovery Charge	dI_F/dt=100A/us, V_{GS}=0V	--	3.5	--	μC
Pulse width tp≤300μs, δ ≤2%						

Symbol	Parameter	Typ.	Units
$R_{θJC}$	Junction-to-Case	1.79	℃/W
$R_{θJA}$	Junction-to-Ambient	100	℃/W

[a1]：Repetitive rating; pulse width limited by maximum junction temperature

[a2]：L=10mH, I_D=12.6A, Start T_J=25℃

[a3]：I_{SD} =16A,di/dt ≤200A/us,V_{DD}≤$BV_{DSS,}$ Start T_J=25℃

Characteristics Curve：
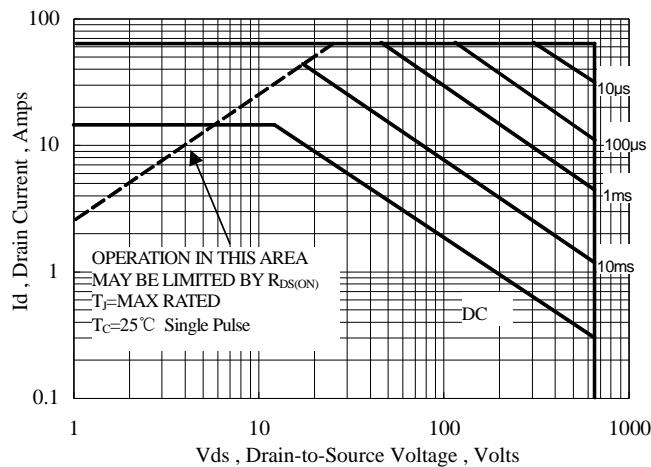
**Figure 1** Maximum Forward Bias Safe Operating Area

(Figure 1 axes: Id , Drain Current , Amps (0.1 to 100) vs Vds , Drain-to-Source Voltage , Volts (1 to 1000). Curves labeled 10μs, 100μs, 1ms, 10ms, DC. Text on figure: OPERATION IN THIS AREA MAY BE LIMITED BY $R_{DS(ON)}$; T_J=MAX RATED; T_C=25℃ Single Pulse)
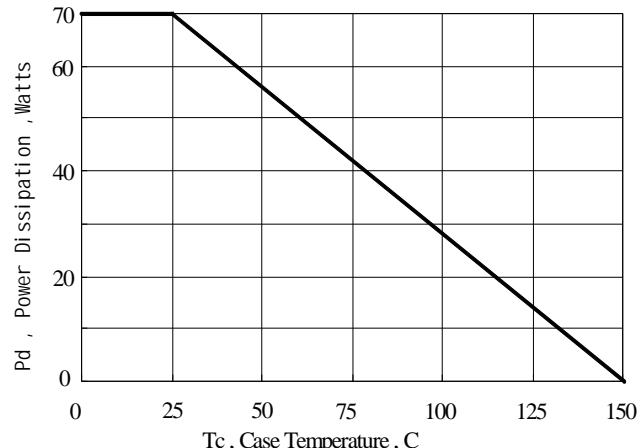
Figure 2 Maximum Power Dissipation vs Case Temperature

(Figure 2 axes: Pd , Power Dissipation , Watts (0 to 70) vs Tc , Case Temperature , C (0 to 150))
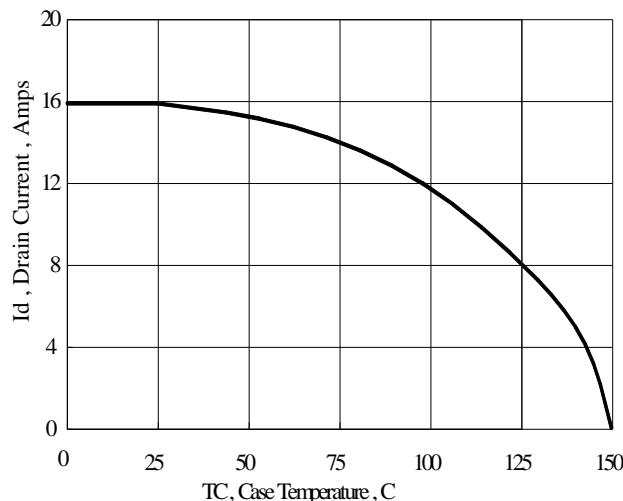
Figure 3 Maximum Continuous Drain Current vs Case Temperature

(Figure 3 axes: Id , Drain Current , Amps (0 to 20) vs TC, Case Temperature , C (0 to 150))
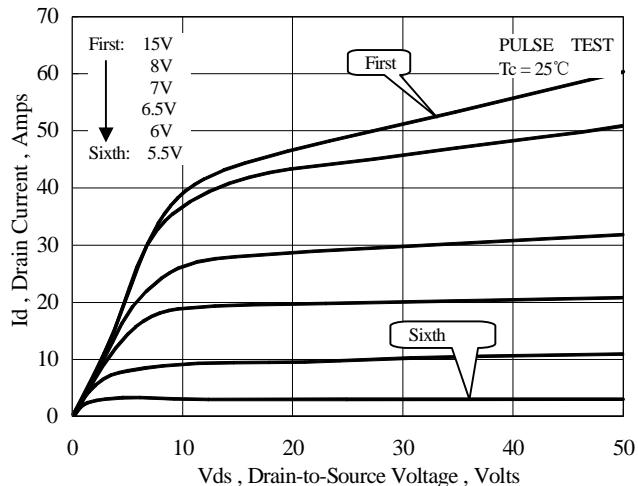
Figure 4 Typical Output Characteristics

(Figure 4 axes: Id , Drain Current , Amps (0 to 70) vs Vds , Drain-to-Source Voltage , Volts (0 to 50). Labels: First: 15V, 8V, 7V, 6.5V, 6V, Sixth: 5.5V. PULSE TEST Tc = 25℃)
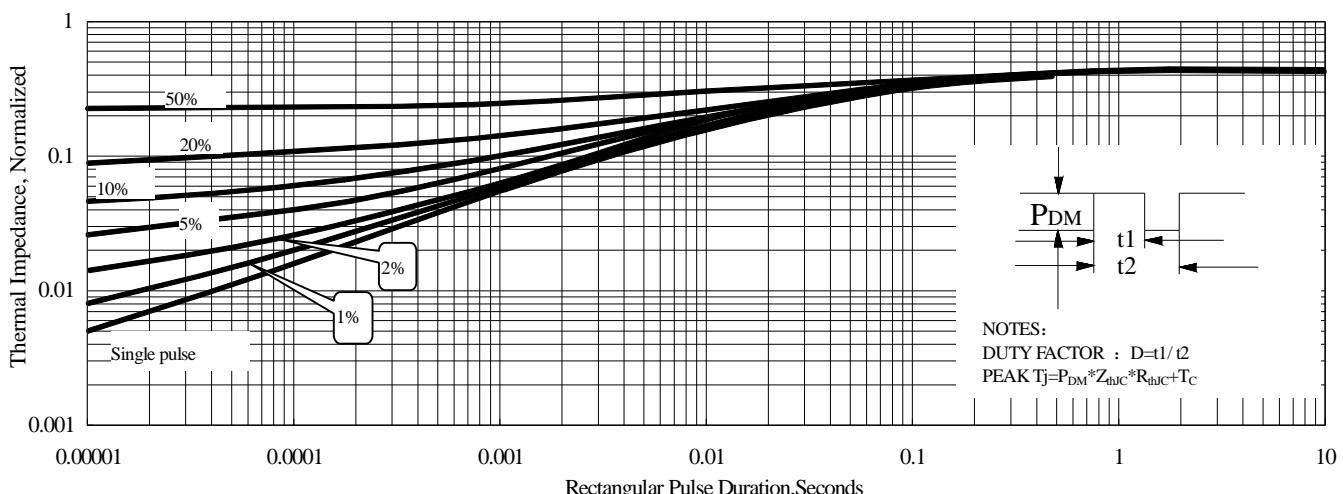
Figure 5 Maximum Effective Thermal Impedance , Junction to Case

(Figure 5 axes: Thermal Impedance, Normalized (0.001 to 1) vs Rectangular Pulse Duration, Seconds (0.00001 to 10). Curves labeled 50%, 20%, 10%, 5%, 2%, 1%, Single pulse.

NOTES：
DUTY FACTOR ： D=t1/t2
PEAK Tj=P_{DM}*Z_{thJC}*R_{thJC}+T_C)
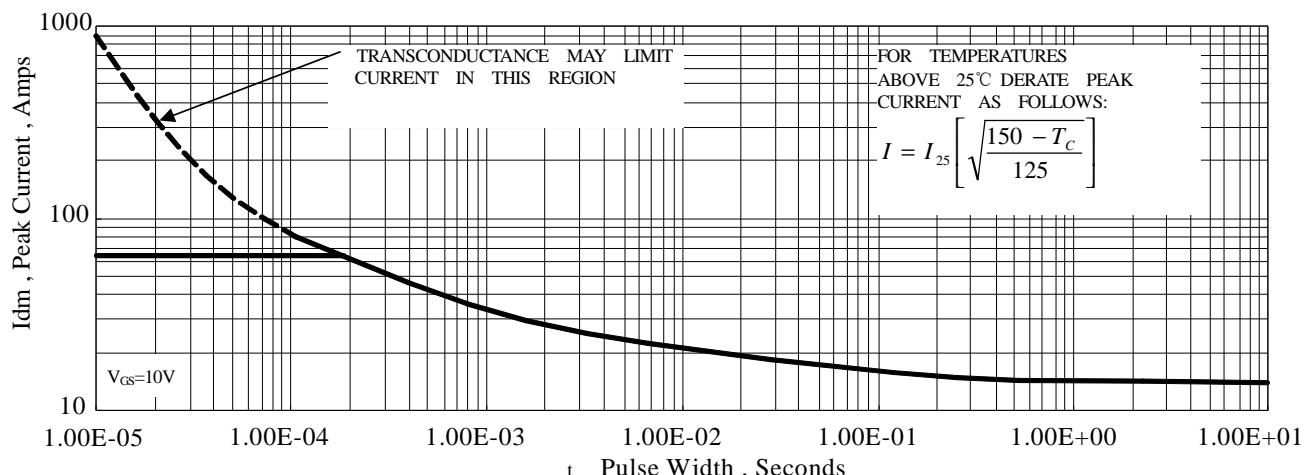
Figure 6 Maximum Peak Current Capability

TRANSCONDUCTANCE MAY LIMIT CURRENT IN THIS REGION

FOR TEMPERATURES ABOVE 25℃ DERATE PEAK CURRENT AS FOLLOWS:

$$I = I_{25}\left[\sqrt{\frac{150 - T_C}{125}}\right]$$

$V_{GS}=10V$
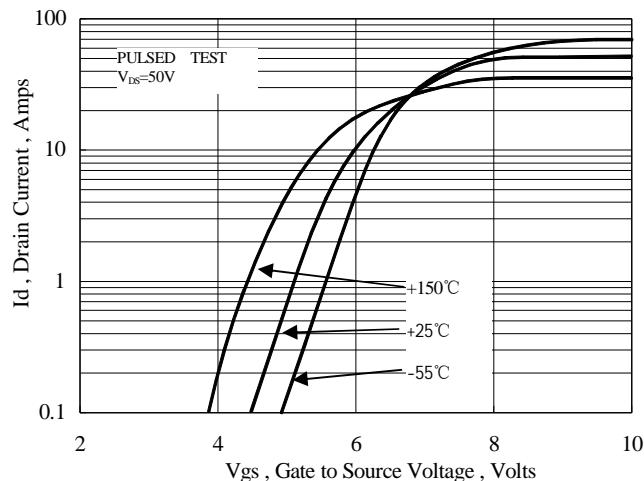
Figure 7 Typical Transfer Characteristics

PULSED TEST
$V_{DS}=50V$

+150℃
+25℃
-55℃
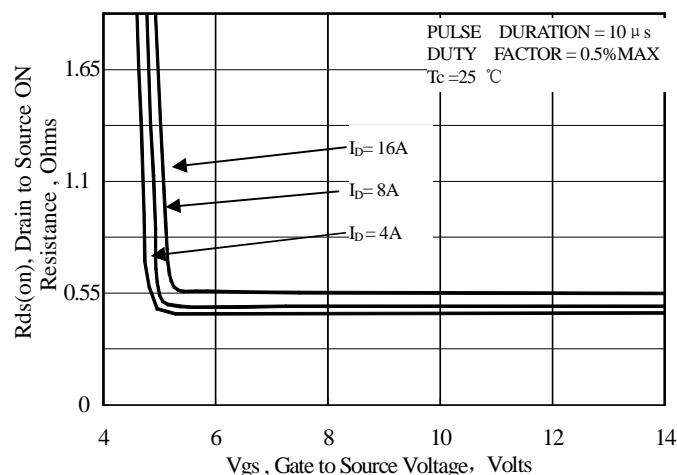
Figure 8 Typical Drain to Source ON Resistance vs Gate Voltage and Drain Current

PULSE DURATION = 10 μs
DUTY FACTOR = 0.5%MAX
Tc =25 ℃

I_D= 16A
I_D= 8A
I_D= 4A
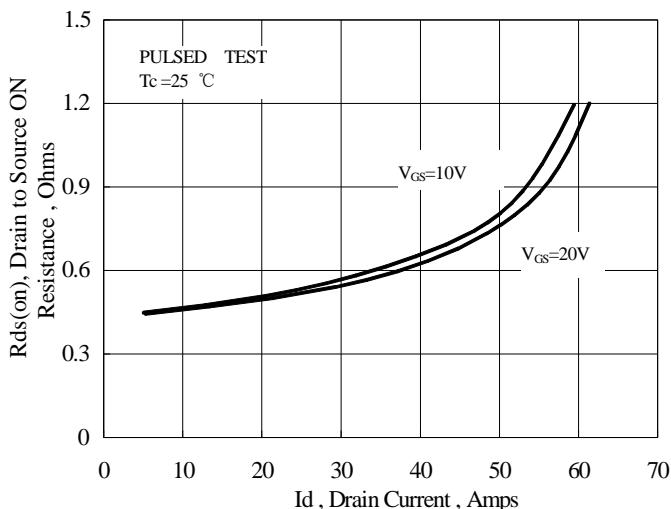
Figure 9 Typical Drain to Source ON Resistance vs Drain Current

PULSED TEST
Tc =25 ℃

$V_{GS}=10V$
$V_{GS}=20V$
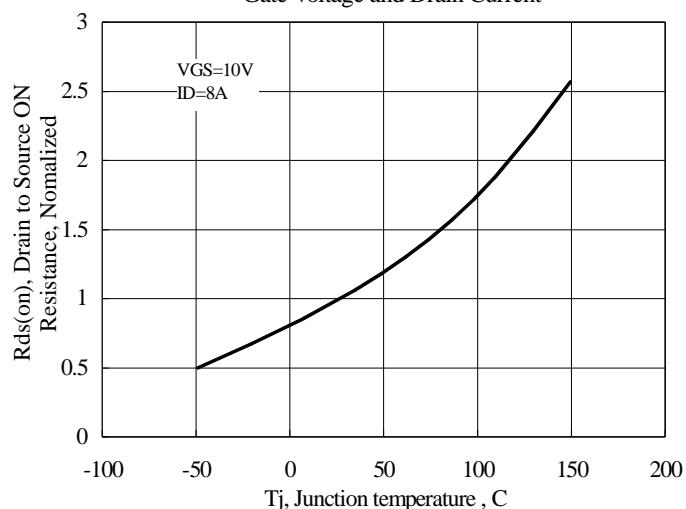
Figure 10 Typical Drian to Source on Resistance vs Junction Temperature

VGS=10V
ID=8A

Figure 11 Typical Theshold Voltage vs Junction Temperature

Figure 12 Typical Breakdown Voltage vs Junction Temperature

Figure 13 Typical Capacitance vs Drain to Source Voltage

Figure 14 Typical Gate Charge vs Gate to Source Voltage

Figure 15 Typical Body Diode Transfer Characteristics

Figure 16 Unclamped Inductive Switching Capability
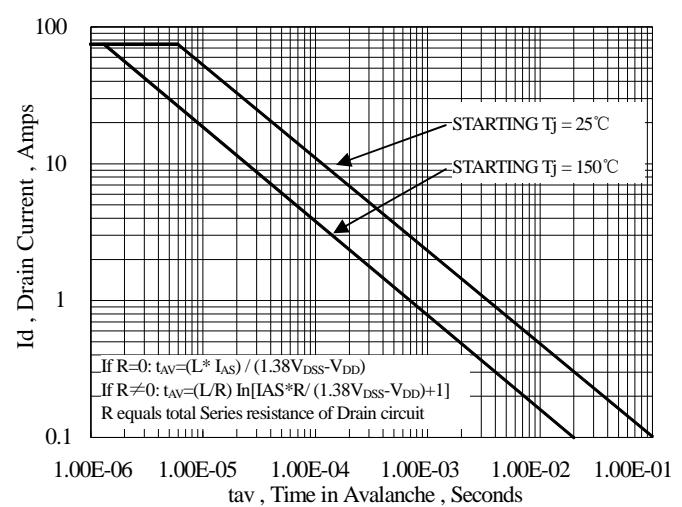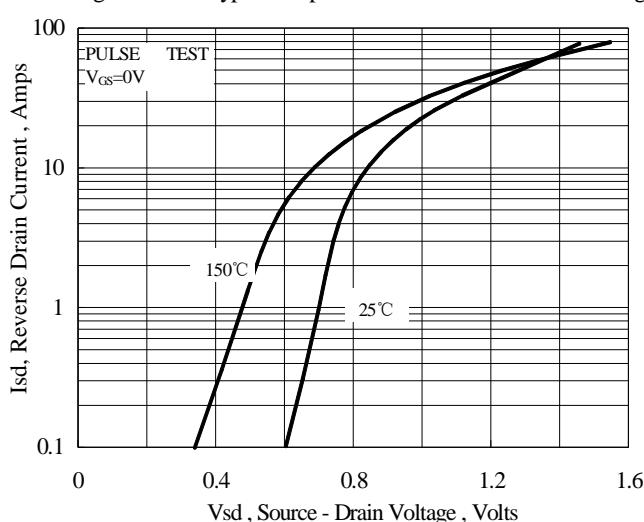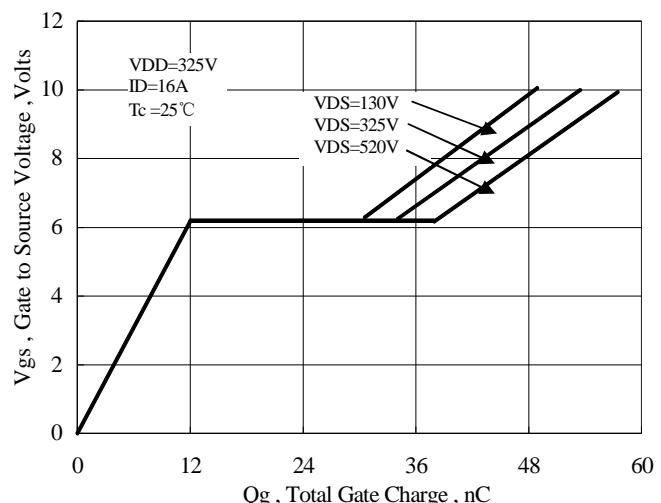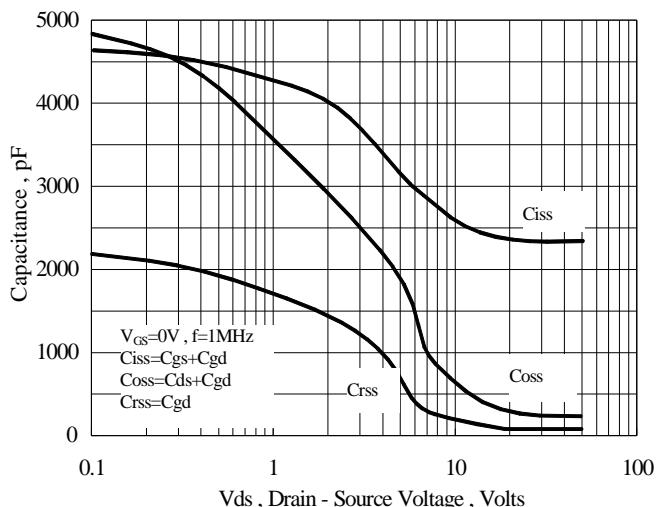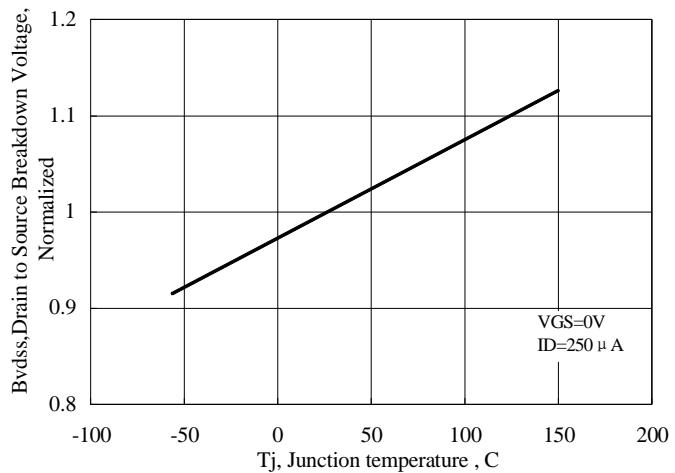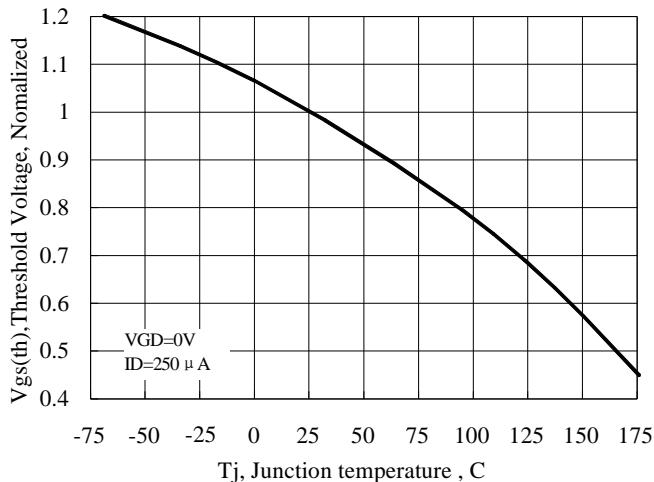
Test Circuit and Waveform
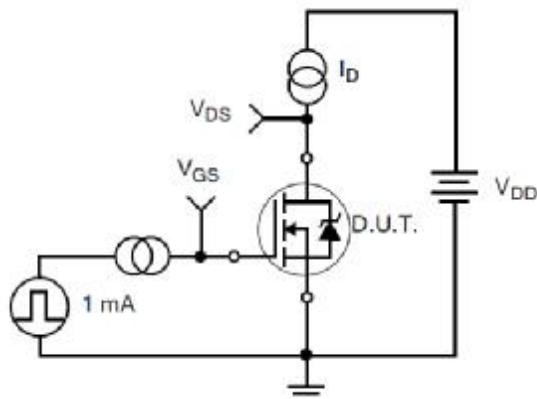

Figure 17. Gate Charge Test Circuit
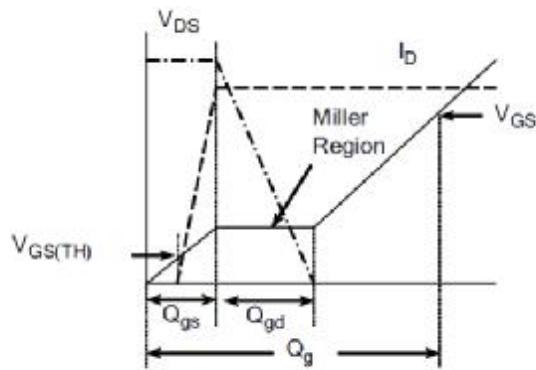

Figure 18. Gate Charge Waveform

Figure 19. Resistive Switching Test Circuit
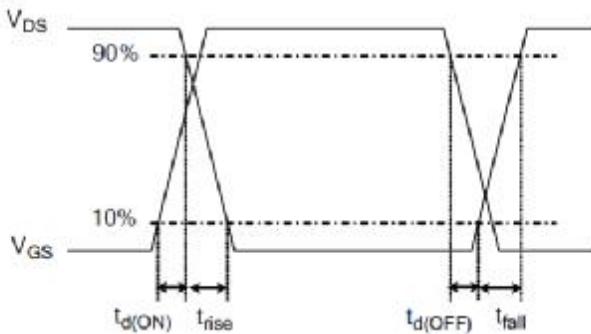
Figure 20. Resistive Switching Waveforms
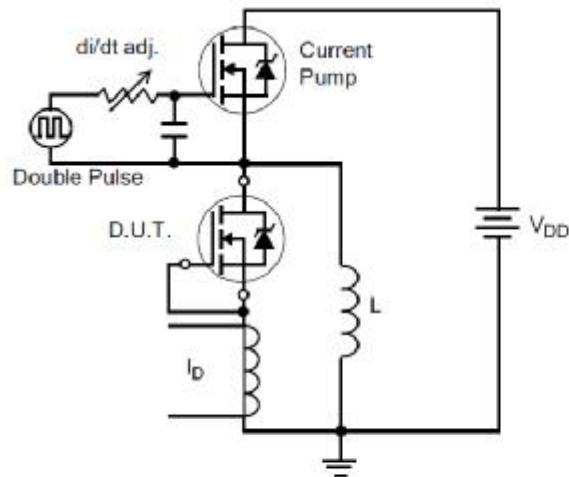
Figure 21. Diode Reverse Recovery Test Circuit
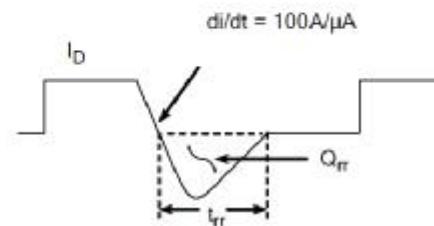
Figure 22. Diode Reverse Recovery Waveform

Figure 23. Unclamped Inductive Switching Test Circuit
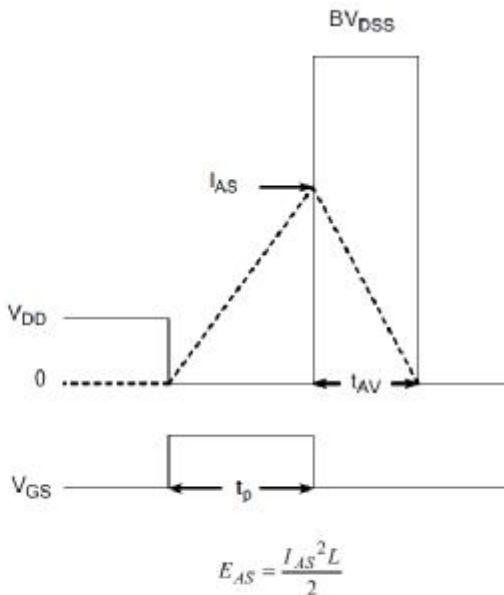
Figure 24. Unclamped Inductive Switching Waveforms

$$E_{AS} = \frac{I_{AS}^2 L}{2}$$

Package Information
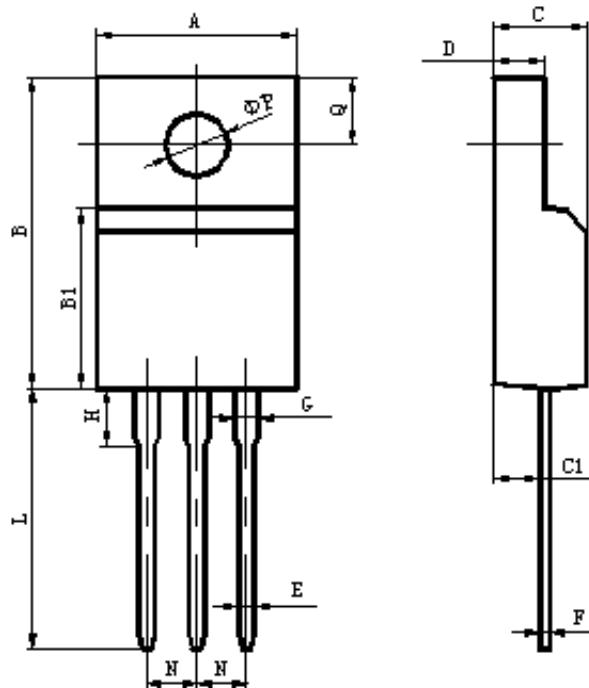
Items	Values(mm)	
	MIN	MAX
A	9.60	10.4
B	15.4	16.2
B1	8.90	9.50
C	4.30	4.90
C1	2.10	3.00
D	2.40	3.00
E	0.60	1.00
F	0.30	0.60
G	1.12	1.42
H	3.40	3.80
	2.40	2.90
L	12.0	14.0
	6.30	7.70
N	2.34	2.74
Q	3.15	3.55
φ P	2.90	3.30

TO-220F Package

The name and content of poisonous and harmful material in products

Part's Name	Hazardous Substance									
	Pb	Hg	Cd	Cr(VI)	PBB	PBDE	DIBP	DEHP	DBP	BBP
Limit	≤0.1%	≤0.1%	≤0.01%	≤0.1%	≤0.1%	≤0.1%	≤0.1%	≤0.1%	≤0.1%	≤0.1%
Lead Frame	○	○	○	○	○	○	○	○	○	○
Molding	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
Wire Bonding	○	○	○	○	○	○	○	○	○	○
Solder	✕	○	○	○	○	○	○	○	○	○
Note	○：Means the hazardous material is under the criterion of SJ/T11363-2006. ✕：Means the hazardous material exceeds the criterion of SJ/T11363-2006. The plumbum element of solder exist in products presently, but within the allowed range of Eurogroup's RoHS.									

Warnings

1. Exceeding the maximum ratings of the device in performance may cause damage to the device, even the permanent failure, which may affect the dependability of the machine. It is suggested to be used under 80 percent of the maximum ratings of the device.

2. When installing the heat sink, please pay attention to the torsional moment and the smoothness of the heat sink.

3. VDMOSFETs is the device which is sensitive to the static electricity, it is necessary to protect the device from being damaged by the static electricity when using it.

4. This publication is made by Huajing Microelectronics and subject to regular change without notice.