Precision RRO Operational Amplifier

Features

- **Low Offset Voltage: 100μV Maximum**
- **Low Drift: ±0.9μV/°C**
- **High EMIRR: 84dB at 900MHz**
- **Low Noise: 19 nV/√Hz(f= 1kHz)**
- **Wide Input Voltage Range: 0 to ±14V**
- **Wide Supply Range: ±1.35V to ±18V**
- **Low Input Bias Current: 40pA Typical**
- **Below-Ground (V-) Input Capability to -0.3V**
- **Rail-to-Rail Output Voltage Range**
- **Unit Gain Stable**
- **–40°C to 125°C Operation Range**
- **Robust 3kV – HBM and 2kV – CDM ESD Rating**
- **Direct or Update Replacement for OP07C,OP07D and OP37**

Applications

- Wireless Base Station Control Circuits
- Optical network Control Circuits
- I/V Converter
- Temperature Measurements
- Strain Gage Amplifier
- Medical Instrumentation

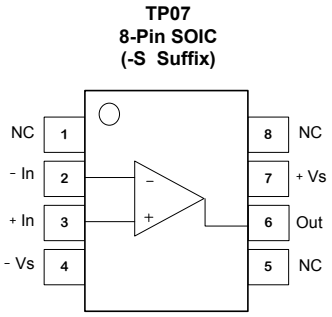
Description

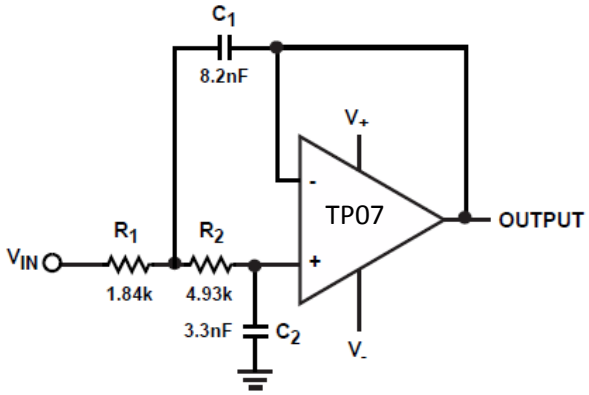
The TP07 has very low input offset voltage (100μV maximum) that is obtained by trimming at the wafer stage. The low offset voltages generally eliminate any need for external nulling. The TP07 also features low input bias current (±40 pA) and high open-loop gain (118 dB). The low offset and high open-loop gain make the TP07 particularly useful for high gain instrumentation applications.

The wide input voltage range of ±14 V minimum combined with a high CMRR of 126 dB and high input impedance provide high accuracy in the non-inverting circuit configuration. Excellent linearity and gain accuracy can be maintained even at high closed-loop gains. Stability of offsets and gain with time or variations in temperature is excellent. The accuracy and stability of the TP07, even at high gain, made the TP07 an industry standard for instrumentation applications.

The TP07 is single channel available in 8-pin SOIC package.

Pin Configuration (Top View)





SALLEN-KEY LOW PASS FILTER (10kHz)

Order Information

Model Name	Order Number	Package	Transport Media, Quantity	Marking Information
TP07	TP07-SR	8-Pin SOIC	Tape and Reel, 4,000	D41S

Absolute Maximum Ratings Note 1

Supply Voltage: $V^+ – V^–$ Note 2.....40.0V
Input Voltage..... $V^–$ – 0.3 to V^+ + 0.3
Input Current: +IN, –IN Note 3..... ±20mA
Output Current: OUT..... ±35mA
Output Short-Circuit Duration Note 4..... Indefinite

Current at Supply Pins……..... ±60mA
Operating Temperature Range.....–40°C to 125°C
Maximum Junction Temperature..... 150°C
Storage Temperature Range..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 260°C

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The op amp supplies must be established simultaneously, with, or before, the application of any input signals.

Note 3: The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 500mV beyond the power supply, the input current should be limited to less than 10mA.

Note 4: A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted. Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	MIL-STD-883H Method 3015.8	3	kV
CDM	Charged Device Model ESD	JEDEC-EIA/JESD22-C101E	2	kV

Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Pin SOIC	158	43	°C/W

Electrical Characteristics

The specifications are at T_A = 27°C, V_{SUPPLY} = ±15V, V_{CM} = V_{OUT} =0V, R_L = 2kΩ, C_L =100pF. Unless otherwise noted.

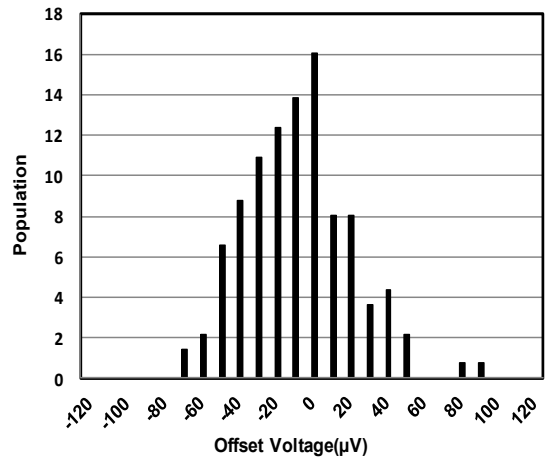
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = V_{DD}/2	-100	±50	+100	μV
V_{OS} TC	Input Offset Voltage Drift	-40°C to 125°C		0.9		μV/°C
I_B	Input Bias Current	T_A = 27 °C		40		pA
		T_A = 85 °C		550		pA
		T_A = 125 °C		7.7		nA
I_{OS}	Input Offset Current			0.001		pA
V_n	Input Voltage Noise	f = 0.1Hz to 10Hz		2.35		μV_{RMS}
e_n	Input Voltage Noise Density	f = 1kHz		19		nV/√Hz
C_{IN}	Input Capacitance	Differential Common Mode		4 2.5		pF
CMRR	Common Mode Rejection Ratio	V_{CM} = -5.6V to 4V		120		dB
V_{CM}	Common-mode Input Voltage Range		V^- -0.3		V^+-2.0	V
PSRR	Power Supply Rejection Ratio			130		dB
A_{VOL}	Open-Loop Large Signal Gain	R_{LOAD} = 2kΩ	100	118		dB
V_{OL}, V_{OH}	Output Swing from Supply Rail	R_{LOAD} = 100kΩ		50		mV
R_{OUT}	Closed-Loop Output Impedance	G = 1, f =1kHz, I_{OUT} = 0		0.01		Ω
R_O	Open-Loop Output Impedance	f = 1kHz, I_{OUT} = 0		125		Ω
I_{SC}	Output Short-Circuit Current	Sink or source current		35		mA
V_{DD}	Supply Voltage		2.7		36	V
I_Q	Quiescent Current per Amplifier			2.2		mA
PM	Phase Margin	R_{LOAD} = 2kΩ, C_{LOAD} = 100pF		55		°
GM	Gain Margin	R_{LOAD} = 2kΩ, C_{LOAD} = 100pF		8		dB
GBWP	Gain-Bandwidth Product	f = 1kHz		1		MHz
SR	Slew Rate	A_V = 1, V_{OUT} = 0V to 10V, C_{LOAD} = 100pF, R_{LOAD} = 2kΩ		6		V/μs
FPBW	Full Power Bandwidth Note 1			210		kHz
t_S	Settling Time, 0.1% Settling Time, 0.01%	A_V = –1, 10V Step		1 1		μs
X_{talk}	Channel Separation	f = 1kHz, R_L = 2kΩ		110		dB

Note 1: Full power bandwidth is calculated from the slew rate FPBW = SR/π • V_{P-P}

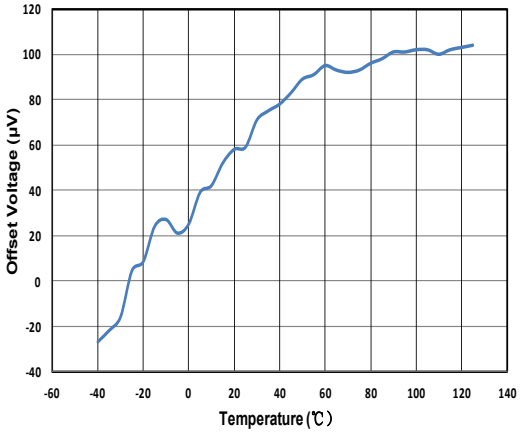
Typical Performance Characteristics

V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified.

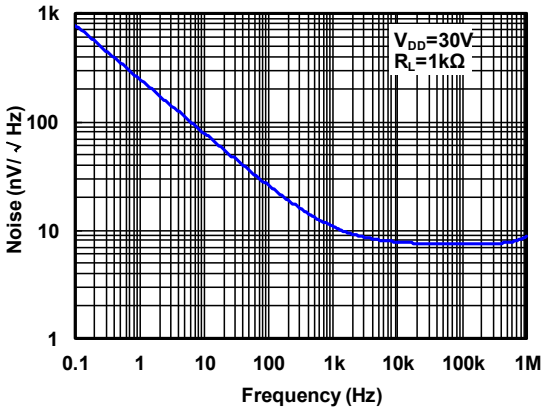
Offset Voltage Production Distribution



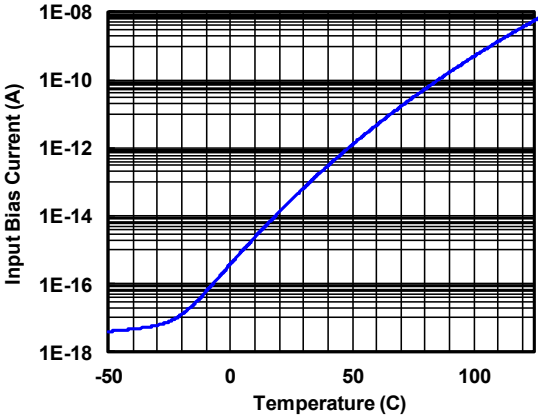
Offset Voltage vs. Temperature



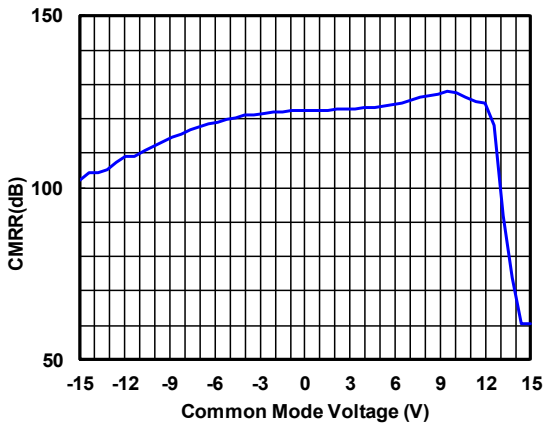
Input Voltage Noise Spectral Density



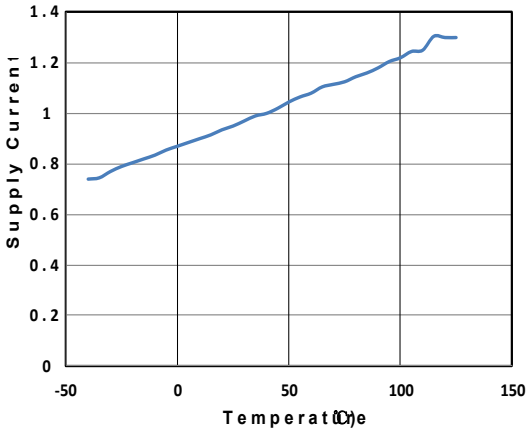
Input Bias Current vs. Temperature



Common Mode Rejection Ratio



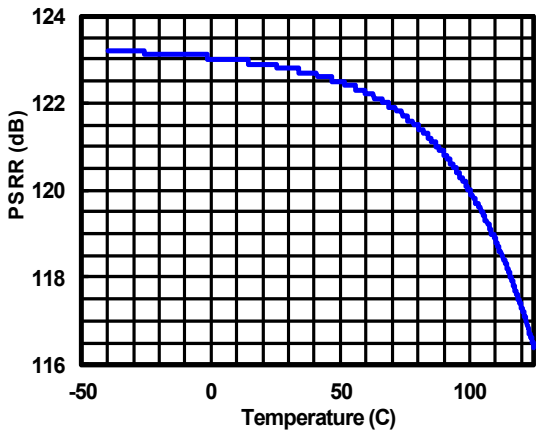
Quiescent Current vs. Temperature



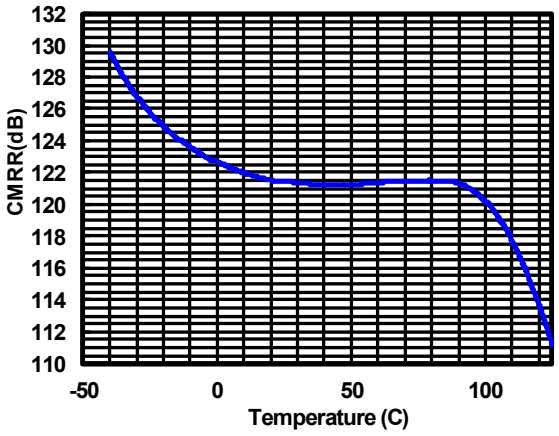
Typical Performance Characteristics

V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified. (Continued)

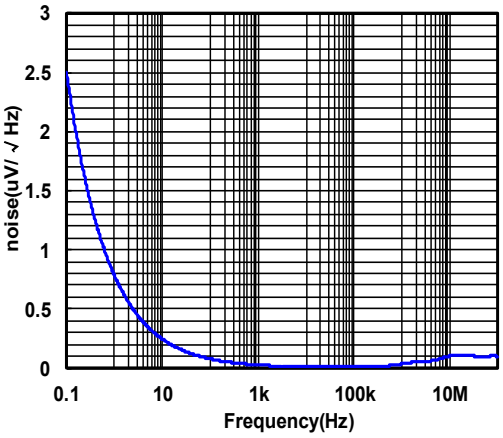
Power-Supply Rejection Ratio vs. Temperature



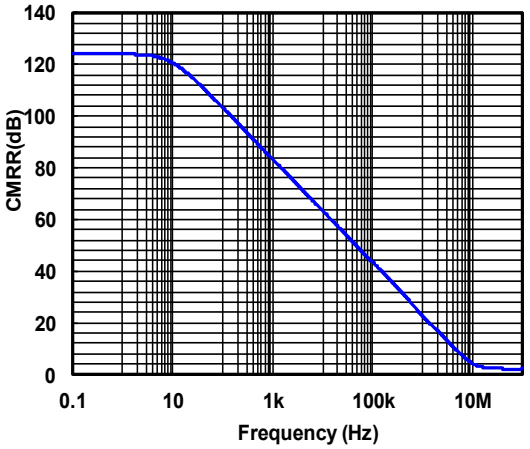
CMRR vs. Temperature



Voltage Noise Spectral Density vs. Frequency



CMRR vs. Frequency



Pin Functions

-IN: Inverting Input of the Amplifier. Voltage range of this pin can go from V^- to (V^+ - 2.0V).

+IN: Non-Inverting Input of Amplifier. This pin has the same voltage range as –IN.

V+ or $+V_S$: Positive Power Supply. Typically the voltage is from 2.7V to 36V. Split supplies are possible as long as the voltage between V+ and V– is between 2.7V and 36V. A bypass capacitor of 0.1µF as close to the part as possible should be used between power supply pins or between supply pins and ground.

V^- or ^-V_S: Negative Power Supply. It is normally tied to ground. It can also be tied to a voltage other than ground as long as the voltage between V^+ and V^- is from 2.7V to 36V. If it is not connected to ground, bypass it with a capacitor of 0.1µF as close to the part as possible.

OUT: Amplifier Output. The voltage range extends to within milli-volts of each supply rail.

N/C: No connection.

Operation

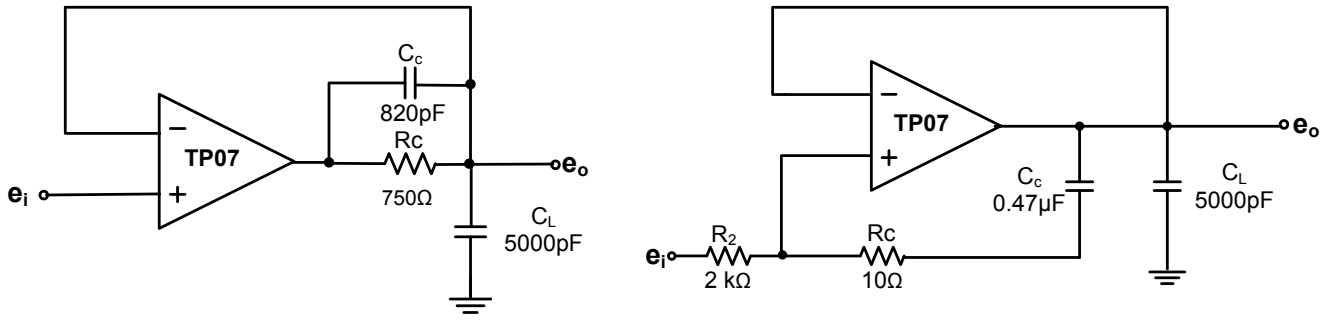
The TP07 has input signal range from V^- to (V^+ – 2.0V). The output can extend all the way to the supply rails. The input stage is comprised of a PMOS differential amplifier. The Class-AB control buffer and output bias stage uses a proprietary compensation technique to take full advantage of the process technology to drive very high capacitive loads. This is evident from the transient over shoot measurement plots in the Typical Performance Characteristics.

Applications Information

Driving Large Capacitive Load

The TP07 provides stable operation with load capacitance of up to 100 pF and ±10 V swings; larger capacitances should be decoupled with a 50Ω decoupling resistor.

Stray thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can degrade drift performance. Therefore, best operation is obtained when both input contacts are maintained at the same temperature, preferably close to the package temperature.



Driving Large Capacitive Loads

PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5pA of current to flow,

which is greater than the TP07 OPA's input bias current at +27°C (±40pA, typical). It is recommended to use multi-layer PCB layout and route the OPA's -IN and +IN signal under the PCB surface.

The effective way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 2 for Inverting Gain application.

1. For Non-Inverting Gain and Unity-Gain Buffer:
   a) Connect the non-inverting pin (V_{IN}+) to the input with a wire that does not touch the PCB surface.
   b) Connect the guard ring to the inverting input pin (V_{IN}–). This biases the guard ring to the Common Mode input voltage.
2. For Inverting Gain and Trans-impedance Gain Amplifiers (convert current to voltage, such as photo detectors):
   a) Connect the guard ring to the non-inverting input pin (V_{IN}+). This biases the guard ring to the same reference voltage as the op-amp (e.g., V_{DD}/2 or ground).
   b) Connect the inverting pin (V_{IN}–) to the input with a wire that does not touch the PCB surface.

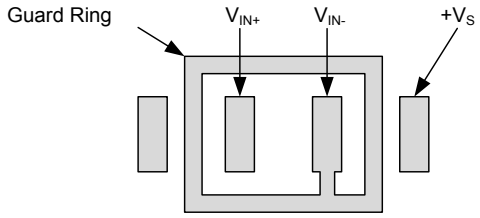


Figure 2 The Layout of Guard Ring

Ground Sensing and Rail to Rail Output

The TP07 family has excellent output drive capability. It drives 2kΩ load directly with good THD performance. The output stage is a rail-to-rail topology that is capable of swinging to within 50mV of either rail.

The maximum output current is a function of total supply voltage. As the supply voltage to the amplifier increases, the output current capability also increases. Attention must be paid to keep the junction temperature of the IC below 150°C when the output is in continuous short-circuit. The output of the amplifier has reverse-biased ESD diodes connected to each supply. The output should not be forced more than 0.3V beyond either supply, otherwise current will flow through these diodes.

Power Supply Layout and Bypass

The TP07 OPA's power supply pin (V_{DD} for single-supply) should have a local bypass capacitor (i.e., 0.01μF to 0.1μF) within 2mm for good high frequency performance. It can also use a bulk capacitor (i.e., 1μF or larger) within 100mm to provide large, slow currents. This bulk capacitor can be shared with other analog parts.

Ground layout improves performance by decreasing the amount of stray capacitance and noise at the OPA's inputs and outputs. To decrease stray capacitance, minimize PC board lengths and resistor leads, and place external components as close to the op amps' pins as possible.

Proper Board Layout

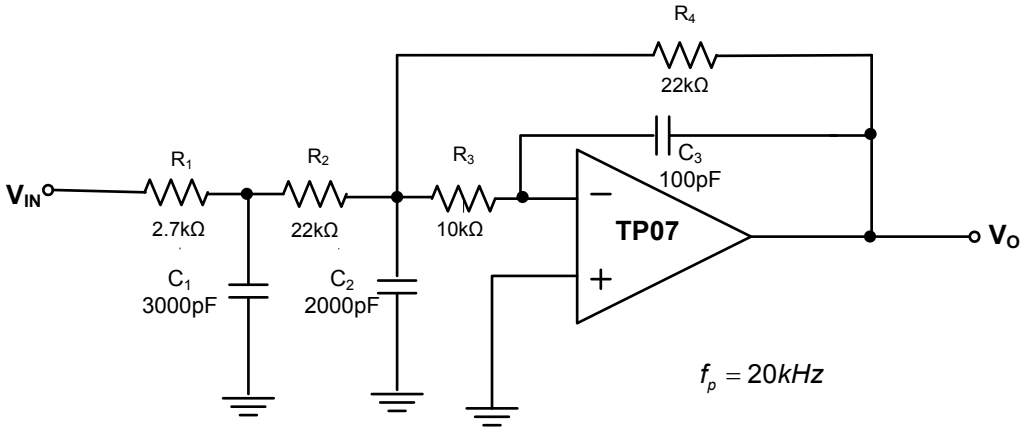
To ensure optimum performance at the PCB level, care must be taken in the design of the board layout. To avoid leakage currents, the surface of the board should be kept clean and free of moisture. Coating the surface creates a barrier to moisture accumulation and helps reduce parasitic resistance on the board.

Keeping supply traces short and properly bypassing the power supplies minimizes power supply disturbances due to output current variation, such as when driving an ac signal into a heavy load. Bypass capacitors should be connected as closely as possible to the device supply pins. Stray capacitances are a concern at the outputs and the inputs of the amplifier. It is recommended that signal traces be kept at least 5mm from supply lines to minimize coupling.

A variation in temperature across the PCB can cause a mismatch in the Seebeck voltages at solder joints and other points where dissimilar metals are in contact, resulting in thermal voltage errors. To minimize these thermocouple effects, orient resistors so heat sources warm both ends equally. Input signal paths should contain matching numbers and types of components, where possible to match the number and type of thermocouple junctions. For example, dummy components such as zero value resistors can be used to match real resistors in the opposite input path. Matching components should be located in close proximity and should be oriented in the same manner. Ensure leads

are of equal length so that thermal conduction is in equilibrium. Keep heat sources on the PCB as far away from amplifier input circuitry as is practical.

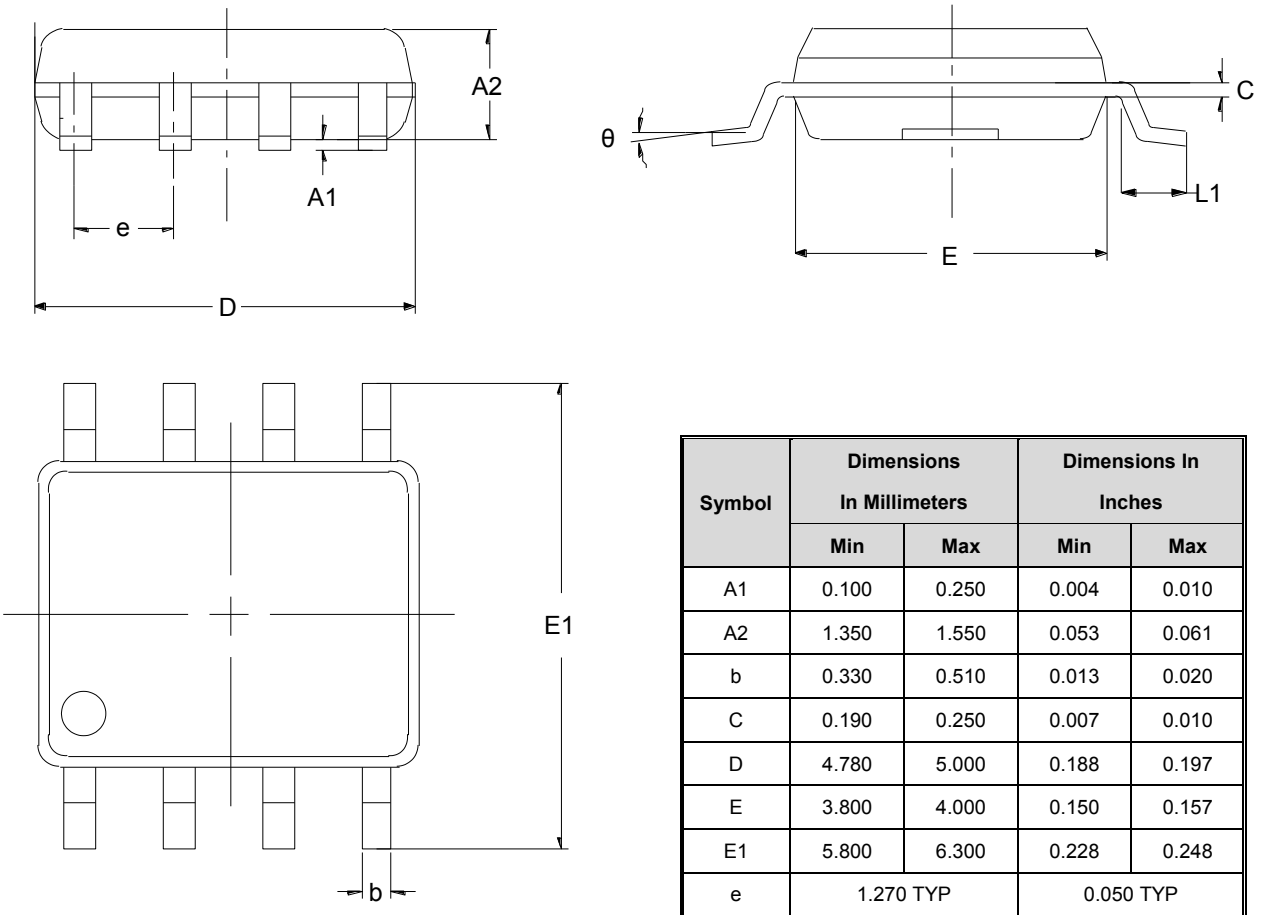
The use of a ground plane is highly recommended. A ground plane reduces EMI noise and also helps to maintain a constant temperature across the circuit board.



Three-Pole Low-Pass Filter

Package Outline Dimensions

SO-8 (SOIC-8)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270 TYP		0.050 TYP	
L1	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°