

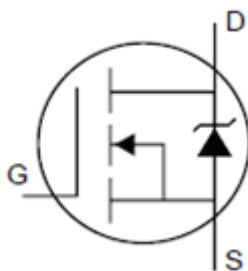
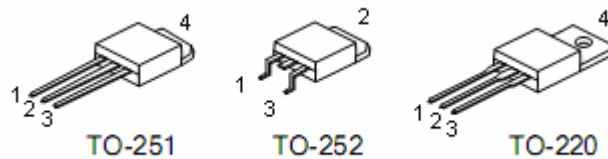
## 1.Features

- Advanced trench process technology
- High density cell design for ultra low on-resistance
- Fully characterized avalanche voltage and current

## 2.Applications

- $V_{DSS}=30V, R_{DS(on)}=6.5m\Omega, I_D=50A$
- $V_{ds}=30V$
- $R_{DS(on)}=6.5m\Omega(\text{Max.}), V_{GS}@10V, I_{ds}@30A$
- $R_{DS(on)}=9.5m\Omega(\text{Max.}), V_{GS}@4.5V, I_{ds}@30A$

## 3. Pin configuration



Pin	Function
1	Gate
2	Drain
3	Source
4	Drain

#### 4. Maximum ratings and thermal characteristics

(Ta=25°C, unless otherwise notes)

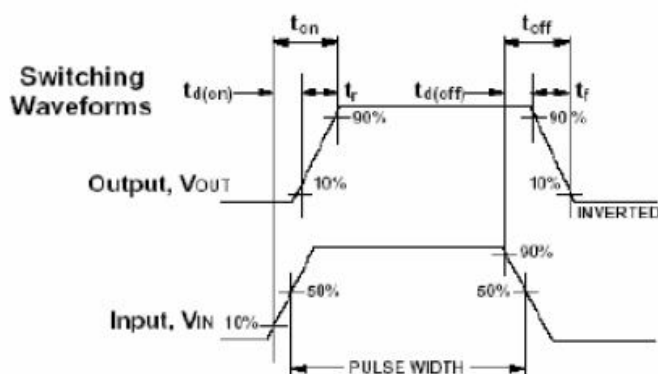
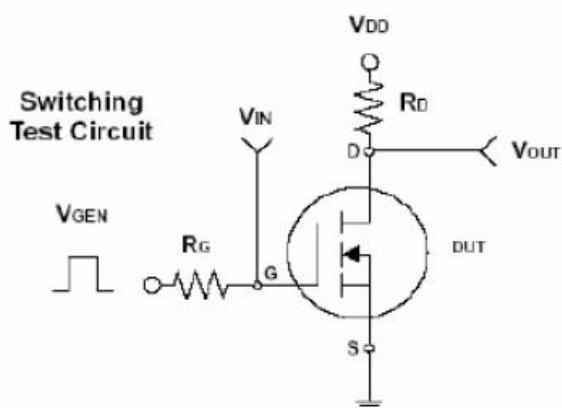
Rating	Symbol	Value	Unit	
Drain-source voltage	$V_{DS}$	30	V	
Gate-source voltage	$V_{GS}$	+20	V	
Continuous drain current	$I_D$	50	A	
Pulsed drain current <sup>1)</sup>	$I_{DM}$	200	A	
Maximum power dissipation	$T_A=25^\circ\text{C}$	$P_D$	60	W
	$T_A=75^\circ\text{C}$	$P_D$	23	W
Operating junction and storage temperature range	$T_J/T_{STG}$	-55 to 150	°C	
Junction-to-case thermal resistance	$R_{\theta JC}$	1.8	°C/W	
Junction-to ambient thermal resistance (PCB mount) <sup>2)</sup>	$R_{\theta JA}$	50	°C/W	

Note: 1. Repetitive rating; pulse width limited by the maximum junction temperature  
 2. 1-in<sup>2</sup> 2oz Cu PCB board  
 3. Guaranteed by design; not subject to production testing

#### 5. Ordering information

Part number	Package
KIA50N03	TO-251, TO-252, TO-220

#### 6. Typical application circuit



## 7. Electrical characteristics

(Ta=25°C, unless otherwise notes)

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Units
<b>Static</b>						
Drain-source breakdown voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	30	-	-	V
Drain-source on-state resistance	$R_{DS(ON)}$	$V_{GS}=4.5V, I_D=30A$	-	9.5	13.0	mΩ
		$V_{GS}=10V, I_D=30A$	-	6.5	9.0	mΩ
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	1	1.8	3	V
Forward transconductance	$g_{fs}$	$V_{DS}=15V, I_D=15A$	-	12	-	S
Zero gate voltage drain current	$I_{DSS}$	$V_{DS}=25V, V_{GS}=0V$	-	-	1	μA
Gate-source forward leakage	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	±100	nA
<b>Dynamic<sup>3)</sup></b>						
Total gate charge	$Q_g$	$I_D=35A$ $V_{DS}=15V$ $V_{GS}=10V$	-	10	25	nC
Gate-source charge	$Q_{gs}$		-	3.5	10	nC
Gate-drain ("miller") charge	$Q_{gd}$		-	3	65	nC
Turn-on delay time	$t_{d(off)}$	$V_{DD}=15V$ $I_D=1A$ $R_G=6\Omega$ $R_L=15\Omega$ $V_{GEN}=10V$	-	12	-	ns
Rise time	$t_r$		-	4	-	ns
Turn-off delay time	$t_{d(off)}$		-	32	-	ns
Fall time	$t_f$		-	6	-	ns
Input capacitance	$C_{iss}$	$V_{GS}=0V$ $V_{DS}=15V$ $f=1.0MHz$	-	1180	-	pF
Output capacitance	$C_{oss}$		-	270	-	pF
Reverse transfer capacitance	$C_{rss}$		-	145	-	pF

### Source-drain diode

Parameter	Symbol	Test condition	Min.	Typ.	Max.	Units
Diode forward voltage	$V_{SD}$	$I_S=20A, V_{GS}=0V$	-	0.87	1.5	V
Max. diode forward current	$I_S$		-	-	20	A

Notes: Pulse width ≤ 300μs, duty cycle ≤ 2%