# SN74AUP1T34 1 位单向电压电平转换器

## 1 特性

- 0.9V 至 3.6V 的宽运行 VCC 范围
- 均衡的传播延迟：$t_{PLH} = t_{PHL}$ （1.8V 至 3.3V 转换时的典型值）
- 低静态功耗：最大 5μA ICC
- ±6mA 输出驱动（电压为 3V 时）
- $I_{off}$ 支持部分掉电模式运行
- VCC 隔离特性 – 如果 $V_{CCA}$ 输入接地，则 B 端口处于高阻态
- 输入滞后可实现输入转换和输入上更好的开关噪声抗扰度
- 静电放电 (ESD) 保护性能超过 JESD 22 规范要求
- 5000V 人体放电模式 (A114-A)
- 锁断性能超过 100mA，符合 JESD 78 II 类规范的要求

## 2 应用

- 企业
- 工业
- 个人电子产品
- 电信

## 3 说明

SN74AUP1T34 器件是一款 1 位非反向转换器，使用两条独立的可配置电源轨。它是一个从 A 至 B 的单向转换器。A 端口设计用来跟踪 $V_{CCA}$。$V_{CCA}$可接受从 0.9V 到 3.6V 范围内的电源电压。B 端口设计用于跟踪 $V_{CCB}$。$V_{CCB}$可接受从 0.9V 至 3.6V 间的电源电压值。这可实现 1V，1.2V，1.5V，1.8V，2.5V 和 3.3V 电压节点间的低压转换。此外，SN74AUP1T34 完全 适用于 使用 $I_{off}$ 的局部掉电应用。$I_{off}$ 电路会禁用输出，从而在器件掉电时防止电流回流损坏器件。

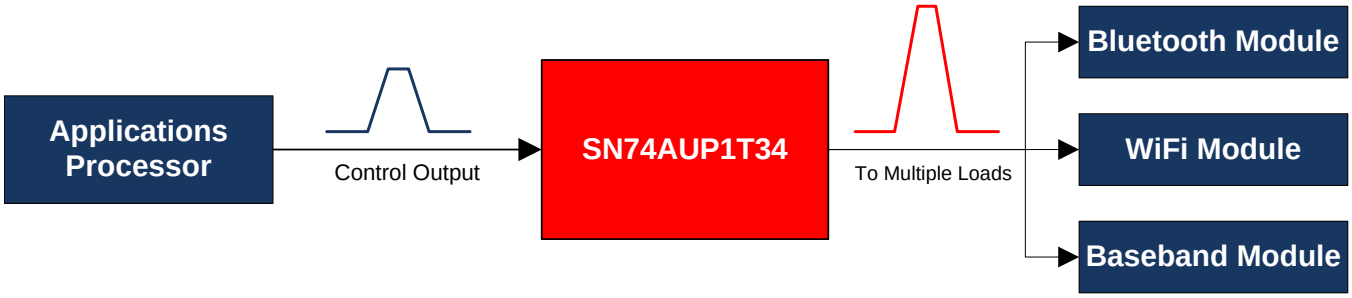
VCC 隔离特性确保了在 $V_{CCA}$输入在 GND 上时，B 端口处于高阻抗状态。如果 $V_{CCB}$输入在 GND 上，到 A 侧的任一输入都不会导致泄漏电流，即使在悬空状态时也是如此。

器件信息(1)

| 器件型号 | 封装 | 封装尺寸（标称值） |
|---|---|---|
| SN74AUP1T34 | SC70 (5) | 2.00mm × 1.25mm |
| | SON (6) | 1.45mm x 1.00mm |
| | | 1.00mm x 1.00mm |

(1) 要了解所有可用封装，请参见数据表末尾的可订购产品附录。

示例应用



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## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

**Changes from Revision D (April 2016) to Revision E** **Page**

- Changed pin A number From: 3 To: 2 and GND From: 2 To: 3 for the SC70 package in the *Pin Configuration and Functions* ... 3

**Changes from Revision C (May 2013) to Revision D** **Page**

- 已添加 *ESD 额定值*表，*特性 描述*部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分。 ... 1
- 已删除*订购信息*表 ... 1

**Changes from Revision B (July 2012) to Revision C** **Page**

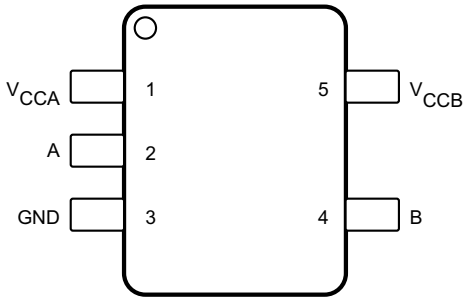
- 已添加特性：VCC 隔离特性 – 如果 $V_{CCA}$ 输入接地，则 B 端口处于高阻态。 ... 1
- Updated PIN FUNCTIONS table. ... 3
- Deleted $I_{OZ}$ PARAMETER from RECOMMENDED OPERATION CONDITIONS. ... 4
- Added $V_{MI}$ and $V_{MO}$ equations to Wavefrom 1 graphic. ... 8
- Added FUNCTION TABLE. ... 10

**Changes from Revision A (June 2012) to Revision B** **Page**

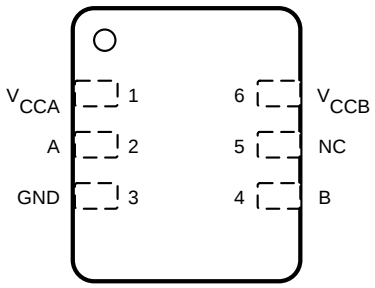
- 已删除特性：输出使能特性方便用户禁用输出，从而降低功耗。 ... 1

# 5 Pin Configuration and Functions

**DCK Package**
**5-Pin SC70**
**Top View**




**DRY or DSF Package**
**6-Pin SON**
**Top Through View**




**Pin Functions**

| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | SC70 | SON | | |
| A | 2 | 2 | I | Input Port |
| B | 4 | 4 | O | Output Port |
| GND | 3 | 3 | — | Ground |
| $V_{CCA}$ | 1 | 1 | — | Input Port DC Power Supply |
| $V_{CCB}$ | 5 | 6 | — | Output Port DC Power Supply |
| NC | — | 5 | — | No Connect. Leave floating. |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CCA}$, $V_{CCB}$ | Supply voltage | | –0.3 | 4 | V |
| $V_I$ | Input voltage | | –0.5 | 4.6 | V |
| | | | –0.5 | 4.6 | |
| | | | –0.5 | 4.6 | |
| $V_O$ | Voltage applied to any output in the high-impedance or power-off state | | –0.5 | 4.6 | V |
| | | | –0.5 | 4.6 | |
| | Voltage applied to any output in the high or low state | | –0.5 | 4.6 | V |
| | | | –0.5 | 4.6 | |
| $I_{IK}$ | Input clamp current | $V_I$ < 0 V | | –50 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0 V | | –50 | mA |
| $I_O$ | Continuous output current | | | ±50 | mA |
| | Continuous current through VCCA or GND | | | ±100 | mA |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1) | 5000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 (2) | 750 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | VCCA | VCCB | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{CCA}$, $V_{CCB}$ | Supply voltage | | | | | 0.9 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | | | 0.9 V to 1.95 V | 0.9 to 1.95V | 0.65 × $V_{CCA}$ | | V |
| | | | | 2.3 V to 2.7 V | 0.9 to 3.6V | 1.6 | | |
| | | | | 3 V to 3.6 V | 0.9 to 3.6V | 2 | | |
| $V_{IL}$ | Low-level input voltage | | | 0.9 V | 0.9 to 1.95V | | 0.3 × $V_{CCA}$ | V |
| | | | | 1 V to 1.95 V | 0.9 to 1.95V | | 0.35 × $V_{CCA}$ | |
| | | | | 2.3 V to 2.7 V | 0.9 to 3.6V | | 0.7 | |
| | | | | 3 V to 3.6 V | 0.9 to 3.6V | | 0.9 | |
| Δt/Δv | Input transition rise or fall rate | | | 3 V to 3.6 V | 0.9 to 3.6V | | 200 | ns/V |
| $T_A$ | Operating free-air temperature | | | | | –40 | 85 | °C |
| $V_{OH}$ | | $I_{OH}$ = –100 µA | $V_I = V_{IH}$ | 0.9 V to 3.6 V | 0.9 V to 3.6 V | VCCB – 0.2 | | V |
| | | $I_{OH}$ = –0.25 mA | | 0.9 V 1 V | 0.9 V 1V | 0.75 × VCCB | | |
| | | $I_{OH}$ = –1.5 mA | | 1.2 V | 1.2 V | 1 | | |
| | | $I_{OH}$ = –2 mA | | 1.65 V | 1.65 V | 1.32 | | |
| | | $I_{OH}$ = –3 mA | | 2.3 V | 2.3 V | 1.9 | | |
| | | $I_{OH}$ = –6 mA | | 3 V | 3 V | 2.72 | | |
| $V_{OL}$ | | $I_{OL}$ = 100 µA | $V_I = V_{IL}$ | 0.9 V to 3.6 V | 0.9 V to 3.6 V | | 0.1 | V |
| | | $I_{OL}$ = 0.25 mA | | 0.9 V to 1 V | 0.9 V 1V | | 0.1 | |
| | | $I_{OL}$ = 1.5 mA | | 1.2 V | 1.2 V | | 0.3 × VCCB | |
| | | $I_{OL}$ = 2 mA | | 1.65 V | 1.65 V | | 0.31 | |
| | | $I_{OL}$ = 3 mA | | 2.3 V | 2.3 V | | 0.31 | |
| | | $I_{OL}$ = 6 mA | | 3 V | 3 V | | 0.31 | |
| $I_I$ | Control inputs | $V_I$ = VCCA or GND | | 0.9 V to 3.6 V | 0.9 V to 3.6 V | | ±1 | µA |
| $I_{off}$ | A or B port | VI or VO = 0 to 3.6 V | | 0 V | 0 V to 3.6 V | | ±5 | µA |
| | | | | 0 V to 3.6 V | 0 V | | ±5 | |
| $I_{CCA}$ | | VI = VCCI or GND, IO = 0 mA | | 0.9 V to 3.6 V | 0.9 V to 3.6 V | | 5 | µA |
| | | | | 0.9 V to 3.6 V | VCCA | | 2 | |
| | | | | 0 V | 0 V to 3.6 V | | 1 | |
| | | | | 0 V to 3.6 V | 0 V | | 1 | |
| $I_{CCB}$ | | VI = VCCI or GND, IO = 0 mA | | 0.9 V to 3.6 V | 0.9 V to 3.6 V | | 5 | µA |
| | | | | 0.9 V to 3.6 V | VCCA | | 2 | |
| | | | | 0 V | 0 V to 3.6 V | | 1 | |
| | | | | 0 V to 3.6 V | 0 V | | 1 | |
| $I_{CCA}$ + $I_{CCB}$ | | VI = VCCI or GND, IO = 0 mA | | 0.9 V to 3.6 V | 0.9 V to 3.6 V | | 5.2 | µA |
| $C_i$ | Control inputs | VI = 3.3 V or GND | | 3.3 V | 3.3 V | | 4 | pF |
| $C_{io}$ | A or B port | VO = 3.3 V or GND | | 0 V | 3.3 V | | 7 | pF |

## 6.4 Thermal Information

| THERMAL METRIC[1] | | SN74AUP1T34 | | | UNIT |
|---|---|---|---|---|---|
| | | DCK (SC70) | DRY (SON) | DSF (SON) | |
| | | 5 PINS | 6 PINS | 6 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 300.8 | 338.5 | 367.1 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 141.3 | 240.4 | 188.8 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 77.3 | 224.6 | 274.6 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 12.6 | 86.8 | 24.1 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 76.5 | 221.4 | 273.1 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 6.5 AC Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | $C_L$ | VCCA | VCCB | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}/t_{PHL}$ | 5 pF | 0.9 V | VCCB = 0.9 V | | 25 | | ns |
| | | | VCCB = 1.2 V | | 18 | | |
| | | | VCCB = 1.65 V | | 16.2 | | |
| | | | VCCB = 2.3 V | | 16.3 | | |
| | | | VCCB = 3 V | | 16.8 | | |
| | 5 pF | 1.2 V | VCCB = 0.9 V | | | 42.5 | |
| | | | VCCB = 1.2 V | | | 24.9 | |
| | | | VCCB = 1.65 V | | | 23.2 | |
| | | | VCCB = 2.3 V | | | 22.6 | |
| | | | VCCB = 3 V | | | 22.5 | |
| | 5 pF | 1.65 V | VCCB = 0.9 V | | | 40 | |
| | | | VCCB = 1.2 V | | | 10.7 | |
| | | | VCCB = 1.65 V | | | 8.84 | |
| | | | VCCB = 2.3 V | | | 8.08 | |
| | | | VCCB = 3 V | | | 7.88 | |
| | 5 pF | 2.3 V | VCCB = 0.9 V | | | 41.3 | |
| | | | VCCB = 1.2 V | | | 8.02 | |
| | | | VCCB = 1.65 V | | | 5.73 | |
| | | | VCCB = 2.3 V | | | 4.92 | |
| | | | VCCB = 3 V | | | 4.2 | |
| | 5 pF | 3 V | VCCB = 0.9 V | | | 42.5 | |
| | | | VCCB = 1.2 V | | | 7.61 | |
| | | | VCCB = 1.65 V | | | 4.5 | |
| | | | VCCB = 2.3 V | | | 3.65 | |
| | | | VCCB = 3 V | | | 3.39 | |

## AC Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | $C_L$ | VCCA | VCCB | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}/t_{PHL}$ | 10 pF | 0.9 V | VCCB = 0.9 V | | 28.9 | | ns |
| | | | VCCB = 1.2 V | | 19.8 | | |
| | | | VCCB = 1.65 V | | 17.9 | | |
| | | | VCCB = 2.3 V | | 18 | | |
| | | | VCCB = 3 V | | 18.5 | | |
| | 10 pF | 1.2 V | VCCB = 0.9 V | | | 43.22 | |
| | | | VCCB = 1.2 V | | | 12.33 | |
| | | | VCCB = 1.65 V | | | 9.57 | |
| | | | VCCB = 2.3 V | | | 8.81 | |
| | | | VCCB = 3 V | | | 8.61 | |
| | 10 pF | 1.65 V | VCCB = 0.9 V | | | 40.44 | |
| | | | VCCB = 1.2 V | | | 9.21 | |
| | | | VCCB = 1.65 V | | | 6.57 | |
| | | | VCCB = 2.3 V | | | 5.5 | |
| | | | VCCB = 3 V | | | 4.73 | |
| | 10 pF | 2.3 V | VCCB = 0.9 V | | | 41.56 | |
| | | | VCCB = 1.2 V | | | 8.3 | |
| | | | VCCB = 1.65 V | | | 5.54 | |
| | | | VCCB = 2.3 V | | | 4.42 | |
| | | | VCCB = 3 V | | | 4.01 | |
| | 10 pF | 3 V | VCCB = 0.9 V | | | 42.81 | |
| | | | VCCB = 1.2 V | | | 7.87 | |
| | | | VCCB = 1.65 V | | | 4.55 | |
| | | | VCCB = 2.3 V | | | 3.8 | |
| | | | VCCB = 3 V | | | 3.36 | |

## AC Electrical Characteristics (continued)

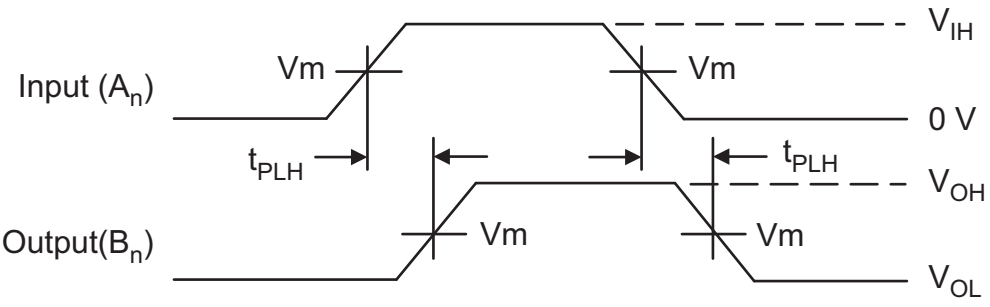
over operating free-air temperature range (unless otherwise noted)

| PARAMETER | $C_L$ | VCCA | VCCB | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}/t_{PHL}$ | 15 pF | 0.9 V | VCCB = 0.9 V | | 30.6 | | ns |
| | | | VCCB = 1.2 V | | 21.6 | | |
| | | | VCCB = 1.65 V | | 19.6 | | |
| | | | VCCB = 2.3 V | | 19.7 | | |
| | | | VCCB = 3 V | | 20.3 | | |
| | 15 pF | 1.2 V | VCCB = 0.9 V | | | 43.87 | |
| | | | VCCB = 1.2 V | | | 12.98 | |
| | | | VCCB = 1.65 V | | | 10.3 | |
| | | | VCCB = 2.3 V | | | 9.54 | |
| | | | VCCB = 3 V | | | 9.34 | |
| | 15 pF | 1.65 V | VCCB = 0.9 V | | | 40.78 | |
| | | | VCCB = 1.2 V | | | 9.59 | |
| | | | VCCB = 1.65 V | | | 6.95 | |
| | | | VCCB = 2.3 V | | | 5.87 | |
| | | | VCCB = 3 V | | | 5.07 | |
| | 15 pF | 2.3 V | VCCB = 0.9 V | | | 41.79 | |
| | | | VCCB = 1.2 V | | | 8.55 | |
| | | | VCCB = 1.65 V | | | 5.8 | |
| | | | VCCB = 2.3 V | | | 4.68 | |
| | | | VCCB = 3 V | | | 4.27 | |
| | 15 pF | 3 V | VCCB = 0.9 V | | | 43.09 | |
| | | | VCCB = 1.2 V | | | 8.16 | |
| | | | VCCB = 1.65 V | | | 4.84 | |
| | | | VCCB = 2.3 V | | | 4.09 | |
| | | | VCCB = 3 V | | | 3.65 | |

## AC Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | $C_L$ | VCCA | VCCB | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}/t_{PHL}$ | 30 pF | 0.9 V | VCCB = 0.9 V | | 32.1 | | ns |
| | | | VCCB = 1.2 V | | 21.3 | | |
| | | | VCCB = 1.65 V | | 18.7 | | |
| | | | VCCB = 2.3 V | | 18 | | |
| | | | VCCB = 3 V | | 18.3 | | |
| | 30 pF | 1.2 V | VCCB = 0.9 V | | | 45.65 | |
| | | | VCCB = 1.2 V | | | 14.76 | |
| | | | VCCB = 1.65 V | | | 12.37 | |
| | | | VCCB = 2.3 V | | | 11.61 | |
| | | | VCCB = 3 V | | | 11.41 | |
| | 30 pF | 1.65 V | VCCB = 0.9 V | | | 41.72 | |
| | | | VCCB = 1.2 V | | | 10.65 | |
| | | | VCCB = 1.65 V | | | 8.01 | |
| | | | VCCB = 2.3 V | | | 6.94 | |
| | | | VCCB = 3 V | | | 5.99 | |
| | 30 pF | 2.3 V | VCCB = 0.9 V | | | 42.44 | |
| | | | VCCB = 1.2 V | | | 9.26 | |
| | | | VCCB = 1.65 V | | | 6.51 | |
| | | | VCCB = 2.3 V | | | 5.39 | |
| | | | VCCB = 3 V | | | 4.97 | |
| | 30 pF | 3 V | VCCB = 0.9 V | | | 43.69 | |
| | | | VCCB = 1.2 V | | | 8.8 | |
| | | | VCCB = 1.65 V | | | 5.48 | |
| | | | VCCB = 2.3 V | | | 4.72 | |
| | | | VCCB = 3 V | | | 4.28 | |




$V_{MI} = V_{IH}/2$; $V_{MO} = V_{CCB}/2$

$t_R = t_F$ = 2.0 ns, 10% to 90%; f = 1 MHz; $t_W$ = 500 ns

**Figure 1. Waveform 1 – Propagation Delays**

## 6.6 Typical Characteristics

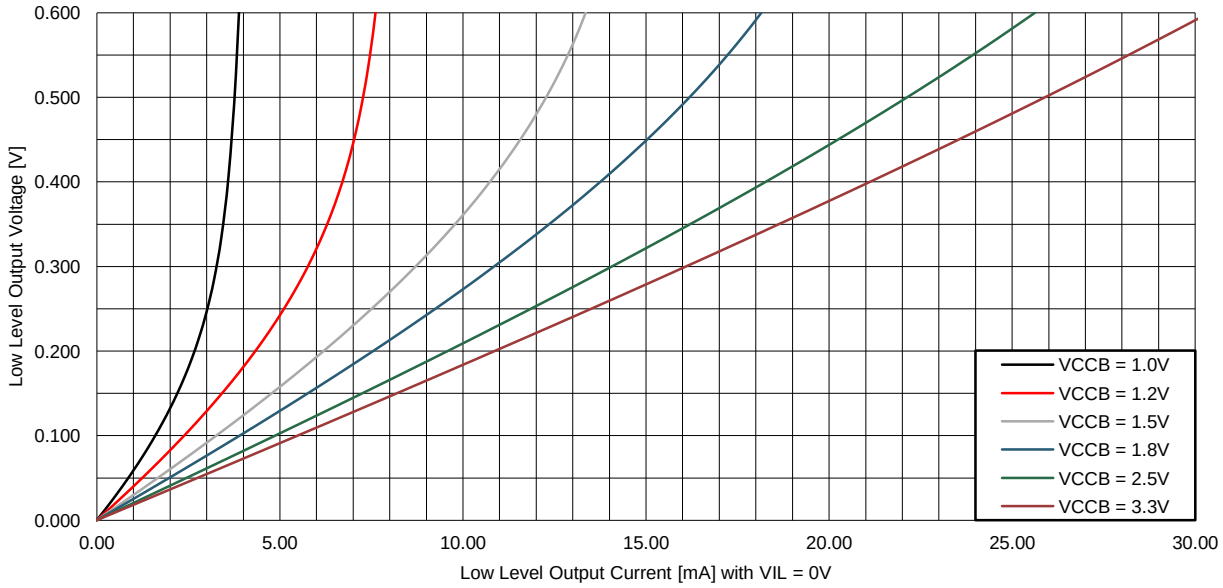
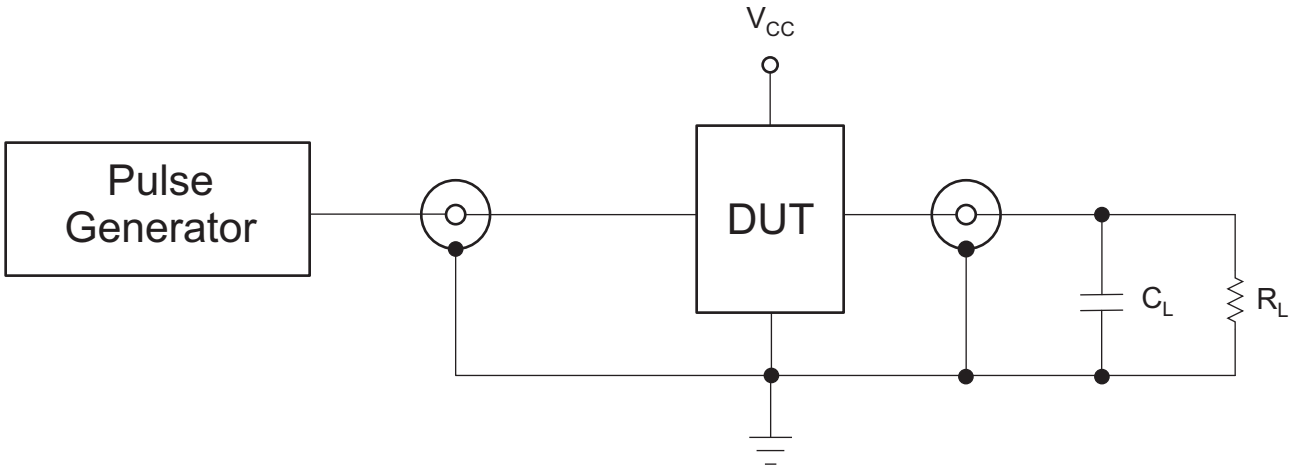



**Figure 2. Low Level Output Voltage vs Low Level Output Current**

## 7 Parameter Measurement Information




**TEST**

$t_{PLH}$, $t_{PHL}$

$C_L$ = 5 pF, 10 pF, 15 pF, 30 pF or equivalent (includes probe and jig capacitance)

$R_L$ = 1 MΩ or equivalent

$Z_{OUT}$ of pulse generator = 50 Ω

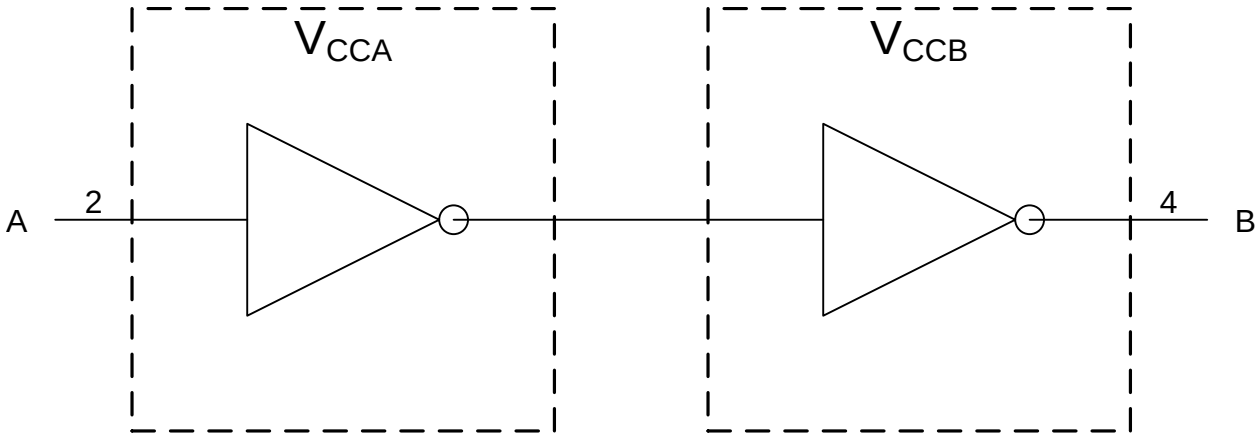
**Figure 3. AC (Propagation Delay) Test Circuit**

# 8 Detailed Description

## 8.1 Overview

The SN74AUP1T34 is a unidirectional, single-bit, dual-supply, noninverting voltage-level translator. Pin A, which is referenced to $V_{CCA}$, receives the signal that is to be level translated. Pin B, which is referenced to $V_{CCB}$, transmits the level translated signal. Both supply pins $V_{CCA}$ and $V_{CCB}$ support a voltage range from 0.9 V to 3.6 V.

## 8.2 Functional Block Diagram






## 8.3 Feature Description

### 8.3.1 Fully Configurable Dual-Rail Design

Both $V_{CCA}$ and $V_{CCB}$ can be supplied at any voltage from 0.9 V to 3.6 V, making the device suitable for translating between any of the voltage nodes (1 V, 1.2 V, 1.8 V, 2.5 V, and 3.3 V).

### 8.3.2 Partial-Power-Down Mode Operation

$I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the SN74AUP1T34 when it is powered down. This can occur in applications where subsections of a system are powered down (partial-power-down) to reduce power consumption.

### 8.3.3 $V_{CC}$ Isolation

The $V_{CC}$ isolation feature ensures that if either $V_{CCA}$ or $V_{CCB}$ are at GND (or < 0.4 V), both ports A and B are set to a high-impedance state, preventing false logic levels from being presented to either bus.

### 8.3.4 Input Hysteresis

Input hysteresis allows the input to support slew rates as slow as 200 ns/V, improving switching noise immunity.

## 8.4 Device Functional Modes

Table 1 lists the functional modes of the SN74AUP1T34.

**Table 1. Function Table**

| INPUT | OUTPUT |
|---|---|
| **A PORT** | **B PORT** |
| L | L |
| H | H |

# 9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The SN74AUP1T34 can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another.

## 9.2 Typical Application

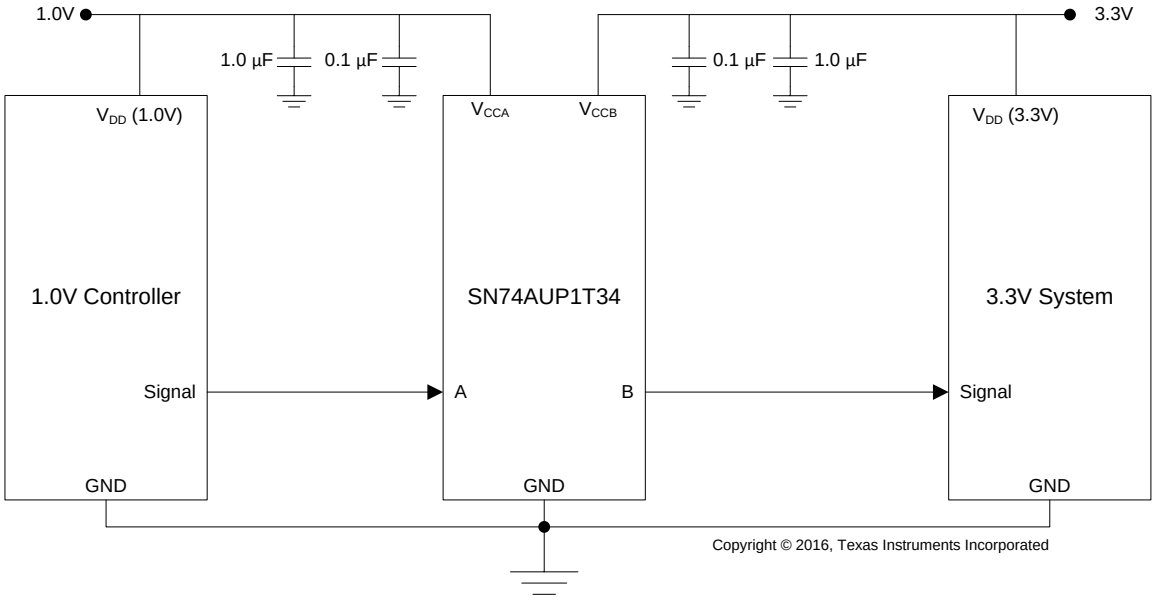



**Figure 4. Typical Application Example**

### 9.2.1 Design Requirements

Table 2 lists the design requirements of the SN74AUP1T34.

**Table 2. Design Parameters**

| DESIGN PARAMETER | EXAMPLE VALUE |
|---|---|
| Input Voltage Range | 0.9 V to 3.6 V |
| Output Voltage Range | 0.9 V to 3.6 V |

### 9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the SN74AUP1T34 device to determine the input voltage range. For a valid logic-high, the value must exceed the $V_{IH}$ of the input port. For a valid logic low the value must be less than the $V_{IL}$ of the input port.
- Output voltage range
  - Use the supply voltage of the device that the SN74AUP1T34 device is driving to determine the output voltage range.

### 9.2.3 Application Curve

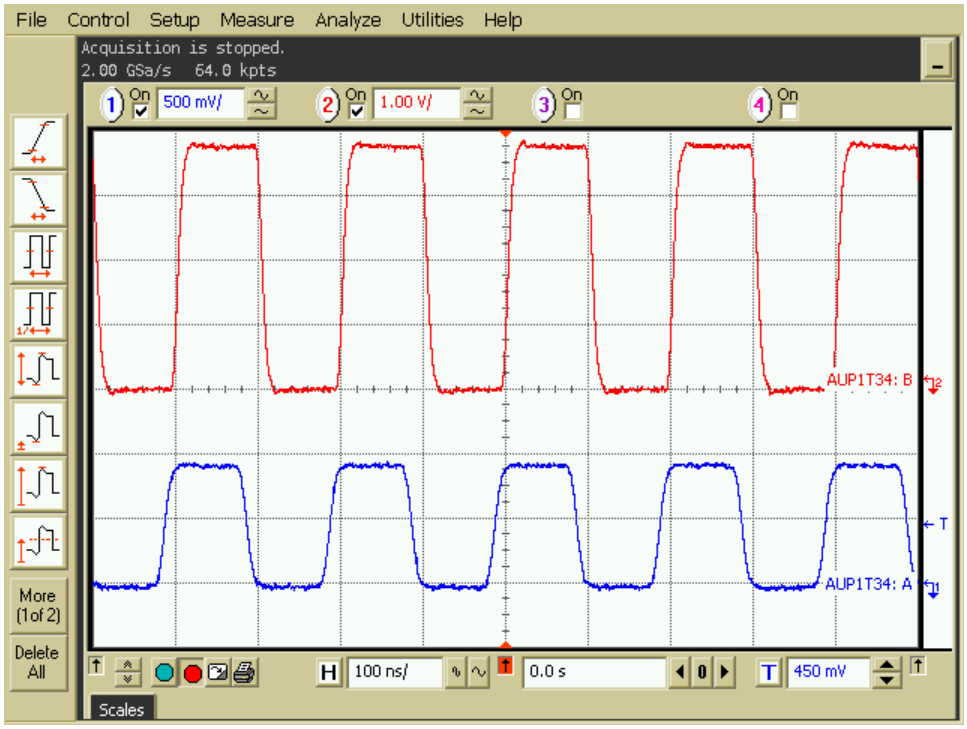



**Figure 5. 10-MHz Up Translation (0.9 V to 3.6 V)**

## 10 Power Supply Recommendations

Connect ground before applying either $V_{CCA}$ or $V_{CCB}$. There is no specific power sequence requirement for the SN74AUP1T34. $V_{CCA}$ or $V_{CCB}$ may be powered up first, and $V_{CCA}$ or $V_{CCB}$ may be powered down first.

## 11 Layout

### 11.1 Layout Guidelines

To ensure reliability of the device, TI recommends following common printed-circuit board layout guidelines is recommended.

- Bypass capacitors must be used on power supplies.
- Short trace lengths must be used to avoid excessive loading.
- Placing pads on the signal paths for loading capacitors or pullup resistors helps adjust rise and fall times of signals depending on the system requirements.

### 11.2 Layout Example

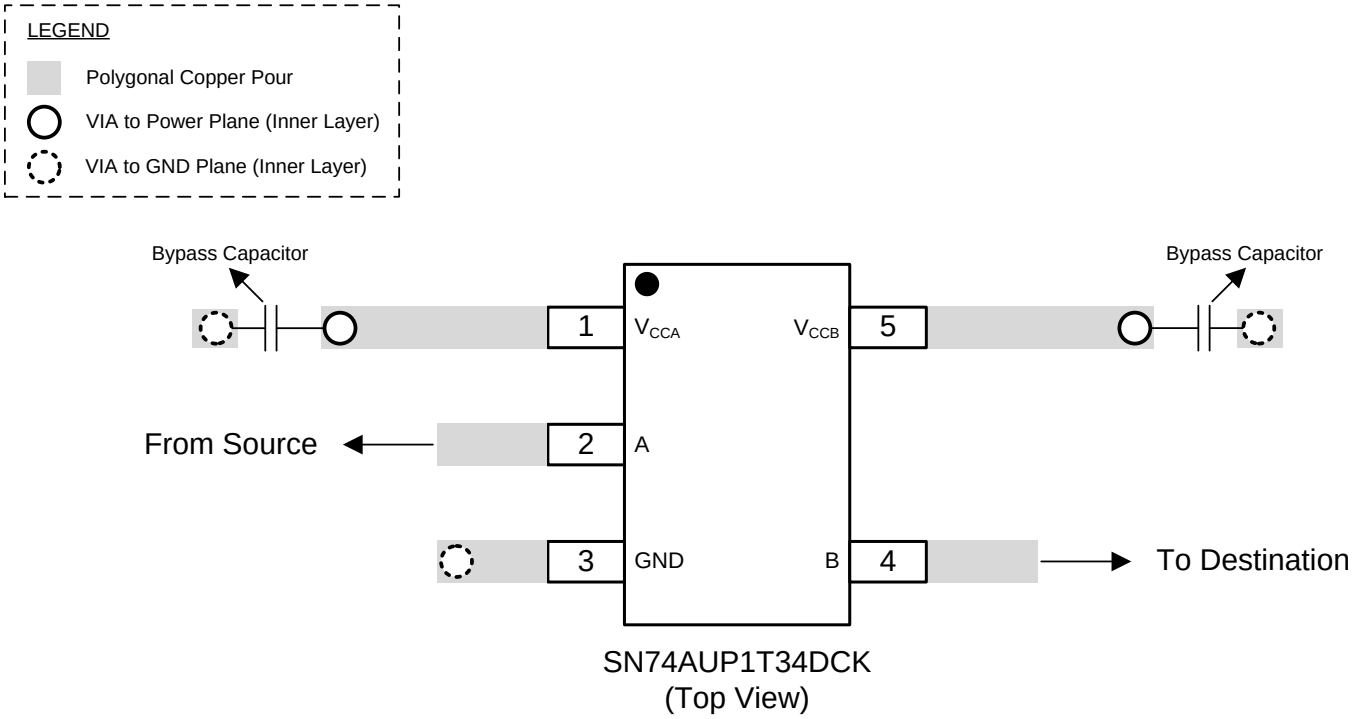



**Figure 6. Example Layout**

# 12 器件和文档支持

## 12.1 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 12.2 商标

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## 12.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

## 12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。要获得这份数据表的浏览器版本，请查阅左侧的导航栏。

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| 数据转换器 | www.ti.com.cn/dataconverters | 消费电子 | www.ti.com/consumer-apps |
| DLP® 产品 | www.dlp.com | 能源 | www.ti.com/energy |
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| 接口 | www.ti.com.cn/interface | 安防应用 | www.ti.com.cn/security |
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| 电源管理 | www.ti.com.cn/power | 视频和影像 | www.ti.com.cn/video |
| 微控制器 (MCU) | www.ti.com.cn/microcontrollers | | |
| RFID 系统 | www.ti.com.cn/rfidsys | | |
| OMAP应用处理器 | www.ti.com/omap | | |
| 无线连通性 | www.ti.com.cn/wirelessconnectivity | 德州仪器在线技术支持社区 | www.deyisupport.com |

邮寄地址： 上海市浦东新区世纪大道1568 号，中建大厦32 楼邮政编码： 200122

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74AUP1T34DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | U2E | Samples |
| SN74AUP1T34DRYR | ACTIVE | SON | DRY | 6 | 5000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | U2 | Samples |
| SN74AUP1T34DSFR | ACTIVE | SON | DSF | 6 | 5000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | U2 | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN74AUP1T34 :**

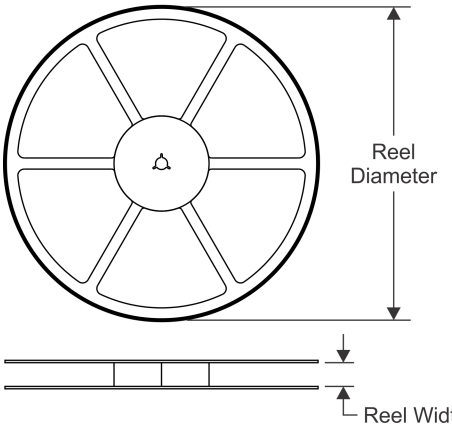
- Automotive: SN74AUP1T34-Q1

NOTE: Qualified Version Definitions:

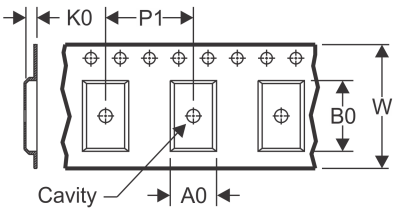
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

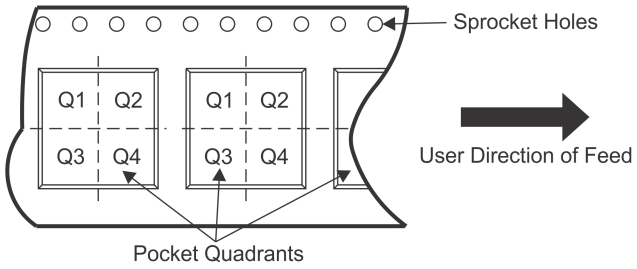



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

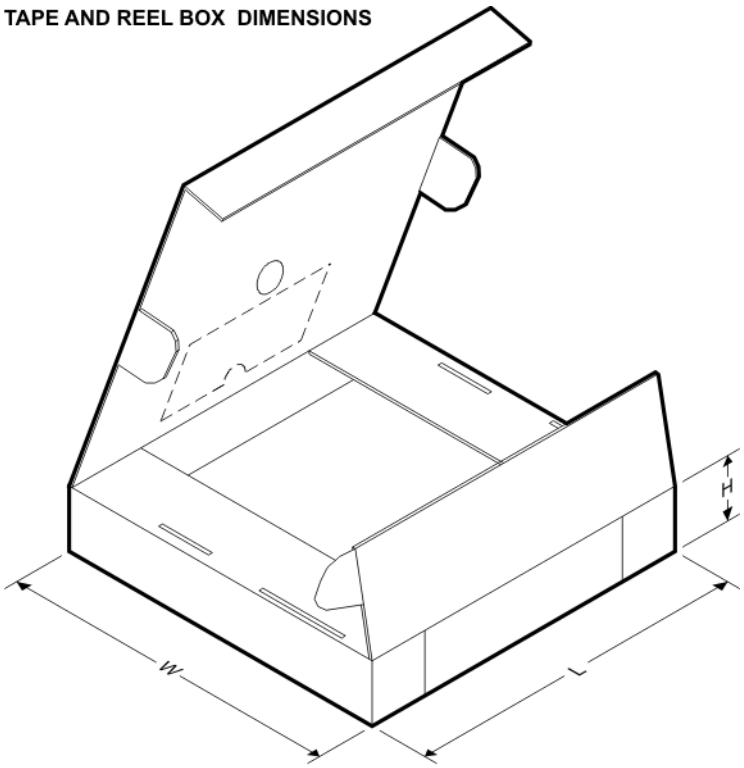
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74AUP1T34DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74AUP1T34DRYR | SON | DRY | 6 | 5000 | 180.0 | 9.5 | 1.15 | 1.6 | 0.75 | 4.0 | 8.0 | Q1 |
| SN74AUP1T34DSFR | SON | DSF | 6 | 5000 | 180.0 | 9.5 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |

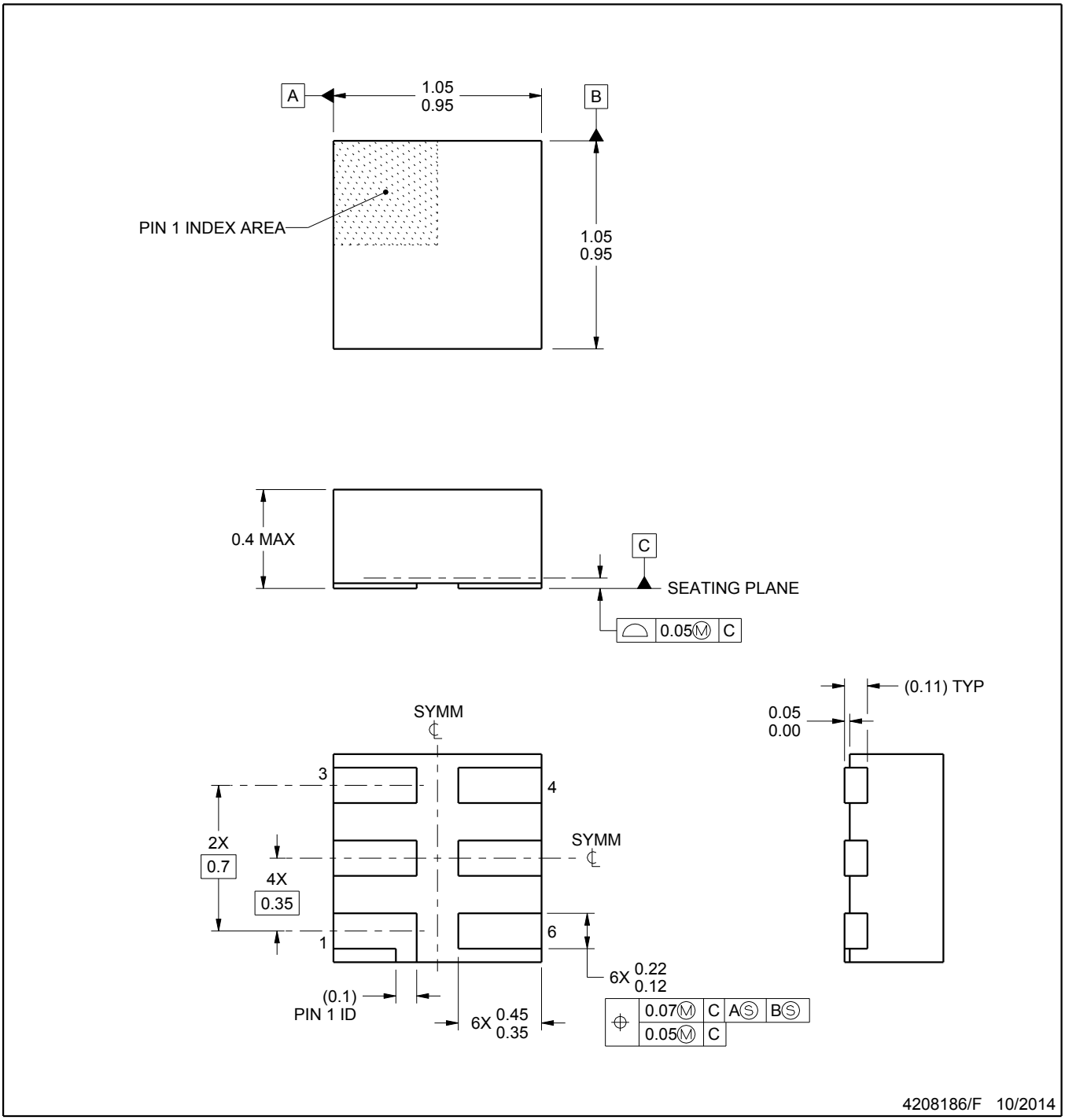
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74AUP1T34DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74AUP1T34DRYR | SON | DRY | 6 | 5000 | 184.0 | 184.0 | 19.0 |
| SN74AUP1T34DSFR | SON | DSF | 6 | 5000 | 184.0 | 184.0 | 19.0 |

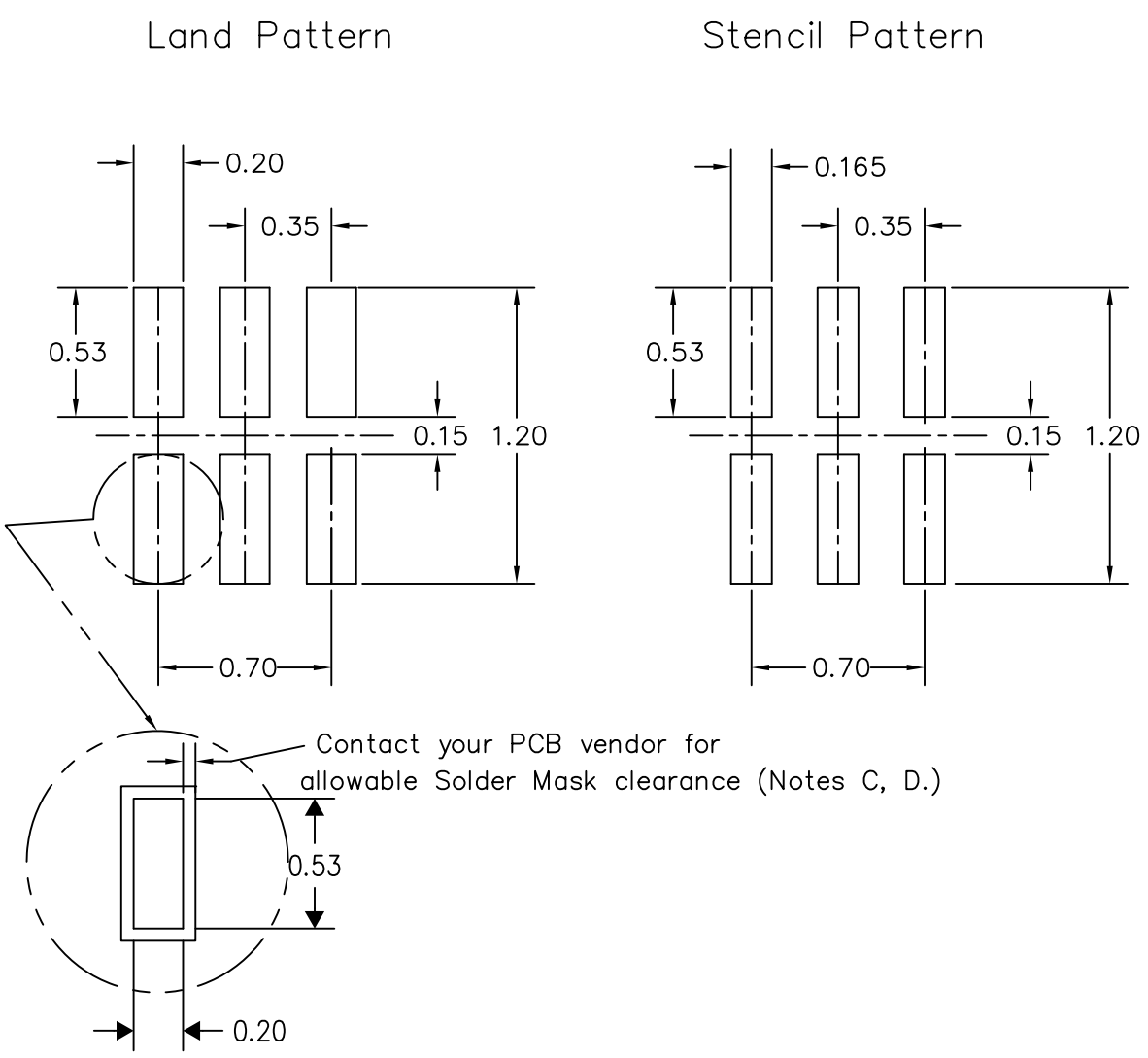
DSF (S-PX2SON-N6) PLASTIC SMALL OUTLINE NO-LEAD




NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.

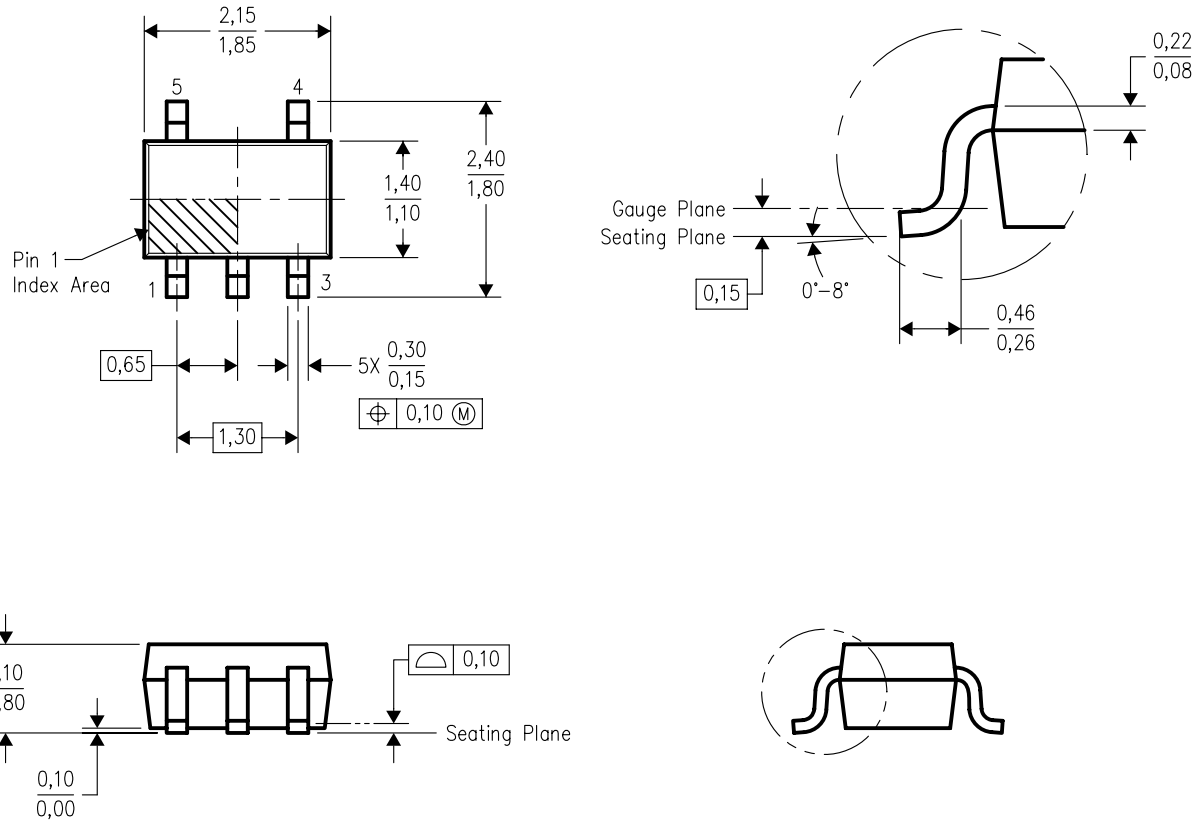
DSF (S–PX2SON–N6) PLASTIC SMALL OUTLINE NO–LEAD




4210277/D 05/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads. If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
H. Component placement force should be minimized to prevent excessive paste block deformation.

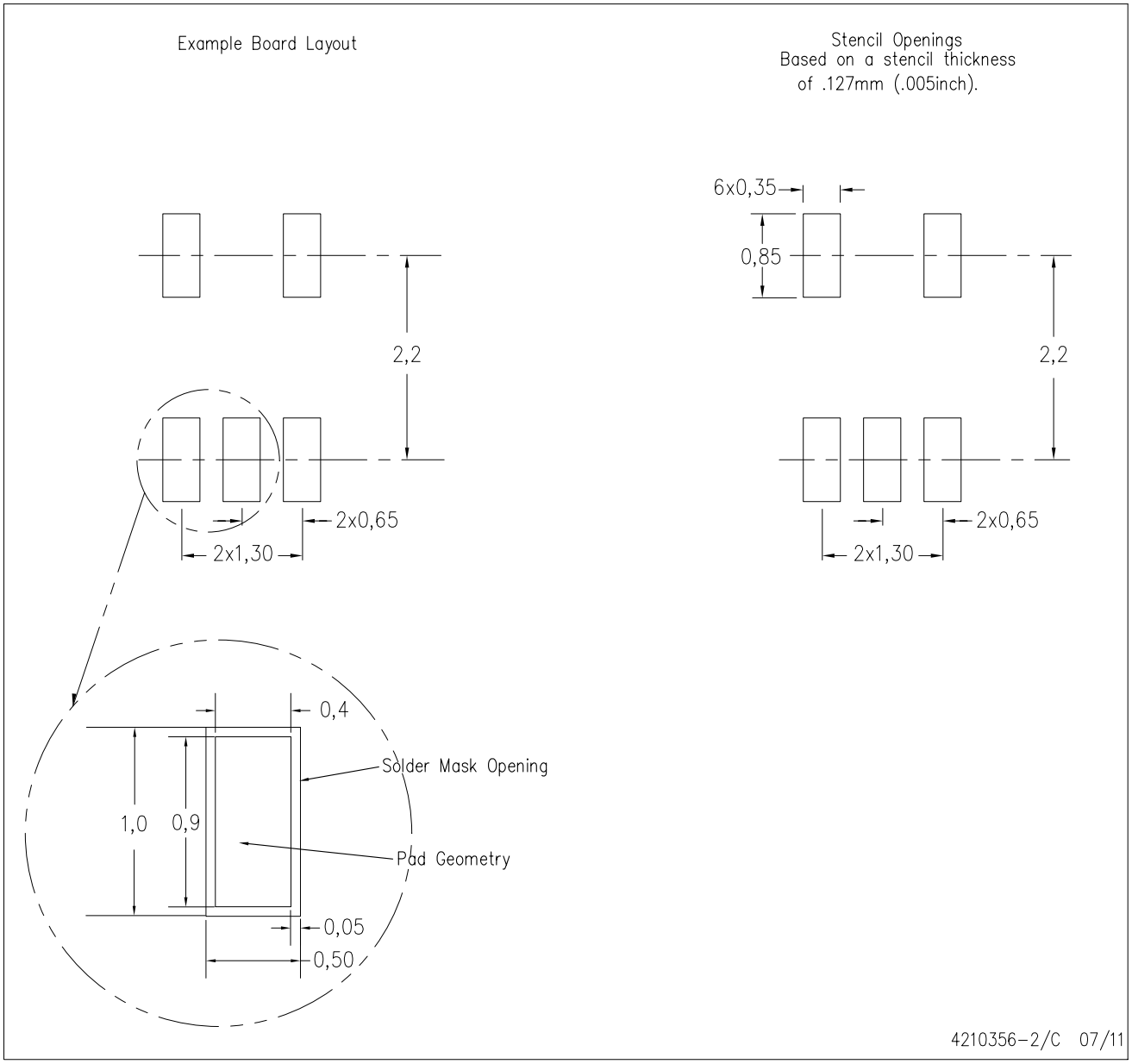
## DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE




4093553–3/G 01/2007

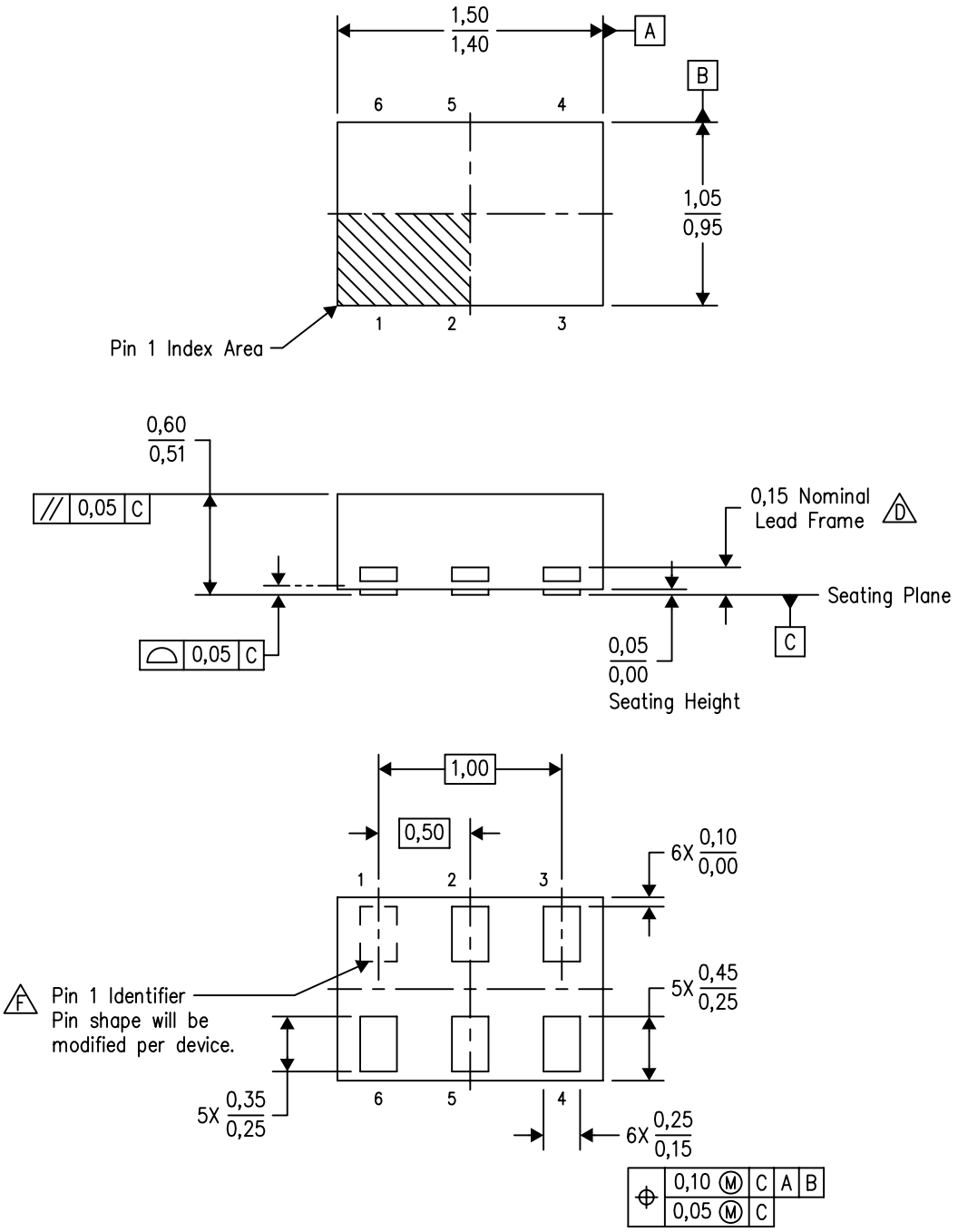
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

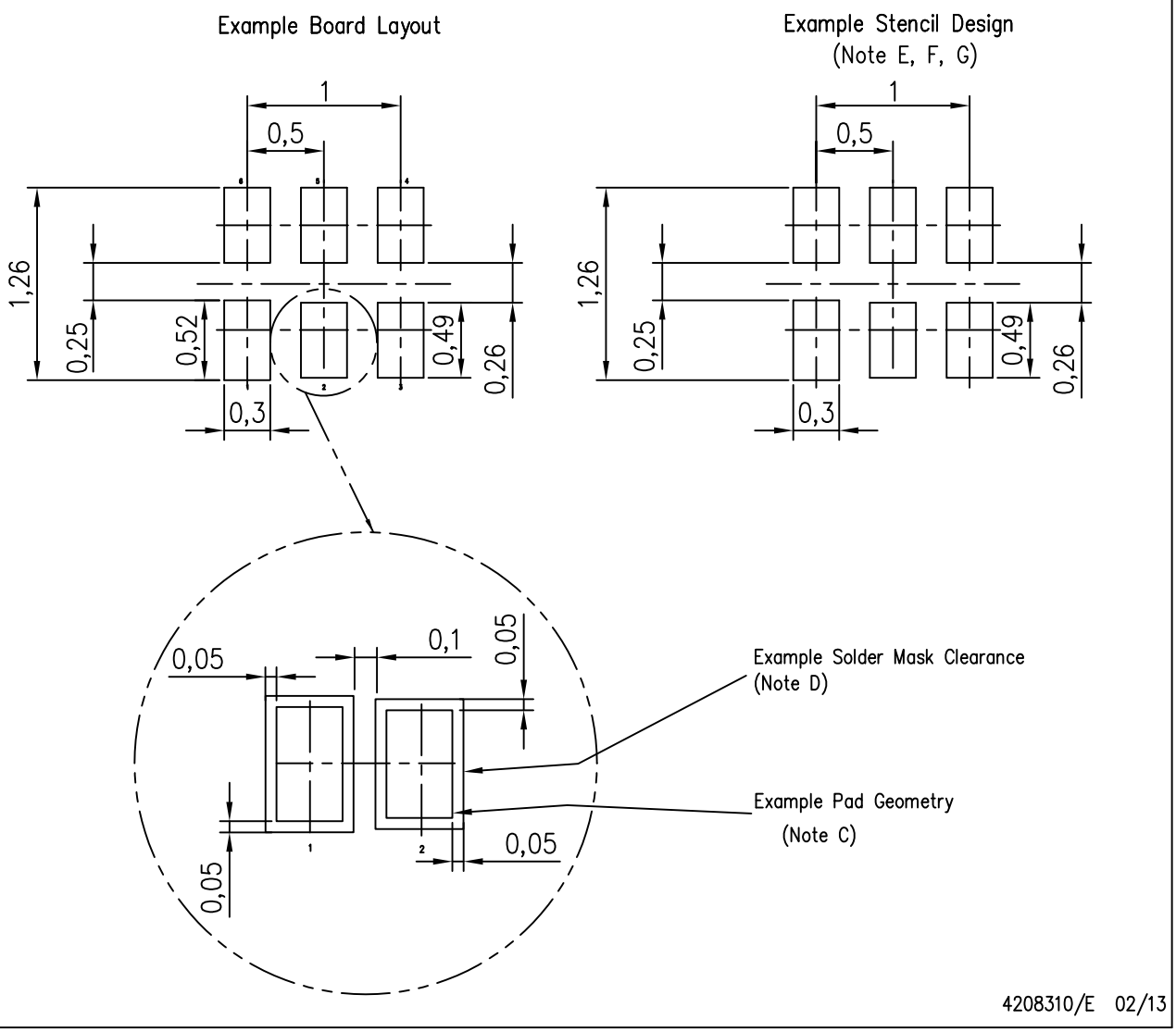
DRY (R–PUSON–N6) PLASTIC SMALL OUTLINE NO–LEAD




4207181/F 12/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.
E. This package complies to JEDEC MO–287 variation UFAD.
F. See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.

DRY (R–PUSON–N6) PLASTIC SMALL OUTLINE NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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