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### SN74AVC2T245

SCES692D - JUNE 2008 - REVISED FEBRUARY 2016

# SN74AVC2T245 Dual-Bit Dual-Supply Bus Transceiver with Configurable Level-Shifting / Voltage Translation and Tri-State Outputs

Technical

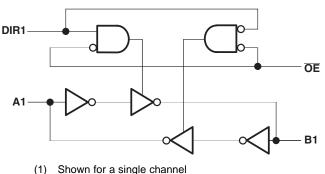
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#### 1 Features

- Each Channel Has Independent Direction Control
- Control Inputs VIH/VIL Levels Are Referenced to V<sub>CCA</sub> Voltage
- Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.2 V to 3.6 V Power-Supply Range
- I/Os Are 4.6 V Tolerant
- Ioff Supports Partial-Power-Down Mode Operation
- V<sub>CC</sub> Isolation Feature If Either V<sub>CC</sub> Input is at GND, Both Ports are in High-Impedance State
- Typical Data Rates
  - 500 Mbps (1.8 V to 3.3 V Level-Shifting)
  - 320 Mbps (<1.8 V to 3.3 V Level-Shifting)
  - 320 Mbps (Translate to 2.5 V or 1.8 V) \_
  - 280 Mbps (Translate to 1.5 V)
  - 240 Mbps (Translate to 1.2 V)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 5000 V Human-Body Model (A114-A)
  - 200 V Machine Model (A115-A)
  - 1500 V Charged-Device Model (C101)

#### Applications 2

- Personal Electronics
- Industrial
- Enterprise
- Telecom



### Logic Diagram (Positive Logic)

### 3 Description

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This dual-bit noninverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track V\_{CCA}. V\_{CCA} accepts any supply voltage from 1.2 V to 3.6 V. The B port is designed to track V<sub>CCB</sub>. V<sub>CCB</sub> accepts any supply voltage from 1.2 V to 3.6 V. This allows for universal low-voltage bidirectional translation between any of the 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V voltage nodes.

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The SN74AVC2T245 is designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR) input and the output-enable (OE) activate either the B-port outputs or the A-port outputs or place both output ports into the high-impedance mode . The device transmits data from the A bus to the B bus when the B-port outputs are activated and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports always is active and must have a logic HIGH or LOW level applied to prevent excess I<sub>CC</sub> and I<sub>CCZ</sub>.

The SN74AVC2T245 control pins (DIR1, DIR2, and  $\overline{OE}$ ) are supplied by V<sub>CCA</sub>.

This device is fully specified for partial-power-down applications using Ioff. The Ioff circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The  $V_{CC}$  isolation feature ensures that if either  $V_{CC}$ input is at GND, both ports are in the high-impedance state.

To ensure the high-impedance state during power up or power down, OE must be connected to V<sub>CC</sub> through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74AVC2T245	UQFN (10)	1.80 mm × 1.40 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.



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CI	hanges from Revision C (July 2015) to Revision D	Page
•	Made changes to Pin Configuration and Functions	1
CI	hanges from Revision B (June 2015) to Revision C	Page
•	The Ordering Information table (formally on page 1) contained a Top-Side Marking of TQ The table has been replaced with the Package Option Addendum in <i>Mechanical, Packaging, and Orderable Information</i> . VC_ was added to the device marking .	17
CI	hanges from Revision A (May 2012) to Revision B	Page
•	Added Pin Configuration and Functions section, ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section	1
•	Removed the Ordering Information table.	1

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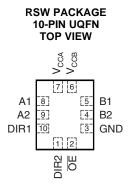
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# 5 Pin Configuration and Functions



### **Pin Functions**

	PIN					
NAME	NO. (UQFN)	DESCRIPTION				
V <sub>CCA</sub>	7	Supply Voltage A				
V <sub>CCB</sub>	6	Supply Voltage B				
GND	3	Ground				
A1	8	Output or input depending on state of DIR. Output level depends on $V_{\mbox{\scriptsize CCA}}$ .				
A2	9	Output or input depending on state of DIR. Output level depends on $V_{CCA}$ .				
B1	5	Output or input depending on state of DIR. Output level depends on $V_{CCB}$ .				
B2	4	Output or input depending on state of DIR. Output level depends on $V_{CCB}$ .				
DIR1,DIR2	10,1	Direction Pin, Connect to GND or to $V_{CCA}$				
ŌĒ	2	Tri-state output-mode enables. Pull OE high to place all outputs in 3-state mode. Referenced to $V_{CCA}$				

### 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
$V_{CCA} V_{CCB}$	Supply voltage	-0.5	4.6	V	
		I/O ports (A port)	-0.5	4.6	
VI	Input voltage <sup>(2)</sup>	I/O ports (B port)	-0.5	4.6	V
		Control inputs	-0.5	4.6	
V	Voltage applied to any output in the high-impedance or power-off	A port	-0.5	4.6	V
Vo	state <sup>(2)</sup>	B port	-0.5	4.6	v
	Voltage applied to any output in the high or low state $^{(2)}$ $^{(3)}$	A port	-0.5	V <sub>CCA</sub> + 0.5	V
Vo		B port	-0.5	V <sub>CCB</sub> + 0.5	v
I <sub>IK</sub>	Input clamp current	V <sub>1</sub> < 0		-50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		-50	mA
I <sub>O</sub>	Continuous output current			±50	mA
	Continuous current through V <sub>CCA</sub> , V <sub>CCB</sub> , or GND			±100	mA
TJ	Junction Temperature		-40	150	°C
T <sub>stg</sub>	Storage temperature range		-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.

### 6.2 ESD Ratings

			VALUE	UNIT
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	5000	
V <sub>(ESD)</sub>	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 $^{\left( 2\right) }$	1500	V

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions<sup>(1) (2) (3)</sup>

			V <sub>CCI</sub>	V <sub>cco</sub>	MIN	MAX	UNIT	
$V_{CCA}$	Supply voltage				1.2	3.6	V	
V <sub>CCB</sub>	Supply voltage				1.2	3.6	V	
			1.2 V to 1.95 V		V <sub>CCI</sub> × 0.65			
V <sub>IH</sub>	High-level input voltage		1.95 V to 2.7 V		1.6		V	
			2.7 V to 3.6 V		2			
			1.2 V to 1.95 V			V <sub>CCI</sub> × 0.35		
VIL	Low-level	put voltage Data inputs <sup>(1)</sup>	1.95 V to 2.7 V			0.7	V	
	input voltage		2.7 V to 3.6 V			0.8		
			1.2 V to 1.95 V		V <sub>CCA</sub> × 0.65			
V <sub>IH</sub>	High-level input voltage			1.95 V to 2.7 V		1.6		V
		(referenced to V <sub>CCA</sub> ) <sup>(2)</sup>			2			

(1)  $V_{CCI}$  is the  $V_{CC}$  associated with the input port.

(2)  $V_{CCO}$  is the  $V_{CC}$  associated with the output port.

<sup>(3)</sup> All unused data inputs of the device must be held at V<sub>CCI</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



# Recommended Operating Conditions<sup>(1) (2) (3)</sup> (continued)

			V <sub>CCI</sub>	V <sub>cco</sub>	MIN	MAX	UNIT
			1.2 V to 1.95 V			$V_{CCA} \times 0.35$	
VIL	Low-level input voltage	DIR (referenced to V <sub>CCA</sub> ) <sup>(2)</sup>	1.95 V to 2.7 V			0.7	V
	input voltage		2.7 V to 3.6 V			0.8	
VI	Input voltage				0	3.6	V
	Output upliers	Active state			0	V <sub>CCO</sub>	V
Vo	Output voltage	3-state			0	3.6	v
				1.1 V to 1.2 V		-3	
				1.4 V to 1.6 V		-6	
I <sub>OH</sub>	High-level output cu	rrent	1.65 V to 1.95 V			-8	mA
				2.3 V to 2.7 V		-9	
				3 V to 3.6 V		-12	
				1.1 V to 1.2 V		3	
				1.4 V to 1.6 V		6	
I <sub>OL</sub>	Low-level output cur	rent		1.65 V to 1.95 V		8	mA
				2.3 V to 2.7 V		9	
				3 V to 3.6 V		12	
$\Delta t / \Delta v$	Input transition rise	or fall rate				5	ns/V
T <sub>A</sub>	Operating free-air te	mperature			-40	85	°C

### 6.4 Thermal Information

		SN74AVC2T245	
	THERMAL METRIC <sup>(1)</sup>	RSW (UQFN)	UNIT
		10 PINS	
$R_{ hetaJA}$	Junction-to-ambient thermal resistance	109.1	°C/W
R <sub>0JC(top)</sub>	Junction-to-case (top) thermal resistance	57.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	57.0	°C/W
ΨJT	Junction-to-top characterization parameter	2.7	°C/W
ΨЈВ	Junction-to-board characterization parameter	57.0	°C/W
R <sub>0JC(bot)</sub>	Junction-to-case (bottom) thermal resistance	18.4	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

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### 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)<sup>(1)(2)</sup>

PARAMETER		TEST CONDI	TIONS		v	T,	<sub>A</sub> = 25°C	–40°C to 8	5°C		
		TEST CONDITIONS		V <sub>CCA</sub>	V <sub>CCB</sub>	MIN	TYP	MAX	MIN	MAX	UNIT
V <sub>он</sub>		I <sub>OH</sub> = −100 μA		1.2 V to 3.6 V	1.2 V to 3.6 V				V <sub>CCO</sub> - 0.2		
		I <sub>OH</sub> = -3 mA		1.2 V	1.2 V		0.95				
		I <sub>OH</sub> = -6 mA		1.4 V	1.4 V				1.05		
VOH		I <sub>OH</sub> = -8 mA	$V_{I} = V_{IH}$	1.65 V	1.65 V				1.2		V
		I <sub>OH</sub> = -9 mA		2.3 V	2.3 V				1.75		
		I <sub>OH</sub> = -12 mA		3 V	3 V				2.3		
		I <sub>OL</sub> = 100 μA		1.2 V to 3.6 V	1.2 V to 3.6 V					0.2	
		I <sub>OL</sub> = 3 mA		1.2 V	1.2 V		0.25				
		I <sub>OL</sub> = 6 mA		1.4 V	1.4 V					0.35	.,
V <sub>OL</sub>		I <sub>OL</sub> = 8 mA	$V_{I} = V_{IL}$	1.65 V	1.65 V					0.45	V
		I <sub>OL</sub> = 9 mA		2.3 V	2.3 V					0.55	
		I <sub>OL</sub> = 12 mA		3 V	3 V					0.7	
I <sub>I</sub>	Control inputs	$V_I = V_{CCA}$ or GND		1.2 V to 3.6 V	1.2 V to 3.6 V		±0.025	±0.25		±1	μA
				0 V	0 V to 3.6 V		±0.1	±1		±5	
l <sub>off</sub>	А ог В роп	$V_1 \text{ or } V_0 = 0 \text{ to } 3.6$	V	0 V to 3.6 V	0 V		±0.1	±1		±5	μA
I <sub>OZ</sub>	A or B port	$V_{O} = V_{CCO} \text{ or GND}$ $V_{I} = V_{CCI} \text{ or GND},$		3.6 V	3.6 V		±0.5	±2.5		±5	μA
				1.2 V to 3.6 V	1.2 V to 3.6 V					8	
I <sub>CCA</sub>		$V_I = V_{CCI}$ or GND,	l <sub>O</sub> = 0	0 V	0 V to 3.6 V					-2	μA
				0 V to 3.6 V	0 V					8	
				1.2 V to 3.6 V	1.2 V to 3.6 V					8	
I <sub>CCB</sub>		$V_I = V_{CCI} \text{ or } GND,$	l <sub>O</sub> = 0	0 V	0 V to 3.6 V					8	μA
				0 V to 3.6 V	0 V					-2	
I <sub>CCA</sub> +	- I <sub>CCB</sub>	$V_I = V_{CCI}$ or GND,	I <sub>O</sub> = 0	1.2 V to 3.6 V	1.2 V to 3.6 V					16	μA
C <sub>i</sub>	Control inputs	$V_{I} = 3.3 \text{ V or GND}$		3.3 V	3.3 V		3.5			4.5	pF
Cio	A or B port	$V_0 = 3.3 \text{ V or GNE}$	)	3.3 V	3.3 V		6			7	pF

 $\begin{array}{ll} \mbox{(1)} & V_{CCO} \mbox{ is the } V_{CC} \mbox{ associated with the output port.} \\ \mbox{(2)} & V_{CCI} \mbox{ is the } V_{CC} \mbox{ associated with the input port.} \end{array}$ 



### 6.6 Switching Characteristics: V<sub>CCA</sub> = 1.2 V

over recommended operating free-air temperature range,  $V_{CCA} = 1.2 \text{ V}$  (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CCB</sub> = 1.2 V	V <sub>CCB</sub> = 1.5 V ± 0.1 V	V <sub>CCB</sub> = 1.8 V ± 0.15 V	V <sub>CCB</sub> = 2.5 V ± 0.2 V	V <sub>CCB</sub> = 3.3 V ± 0.3 V	UNIT
	(INFOT)	(001F01)	ТҮР	TYP	TYP	TYP	TYP	
t <sub>PLH</sub>	А	В	2.5	2.1	1.9	1.9	1.9	20
t <sub>PHL</sub>	A	D	2.5	2.1	1.9	1.9	1.9	ns
t <sub>PLH</sub>	В	^	2.5	2.2	2	1.8	1.7	20
t <sub>PHL</sub>	В	A	2.5	2.2	2	1.8	1.7	ns
t <sub>PZH</sub>	OE	^	3.8	3.1	2.7	2.6	3	20
t <sub>PZL</sub>	UE	A	3.8	3.1	2.7	2.6	3	ns
t <sub>PZH</sub>	OE	В	3.7	3.7	3.7	3.7	3.7	5
t <sub>PZL</sub>	UE	D	3.7	3.7	3.7	3.7	3.7	ns
t <sub>PHZ</sub>	OE	^	4.4	3.6	3.5	3.3	4.1	20
t <sub>PLZ</sub>	UE	A	4.4	3.6	3.5	3.3	4.1	ns
t <sub>PHZ</sub>	OE	В	4.2	4.2	4.3	4.1	4.2	20
t <sub>PLZ</sub>	UE	D	4.2	4.2	4.3	4.1	4.2	ns

# 6.7 Switching Characteristics: $V_{CCA} = 1.5 V \pm 0.1 V$

over recommended operating free-air temperature range,  $V_{CCA} = 1.5 \text{ V} \pm 0.1 \text{ V}$  (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CCB</sub> = 1.2 V	V <sub>CCB</sub> = ± 0.1	1.5 V I V	V <sub>CCB</sub> = ± 0.1		V <sub>CCB</sub> = ± 0.2		V <sub>CCB</sub> = ± 0.		UNIT
	(INPOT)	(001201)	ТҮР	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	А	В	2.2	0.3	4.4	0.2	3.9	0.1	3.6	0.1	3.9	20
t <sub>PHL</sub>	A	В	2.2	0.3	4.4	0.2	3.9	0.1	3.6	0.1	3.9	ns
t <sub>PLH</sub>	В	•	2	0.6	5.1	0.4	4.9	0.2	4.6	0.1	4.5	~~
t <sub>PHL</sub>	Б	A	2	0.6	5.1	0.4	4.9	0.2	4.6	0.1	4.5	ns
t <sub>PZH</sub>	OE	А	3.4	1.1	7.1	0.9	6.2	0.7	5.5	0.1	6.4	~~
t <sub>PZL</sub>	UE	A	3.4	1.1	7.1	0.9	6.2	0.7	5.5	0.1	6.4	ns
t <sub>PZH</sub>	OE	В	2.5	1.1	8.2	1.1	8.2	1.1	8.2	1.1	8.2	
t <sub>PZL</sub>	UE	Б	2.5	1.1	8.2	1.1	8.2	1.1	8.2	1.1	8.2	ns
t <sub>PHZ</sub>	OE	А	4.1	1.2	7.1	0.8	6.7	0.4	5.6	1	74	~~
t <sub>PLZ</sub>	UE	A	4.1	1.2	7.1	0.8	6.7	0.4	5.6	1	7.4	ns
t <sub>PHZ</sub>	OE	D	3.3	0.3	7.4	0.2	5.7	0.3	5.6	0.3	5.6	
t <sub>PLZ</sub>	UE	В	3.3	0.3	7.4	0.2	5.7	0.3	5.6	0.3	5.6	ns

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## 6.8 Switching Characteristics: $V_{CCA} = 1.8 \text{ V} \pm 0.15 \text{ V}$

over recommended operating free-air temperature range,  $V_{CCA} = 1.8 \text{ V} \pm 0.15 \text{ V}$  (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CCB</sub> = 1.2 V	V <sub>CCB</sub> = 1.5 V ± 0.1 V		V <sub>CCB</sub> = 1.8 V ± 0.15 V		V <sub>CCB</sub> = 2.5 V ± 0.2 V		V <sub>CCB</sub> = 3.3 V ± 0.3 V		UNIT
	(INPUT)	(001901)	TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	А	в	2	0.1	4.1	0.1	3.6	0.1	3.1	0.1	3.3	20
t <sub>PHL</sub>	A	D	2	0.1	4.1	0.1	3.6	0.1	3.1	0.1	3.3	ns
t <sub>PLH</sub>	В	А	1.9	0.4	4.3	0.1	4.1	0.1	3.8	0.1	3.7	20
t <sub>PHL</sub>	Б	A	1.9	0.4	4.3	0.1	4.1	0.1	3.8	0.1	3.7	ns
t <sub>PZH</sub>	OE	А	3.2	0.8	6.7	0.4	5.8	0.4	4.8	0.3	4.6	ns
t <sub>PZL</sub>	0E	A	3.2	0.8	6.7	0.4	5.8	0.4	4.8	0.3	4.6	
t <sub>PZH</sub>	OE	В	1.9	0.2	6.7	0.2	6.6	0.2	6.7	0.2	6.7	20
t <sub>PZL</sub>	UE	D	1.9	0.2	6.7	0.2	6.6	0.2	6.7	0.2	6.7	ns
t <sub>PHZ</sub>	ŌE	А	3.8	0.7	6.2	0.3	6.5	0.1	5.2	0.8	6.5	20
t <sub>PLZ</sub>	UE	A	3.8	0.7	6.2	0.3	6.5	0.1	5.2	0.8	6.5	ns
t <sub>PHZ</sub>	OE	В	3.4	0.1	6.8	0.1	6.8	0.1	6.7	0.1	6.7	20
t <sub>PLZ</sub>	UE	В	3.4	0.1	6.8	0.1	6.8	0.1	6.7	0.1	6.7	ns

# 6.9 Switching Characteristics: $V_{CCA} = 2.5 V \pm 0.2 V$

over recommended operating free-air temperature range,  $V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}$  (see Figure 3)

		<u> </u>		1 <b>0</b> / 00A									
PARAMETER	FROM TO (INPUT) (OUTPUT)		V <sub>CCB</sub> = 1.2 V	V <sub>CCB</sub> = ± 0.1		V <sub>CCB</sub> = 1.8 V ± 0.15 V		V <sub>CCB</sub> = 2.5 V ± 0.2 V		V <sub>CCB</sub> = 3.3 V ± 0.3 V		UNIT	
	(INFOT)	(001201)	ТҮР	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
t <sub>PLH</sub>	А	В	1.9	0.1	3.8	0.1	3.2	0.1	2.7	0.1	2.6	2	
t <sub>PHL</sub>	A	В	1.9	0.1	3.8	0.1	3.2	0.1	2.7	0.1	2.6	ns	
t <sub>PLH</sub>	В	А	1.8	0.5	3.4	0.2	3.1	0.1	2.8	0.1	2.6	20	
t <sub>PHL</sub>	Б	A	1.8	0.5	3.4	0.2	3.1	0.1	2.8	0.1	2.6	ns	
t <sub>PZH</sub>	ŌĒ	А	3.1	0.7	6.2	0.5	5.2	0.3	4.1	0.3	3.6	2	
t <sub>PZL</sub>		A	3.1	0.7	6.2	0.5	5.2	0.3	4.1	0.3	3.6	ns	
t <sub>PZH</sub>	OE	В	1.4	0.4	4.5	0.4	4.5	0.4	4.5	0.4	4.5	20	
t <sub>PZL</sub>	UE	Б	1.4	0.4	4.5	0.4	4.5	0.4	4.5	0.4	4.5	ns	
t <sub>PHZ</sub>	OE	А	3.6	0.2	5.2	0.1	5.4	0.1	4.5	0.7	6	2	
t <sub>PLZ</sub>	UE	А	3.6	0.2	5.2	0.1	5.4	0.1	4.5	0.7	6	ns	
t <sub>PHZ</sub>	OE	В	2.1	0.1	4.7	0.1	4.6	0.1	4.7	0.1	4.7		
t <sub>PLZ</sub>	UE	В	2.1	0.1	4.7	0.1	4.6	0.1	4.7	0.1	4.7	ns	



# 6.10 Switching Characteristics: $V_{CCA} = 3.3 V \pm 0.3 V$

over recommended operating free-air temperature range,  $V_{CCA} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CCB</sub> = 1.2 V	V <sub>CCB</sub> = ± 0.1		V <sub>CCB</sub> = ± 0.1	1.8 V 5 V	V <sub>CCB</sub> = ± 0.2		V <sub>CCB</sub> = ± 0.3		UNIT
	(INPUT)	(001901)	ТҮР	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	А	В	1.8	0.1	3.6	0.1	3	0.1	2.6	0.1	2.4	~~
t <sub>PHL</sub>	A	D	1.8	0.1	3.6	0.1	3	0.1	2.6	0.1	2.4	ns
t <sub>PLH</sub>	В	•	1.9	0.5	3.4	0.2	2.9	0.1	2.5	0.1	2.3	
t <sub>PHL</sub>	В	A	1.9	0.5	3.4	0.2	2.9	0.1	2.5	0.1	2.3	ns
t <sub>PZH</sub>	OE	•	3.1	0.9	5.9	0.5	5	0.3	3.8	0.3	3.3	~~~
t <sub>PZL</sub>	ÛE	A	3.1	0.9	5.9	0.5	5	0.3	3.8	0.3	3.3	ns 8.3
t <sub>PZH</sub>	OE	В	1.2	0.4	3.6	0.4	3.6	0.4	3.6	0.4	3.6	
t <sub>PZL</sub>	ÛE	В	1.2	0.4	3.6	0.4	3.6	0.4	3.6	0.4	3.6	ns
t <sub>PHZ</sub>	OE	А	3.4	0.1	4.6	0.1	4.7	0.3	4.8	0.7	4.5	~~~
t <sub>PLZ</sub>	UE	A	3.4	0.1	4.6	0.1	4.7	0.3	4.8	0.7	4.5	ns
t <sub>PHZ</sub>	OE	Р	2.9	0.1	5.4	0.1	5.3	0.1	5.3	0.1	5.3	~~
t <sub>PLZ</sub>	UE	В	2.9	0.1	5.4	0.1	5.3	0.1	5.3	0.1	5.3	ns

### 6.11 Operating Characteristics

 $T_A = 25^{\circ}C$ 

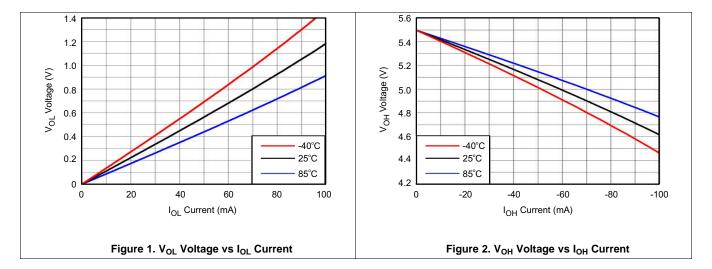
P	PARAME	TER	TEST CONDITIONS	V <sub>CCA</sub> = V <sub>CCB</sub> = 1.2 V TYP	V <sub>CCA</sub> = V <sub>CCB</sub> = 1.5 V TYP	V <sub>CCA</sub> = V <sub>CCB</sub> = 1.8 V TYP	V <sub>CCA</sub> = V <sub>CCB</sub> = 2.5 V TYP	V <sub>CCA</sub> = V <sub>CCB</sub> = 3.3 V TYP	UNIT	
		Outputs enabled		3	3	3	3	4		
<b>c</b> (1)	A to B	Outputs disabled	$C_L = 0,$	1	1	1	2	2	- 5	
$C_{pdA}$ <sup>(1)</sup>	B to A	Outputs enabled	f = 10  MHz, $t_r = t_f = 1 \text{ ns}$	12	13	13	15	15	pF	
	D IO A	Outputs disabled		1	2	2	2	2		
	A to B	Outputs enabled		12	13	13	14	16		
<b>C</b> (1)		Outputs disabled	$C_L = 0,$	1	2	2	2	2	~ <b>F</b>	
$C_{pdB}^{(1)}$		Outputs enabled	f = 10  MHz, $t_r = t_f = 1 \text{ ns}$	3	3	3	4	4	pF	
	B to A	Outputs disabled		1	1	1	2	2		

(1) Power dissipation capacitance per transceiver. Refer to the TI application report, CMOS Power Consumption and Cpd Calculation, SCAA035

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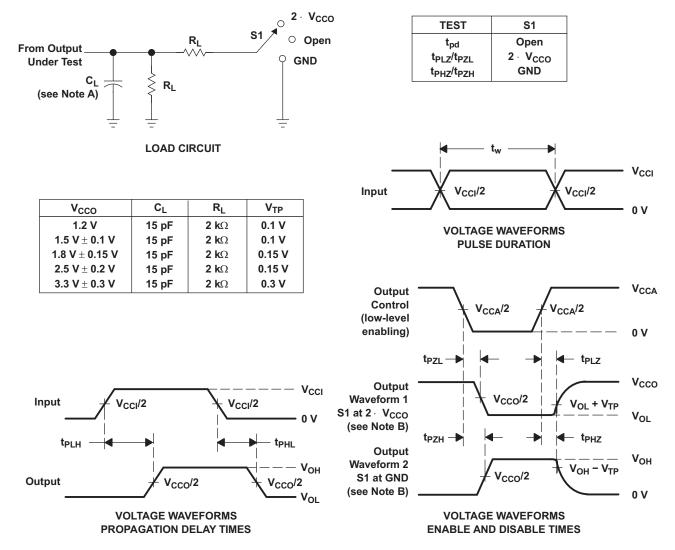
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# 6.12 Typical Characteristics





### 7 Parameter Measurement Information



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR 10 MHz,  $Z_0 = 50 \Omega$ , dv/dt  $\ge 1$  V/ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- F.  $V_{CCI}$  is the  $V_{CC}$  associated with the input port.
- G.  $V_{CCO}$  is the  $V_{CC}$  associated with the output port.

### Figure 3. Load and Circuit and Voltage Waveforms

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### 8 Detailed Description

### 8.1 Overview

The SN74AVC2T245 is a dual-bit, dual-supply noninverting bidirectional voltage level translation. Pins A and control pins (DIR and  $\overline{OE}$ ) are supported by V<sub>CCA</sub> and pins B are supported by V<sub>CCB</sub>. The A port can accept I/O voltages ranging from 1.2 V to 3.6 V, while the B port can accept I/O voltages from 1.2 V to 3.6 V. A high on DIR allows data transmission from A to B and a low on DIR allows data transmission from B to A when  $\overline{OE}$  is set to low. When  $\overline{OE}$  is set to high, both A and B are in the high-impedance state.

This device is fully specified for partial-power-down applications using off output current (I<sub>off</sub>).

The  $V_{CC}$  isolation feature ensures that if either  $V_{CC}$  input is at GND, both ports are put in a high-impedance state.

### 8.2 Functional Block Diagram

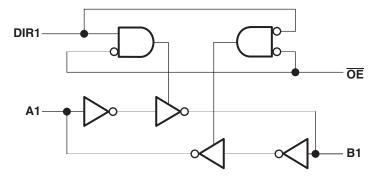


Figure 4. Logic Diagram (Positive Logic)

### 8.3 Feature Description

# 8.3.1 Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.2 V to 3.6 V Power-Supply Range

Both  $V_{CCA}$  and  $V_{CCB}$  can be supplied at any voltage from 1.2 V to 3.6 V making the device suitable for translating between any of the low voltage nodes (1.2 V, 1.8 V, 2.5 V, and 3.3 V).

### 8.3.2 Partial-Power-Down Mode Operation

This device is fully specified for partial-power-down applications using off output current (I<sub>off</sub>). The I<sub>off</sub> circuitry will prevent backflow current by disabling I/O output circuits when device is in partial power-down mode.

### 8.3.3 V<sub>CC</sub> Isolation

The  $V_{CC}$  isolation feature ensures that if either  $V_{CCA}$  or  $V_{CCB}$  are at GND, both ports will be in a high-impedance state ( $I_{OZ}$ ). This prevents false logic levels from being presented to either bus.



### 8.4 Device Functional Modes

The SN74AVC2T245 is a voltage level translator that can operate from 1.2 V to 3.6 V (V<sub>CCA</sub>) and 1.2 V to 3.6 V (V<sub>CCB</sub>). The signal translation requires direction control and output enable control. The table below enlists the operation of the part for the respective states of the control inputs.

ſ	CONTRO	L INPUTS	OUTPUT	CIRCUITS	OPERATION			
	OE	DIR1	A PORT	<b>B PORT</b>	OPERATION			
	L	L	Enabled	Hi-Z	B data to A data			
	L	Н	Hi-Z	Enabled	A data to B data			
	Н	Х	Hi-Z	Hi-Z	Isolation			

# Table 1. Function Table<sup>(1)</sup> (Each Transceiver)

(1) Input circuits of the data I/Os are always active.

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### 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The SN74AVC2T45 is used to shift IO voltage levels from one voltage domain to another. Bus A and bus B have independent power supplies, and a direction pin is used to control the direction of data flow. Unused data ports must not be floating; tie the unused port input and output to ground directly.

### 9.1.1 Enable Times

Calculate the enable times for the SN74AVC16T45 using the following formulas:

$t_{PZH}$ (DIR to A) = $t_{PLZ}$ (DIR to B) + $t_{PLH}$ (B to A)	(1)
$t_{PZL}$ (DIR to A) = $t_{PHZ}$ (DIR to B) + $t_{PHL}$ (B to A)	(2)
$t_{PZH}$ (DIR to B) = $t_{PLZ}$ (DIR to A) + $t_{PLH}$ (A to B)	(3)
$t_{PZL}$ (DIR to B) = $t_{PHZ}$ (DIR to A) + $t_{PHL}$ (A to B)	(4)

In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the SN74AVC2T245 initially is transmitting from A to B, then the DIR bit is switched; the B port of the device must be disabled before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay.

### 9.2 Typical Application

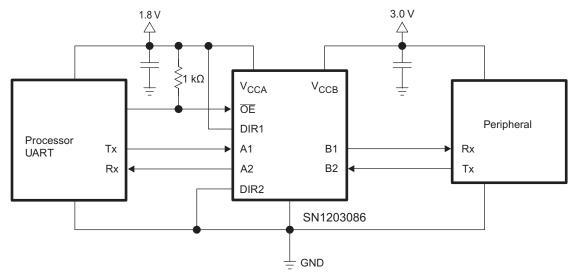


Figure 5. Typical Application of the SN74AVC2T245

### 9.2.1 Design Requirements

This device uses drivers which are enabled depending on the state of the DIR pin. The designer must know the intended flow of data and take care not to violate any of the high or low logic levels. Unused data inputs must not be floating, as this can cause excessive internal leakage on the input CMOS structure. Tie any unused input and output ports directly to ground.

For this design example, use the parameters listed in Table 2.



### **Table 2. Design Parameters**

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	1.2 V to 3.6 V
Output voltage range	1.2 V to 3.6 V

### 9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

### 9.2.2.1 Input Voltage Ranges

Use the supply voltage of the device that is driving the SN74AVC2T245 device to determine the input voltage range. For a valid logic high the value must exceed the  $V_{IH}$  of the input port. For a valid logic low the value must be less than the  $V_{IL}$  of the input port.

### 9.2.2.2 Output Voltage Range

Use the supply voltage of the device that the SN74AVC2T245 device is driving to determine the output voltage range.

### 9.2.3 Application Curves

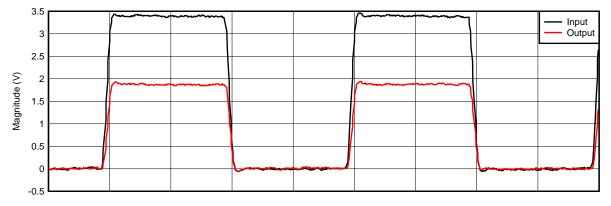


Figure 6. 3.3 V to 1.8 V Level-Shifting With 1-MHz Square Wave

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### **10 Power Supply Recommendations**

The SN74AVC2T245 device uses two separate configurable power-supply rails, V<sub>CCA</sub> and V<sub>CCB</sub>. V<sub>CCA</sub> accepts any supply voltage from 1.2 V to 3.6 V and V<sub>CCB</sub> accepts any supply voltage from 1.2 V to 3.6 V. The A port and B port are designed to track V<sub>CCA</sub> and V<sub>CCB</sub> respectively allowing for low-voltage bidirectional translation between any of the 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V and 5 V voltage nodes.

### 11 Layout

### 11.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit-board layout guidelines is recommended.

- Bypass capacitors should be used on power supplies.
- · Short trace lengths should be used to avoid excessive loading.
- Placing pads on the signal paths for loading capacitors or pullup resistors to help adjust rise and fall times of signals depending on the system requirements.

### 11.2 Layout Example

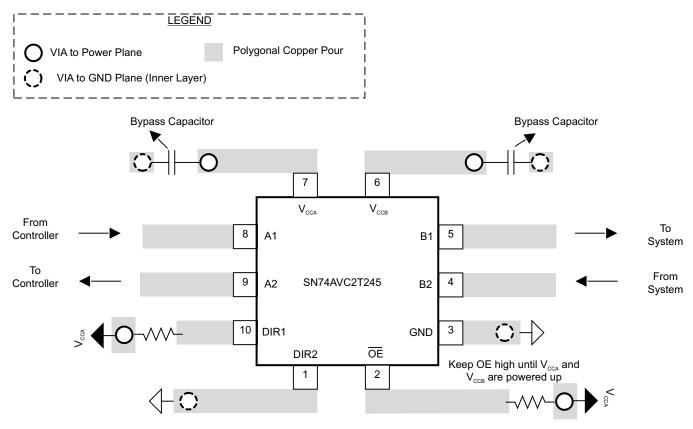


Figure 7. Recommended Layout Example



### **12 Device and Documentation Support**

### 12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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**Design Support TI's Design Support** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.2 Trademarks

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### 12.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.4 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

### 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

# PACKAGE MATERIALS INFORMATION

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### TAPE AND REEL INFORMATION





# QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AVC2T245RSWR	UQFN	RSW	10	3000	180.0	9.5	1.6	2.0	0.8	4.0	8.0	Q1
SN74AVC2T245RSWR	UQFN	RSW	10	3000	180.0	8.4	1.59	2.09	0.72	4.0	8.0	Q1
SN74AVC2T245RSWR	UQFN	RSW	10	3000	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
SN74AVC2T245RSWR	UQFN	RSW	10	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q1

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# PACKAGE MATERIALS INFORMATION

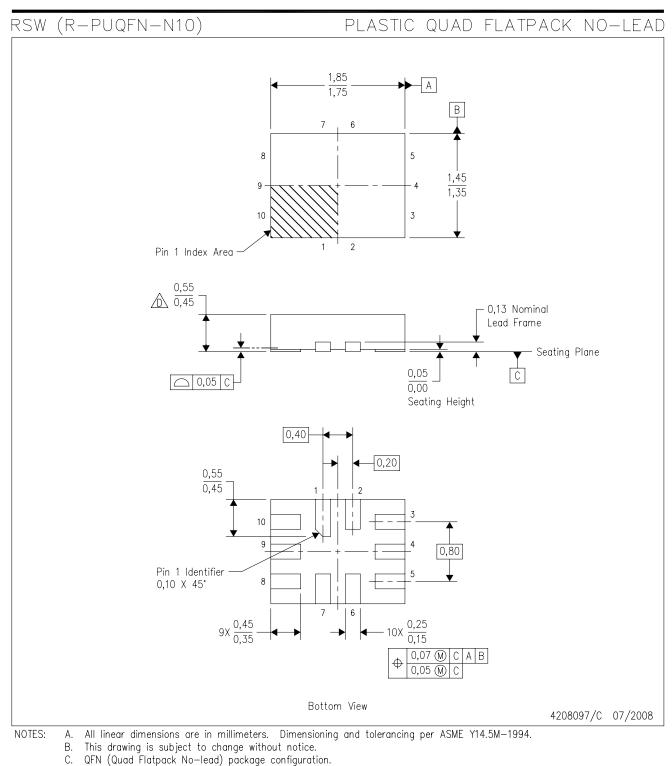
3-Aug-2017



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AVC2T245RSWR	UQFN	RSW	10	3000	189.0	185.0	36.0
SN74AVC2T245RSWR	UQFN	RSW	10	3000	202.0	201.0	28.0
SN74AVC2T245RSWR	UQFN	RSW	10	3000	203.0	203.0	35.0
SN74AVC2T245RSWR	UQFN	RSW	10	3000	184.0	184.0	19.0

# **MECHANICAL DATA**

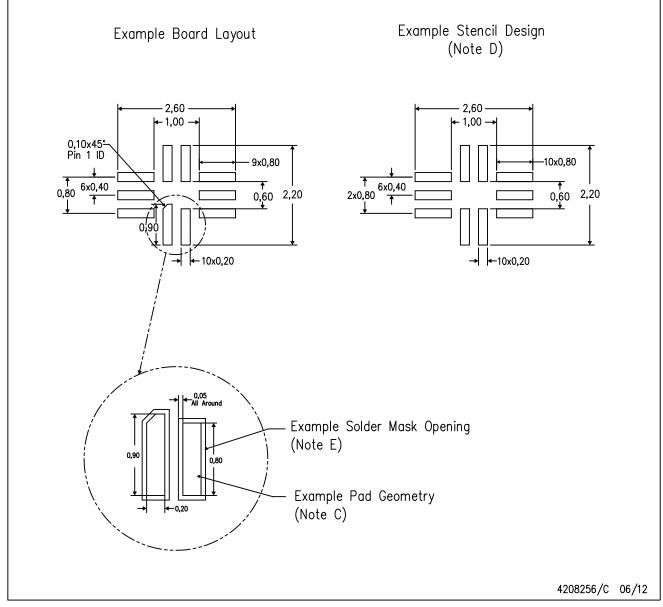


This package complies to JEDEC MO-288 variation UDEE, except minimum package height.



RSW (R-PUQFN-N10)

PLASTIC QUAD FLATPACK NO-LEAD



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- E. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.



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