普誠科技股份有限公司
Princeton Technology Corp.
Tel:886-2-66296288
Fax:886-2-29174598
URL:http://www.princeton.com.tw

DESCRIPTION

PT6523 is an LCD Driver IC which can drive up to 156 segments. It can be used for frequency display in microprocessor-controlled radio receiver and in other display applications. PT6523 supports both 1/2 bias, 1/3 duty and 1/3 duty, 1/3 bias. Pin assignments and application circuit are optimized for easy PCB layout and cost saving advantages.

FEATURES

- Up to 156 Segments Outputs
- 1/3 Duty - 1/2 Bias and 1/3 Duty - 1/3 Bias Drive Techniques
- Power Saving Mode and all Segments OFF Function
- Direct Display of Display Data without using a Decoder
- RC Oscillation Circuit
- Power Supply Voltage: 4.5 to 6V
- LCD Drive Bias Voltage can be provided internally or externally
- Available in 64 pins LQFP

APPLICATIONS

- Electronic Dictionary / Translator
- P.O.S.
- Caller ID
- Pager
- Mini Compo
- Electronic Equipment with LCD Display

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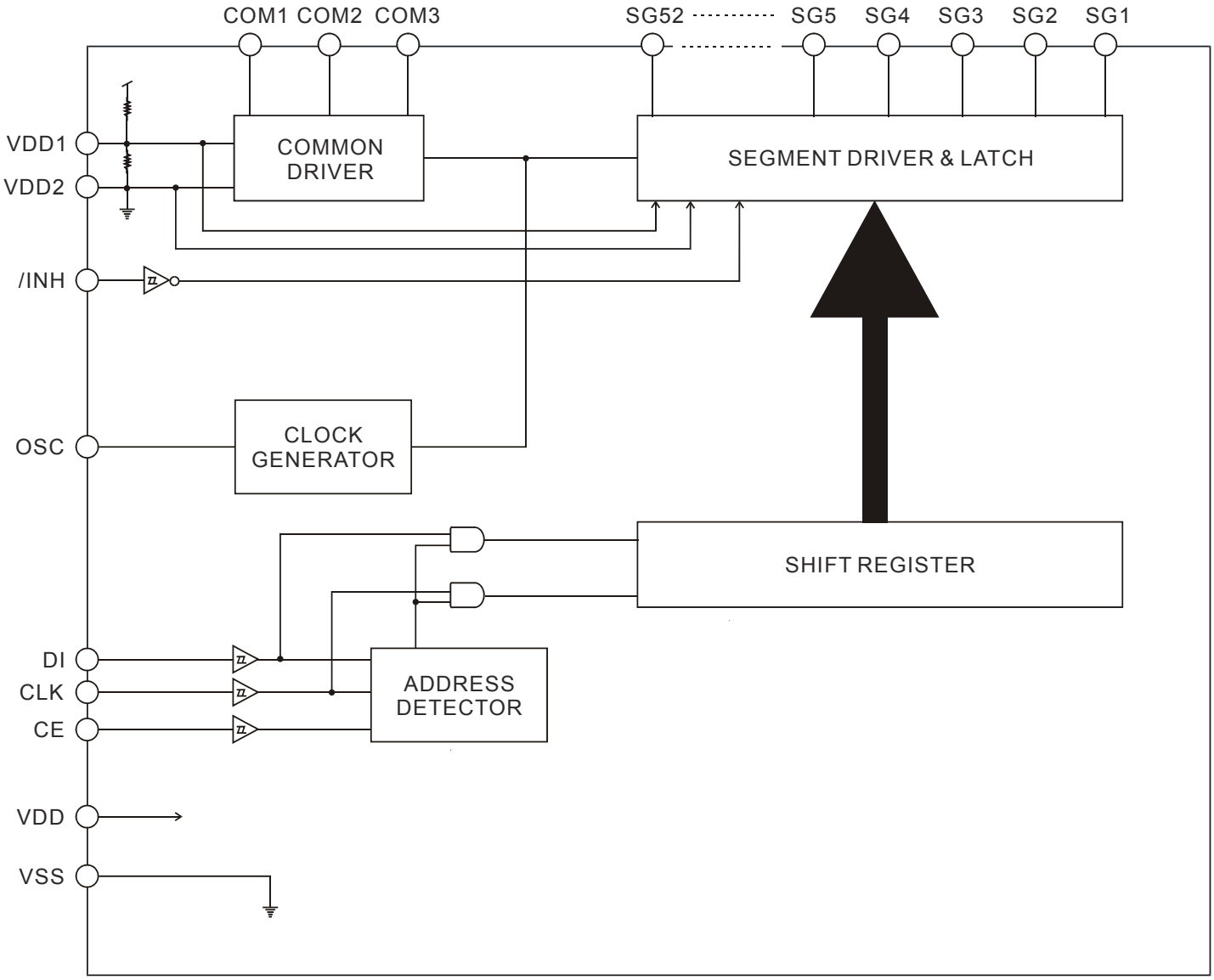
BLOCK DIAGRAM



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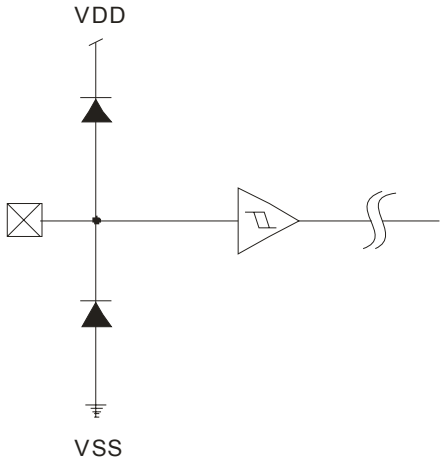
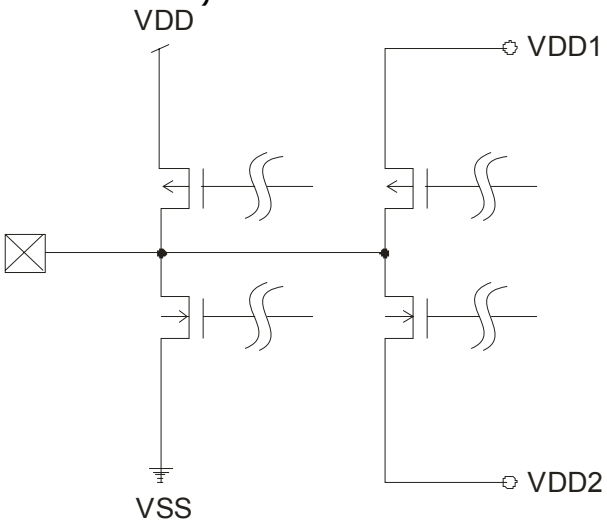
INPUT/OUTPUT CONFIGURATIONS

The schematic diagrams of the input and output circuits of the logic section are shown below:

INPUT PIN: CLK, CE, DI



OUTPUT PIN: COM1 TO COM3, SG1 TO SG52



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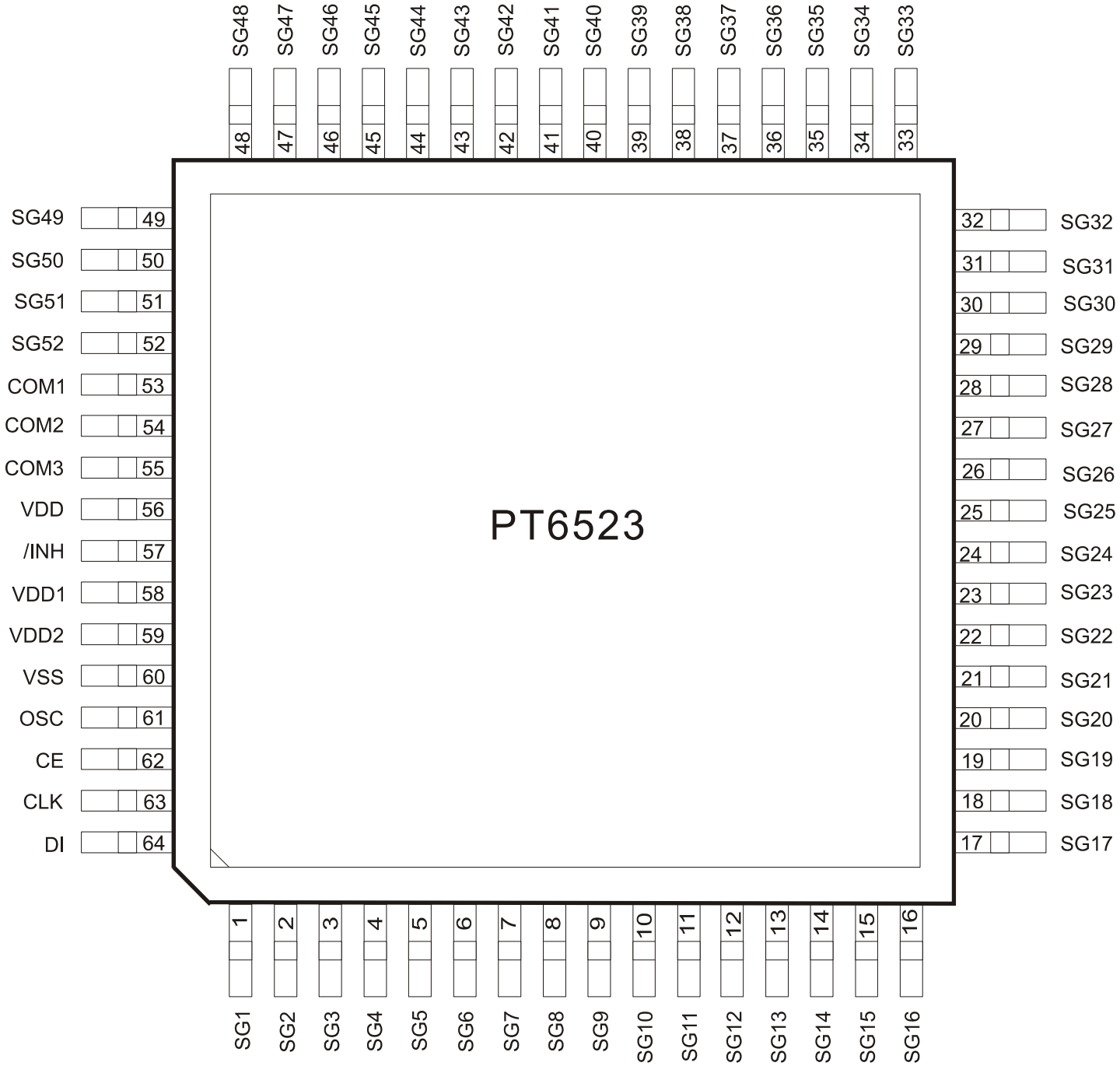
PIN CONFIGURATION



PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
SG1 to SG52 COM1 to COM3	O	Segment Output Pins Common Driver Output Pins	1 to 52 53 to 55
VDD	-	Power Supply	56
/INH	I	Display OFF Control Input Pin When this pin is Low, the display is forcibly turned off. (SG1~SG52, COM1~COM3 are set to Low) (see Note)	57
VDD1	I	Used for the 2/3 Bias Voltage when the Bias Voltages are provided externally. Connect to VDD2 when 1/2 bias is used.	58
VDD2	I	Used for 1/3 Bias Voltage when the Bias Voltage are provided externally. Connect to VDD1 when 1/2 Bias is used.	59
VSS	-	Ground Pin	60
OSC	I/O	Oscillation Input/Output Pin	61
CE	I	Chip Enable Pin	62
CLK	I	Synchronization Clock	63
DI	I	Transfer Data Pin	64

Note: When /INH = Low: Serial data transfers can be performed when the display is forcibly off.

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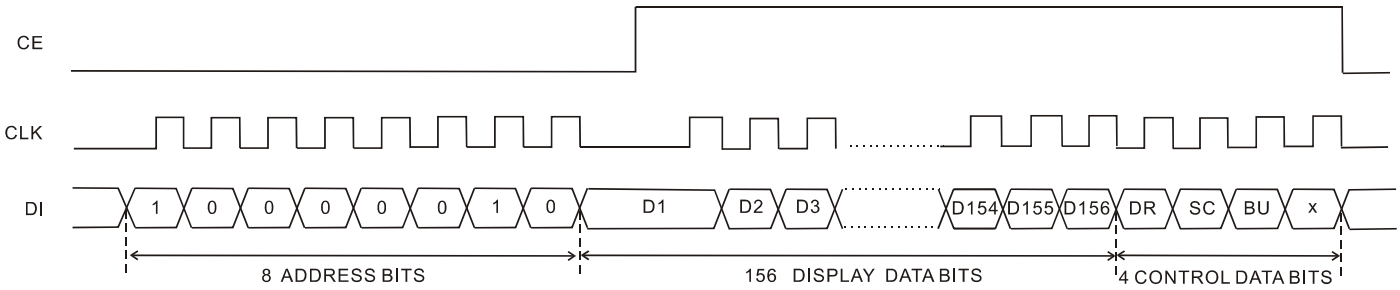
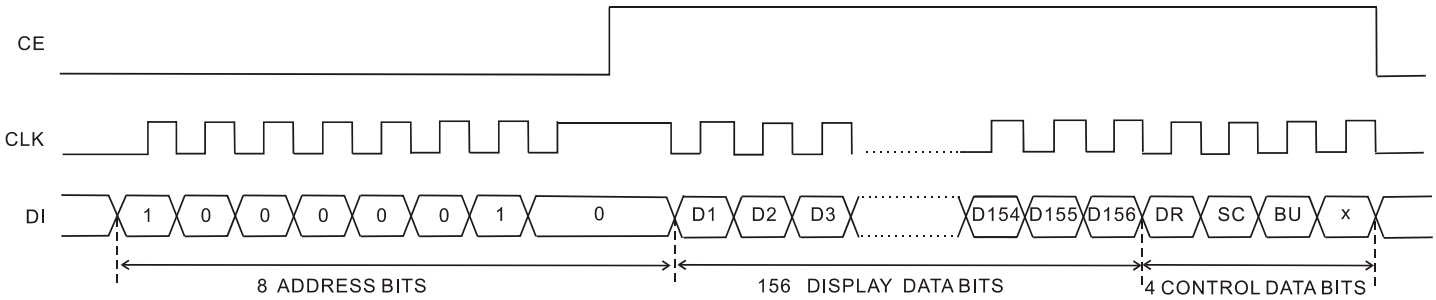
FUNCTION DESCRIPTION

SERIAL DATA TRANSFER

CONDITION 1: CLK IS TERMINATED AT THE "LOW" LEVEL



CONDITION 2: CLK IS TERMINATED AT THE "HIGH" LEVEL



Notes:
1. Address: 41H
2. D1 to D156 = Display Data
   When D1 to D156 are set to "1", Display is turned ON.
   When D1 to D156 are set to "0", Display is turned OFF.
3. DR = 1/2 Bias Drive or 1/3 Bias Drive Switching Control Data
4. SC = Segment ON/OFF Control Data
5. BU = Normal Mode/Power-Saving Control Data
6. x = Not Relevant

For example, there are 63 segments that are being used, the 63 bits of display data (D94 to D156) must be sent. Please refer to the diagram below.

8 BITS									67 BITS										
1	0	0	0	0	0	1	0		D94	D95	D96		D154	D155	D156	DR	SC	BU	X

←---------- ADDRESS ----------→

Note: x = Not Relevant

CONTROL DATA

DR: 1/2 BIAS DRIVE OR 1/3 BIAS DRIVE SWITCHING CONTROL DATA.

DR is the 1/2 bias drive or 1/3 bias drive switching control data bit. It is used to select either 1/2 bias drive or 1/3 bias drive. When this pin is set to “0” the 1/2 bias drive is selected. When this pin is set to “1’, the 1/3 bias drive is selected. Please refer to the table below for the DR settings.

DR	Drive Type
“0”	1/2 Bias Drive
“1”	1/3 Bias Drive

SC: SEGMENT ON/OFF CONTROL DATA

SC is the Segment ON/OFF Control Data Bit. It is used to select the state of the segments. If the SC is set to “0”, then the Segment Display are turned ON, however, if the SC is set to “1”, the Display State is OFF. Please refer to the table below.

SC	Display State
“0”	ON
“1”	OFF

It should be noted that when the segments are turned off via the SC setting (SC=”1”), the segments are turned off the outputting of the segment OFF waveforms from the Segment Output Pins.

BU: NORMAL MODE/POWER SAVING MODE CONTROL DATA BIT

BU is the Normal Mode/Power Saving Mode Control Data Bit. It is used to select either the Normal Mode or the Power saving Mode. When the BU is set to “0”, the Normal Mode is enabled, however, if the BU is set to “1”, the Power saving Mode is active. It should be noted that under the Power Saving Mode, the Oscillation (OSC Pin) is stopped and the Common and Segment Pins output Vss levels.

BU	Mode Selected
“0”	Normal Mode
“1”	Power Saving Mode

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/INH AND DISPLAY CONTROL

When power is first applied, the PT6523 internal data are not defined (D1 to D156, DR, SC and BU). The display is turned off (SG1 to SG52, COM1 to COM3 are all set to “Low” Level) by setting the /INH pin to “Low” at the same time the power is applied. (Please note that when the /INH Pin is set to “LOW”, the OSC Pin is not active.) As a result of this, irrelevant display at the time of the power ON can be eliminated if not prevented by transferring the serial data from the controller while the display is OFF and by setting the /INH pin after the transfer is completed. Please refer to figures below.

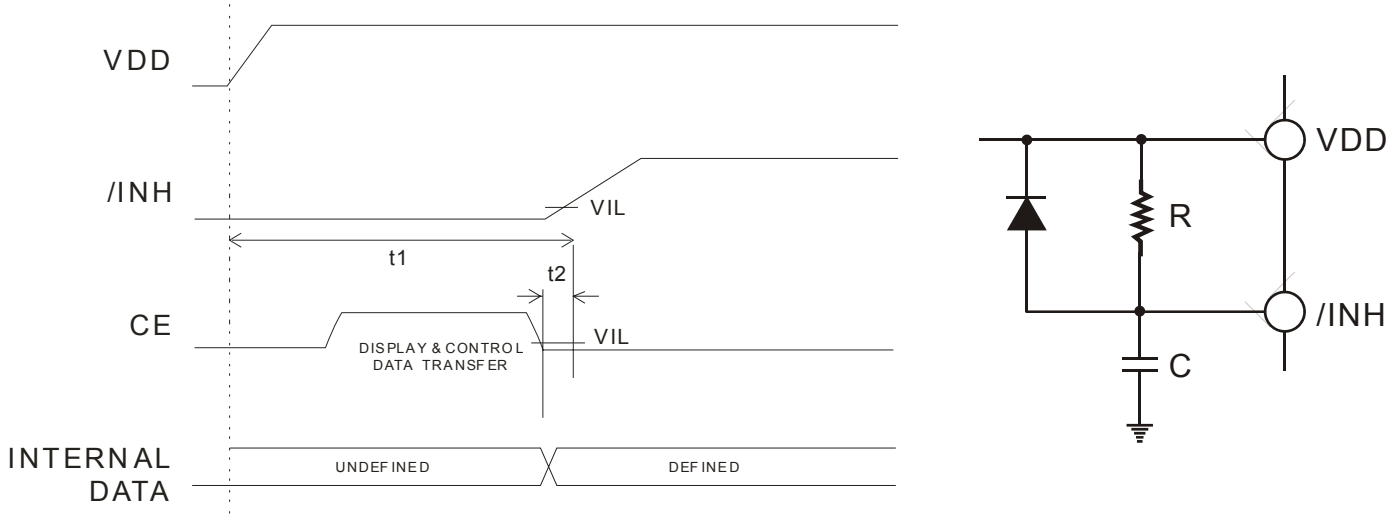


Figure 1

where:
1. t1 is determined by the value of C and R.
2. t2=10μs (minimum)
3. Vcc=4.5V to 6.0V

DISPLAY DATA TO SEGMENT OUTPUT PIN CORRESPONDENCE

Segment Output Pin	COM3	COM2	COM1
SG1	D1	D2	D3
SG2	D4	D5	D6
SG3	D7	D8	D9
SG4	D10	D11	D12
SG5	D13	D14	D15
SG6	D16	D17	D18
SG7	D19	D20	D21
SG8	D22	D23	D24
SG9	D25	D26	D27
SG10	D28	D29	D30
SG11	D31	D32	D33
SG12	D34	D35	D36
SG13	D37	D38	D39
SG14	D40	D41	D42
SG15	D43	D44	D45
SG16	D46	D47	D48
SG17	D49	D50	D51
SG18	D52	D53	D54
SG19	D55	D56	D57
SG20	D58	D59	D60
SG21	D61	D62	D63
SG22	D64	D65	D66
SG23	D67	D68	D69
SG24	D70	D71	D72
SG25	D73	D74	D75
SG26	D76	D77	D78
SG27	D79	D80	D81
SG28	D82	D83	D84
SG29	D85	D86	D87
SG30	D88	D89	D90
SG31	D91	D92	D93
SG32	D94	D95	D96
SG33	D97	D98	D99
SG34	D100	D101	D102
SG35	D103	D104	D105
SG36	D106	D107	D108
SG37	D109	D110	D111
SG38	D112	D113	D114
SG39	D115	D116	D117
SG40	D118	D119	D120
SG41	D121	D122	D123

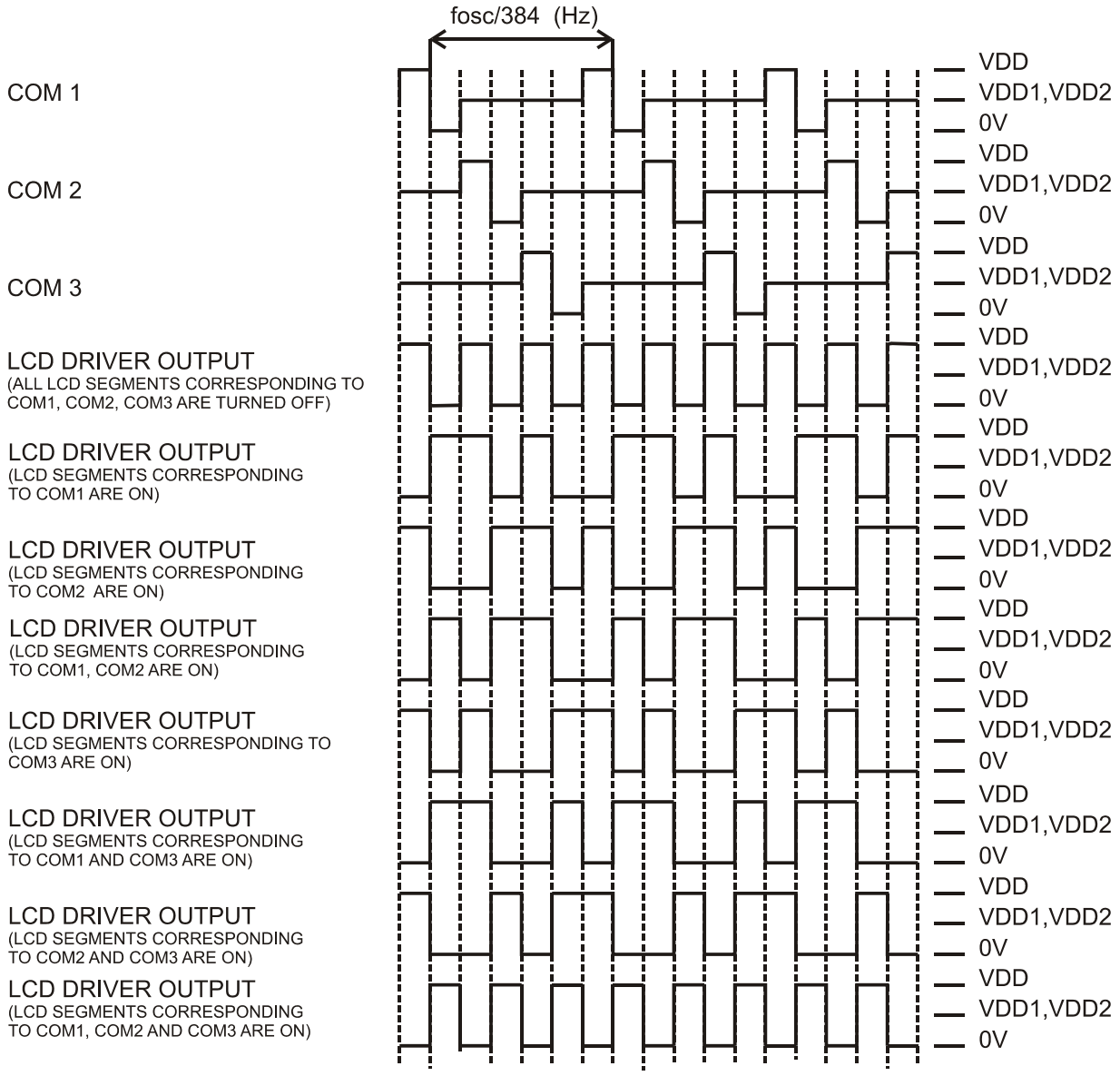
Segment Output Pin	COM3	COM2	COM1
SG42	D124	D125	D126
SG43	D127	D128	D129
SG44	D130	D131	D132
SG45	D133	D134	D135
SG46	D136	D137	D138
SG47	D139	D140	D141
SG48	D142	D143	D144
SG49	D145	D146	D147
SG50	D148	D149	D150
SG51	D151	D152	D153
SG52	D154	D155	D156

For clarity, the table below gives an example of the segment output states for the SG11 Output Pins

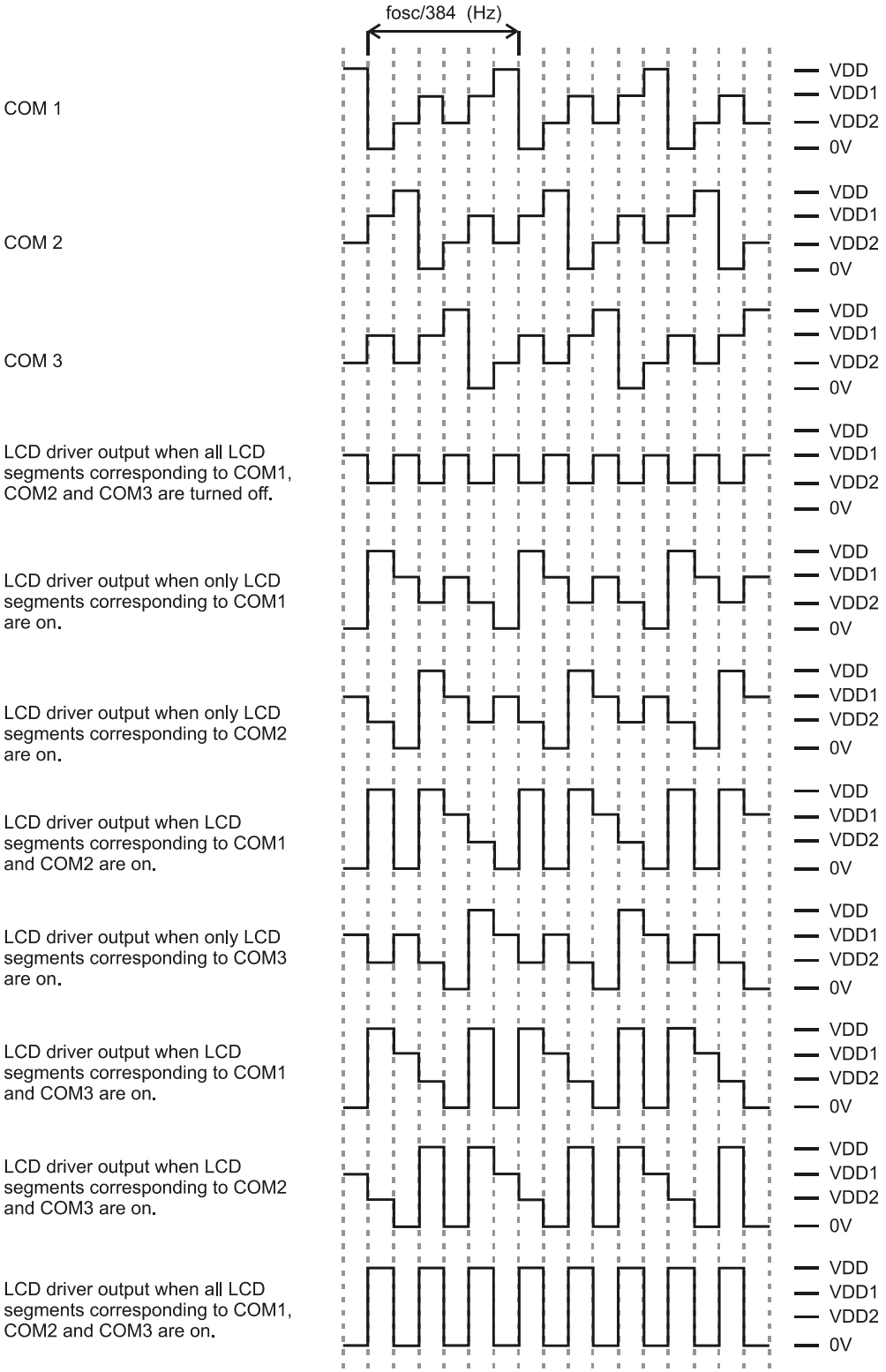
Display Data			Segment Output Pin (SG11) State Correspondence
D31	D32	D33	
0	0	0	COM1 to COM3=OFF
0	0	1	COM1=ON
0	1	0	COM2=ON
0	1	1	COM1=COM2=ON
1	0	0	COM3=ON
1	0	1	COM1=COM3=ON
1	1	0	COM2=COM3=ON
1	1	1	COM1 to COM3=ON

1/3 DUTY, 1/2 BIAS DRIVE WAVEFORMS

The 1/3 duty, 1/2 bias waveforms are shown below.



1/3 DUTY, 1/3 BIAS DRIVE WAVEFORMS



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ABSOLUTE MAXIMUM RATING

(Unless otherwise stated, Ta=25℃, Vss=0V)

Parameter	Symbol	Condition	Ratings	Unit
Maximum Supply Voltage	VDDmax	VDD	-0.3 to +6.5	V
Input Voltage	VIN1	CE, CLK, DI , /INH	-0.3 to VDD+0.3	V
	VIN2	OSC	-0.3 to VDD+0.3	V
Output Voltage	VOUT	OSC	-0.3 to VDD+0.3	V
Output Current	IOUT1	SG1 to SG52	300	uA
	IOUT2	COM1 to COM3	3	mA
Allowable Power Dissipation	Pd max	Ta=85℃	200	mW
Operating Temperature	Topr		-40 to +85	℃
Storage Temperature	Tstg		-65 to +150	℃

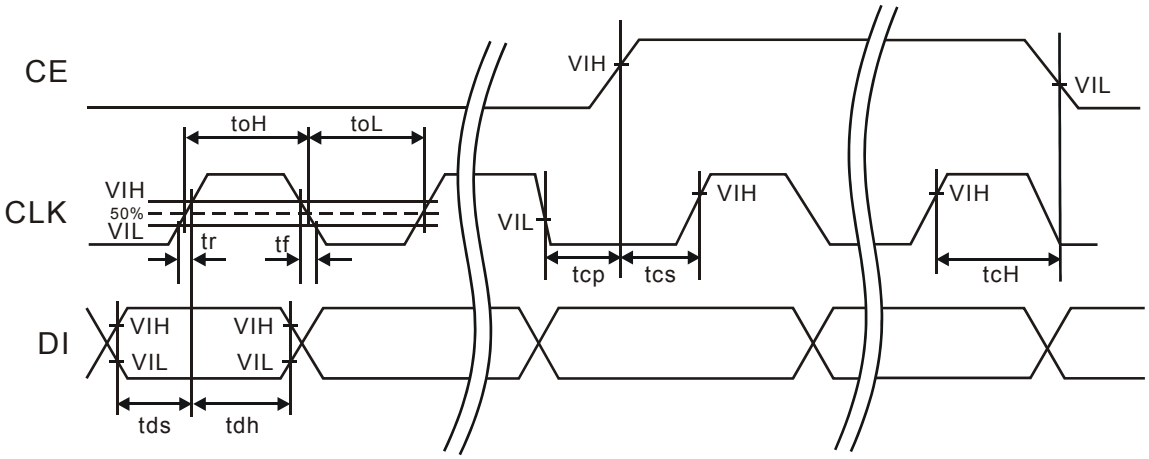
ALLOWABLE OPERATING RANGE

(Unless otherwise stated, Ta=25℃, Vss=0V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	VDD	VDD	4.5	-	6.0	V
Input Voltage	VDD1	VDD1	-	2/3VDD	VDD	V
Input Voltage	VDD2	VDD2	-	1/3VDD	VDD	V
High Level Input Voltage	VIH	CE, CLK, DI, /INH	4.0	-	VDD	V
Low Level Input Voltage	VIL	CE, CLK, DI, /INH	0	-	0.7	V
Recommended External Resistance	Rosc	OSC	-	47	-	KΩ
Recommended External Capacitance	Cosc	OSC	-	1000	-	pF
Guaranteed Oscillator Range	fosc	OSC	19	38	76	KHz
Data Setup Time *	tds	CLK, DI: Figure 2	100	-	-	ns
Data Hold Time *	tdh	CLK, DI: Figure 2	100	-	-	ns
CE Wait Time *	tcp	CE, CLK: Figure 2	100	-	-	ns
CE Setup Time *	tcs	CE, CLK: Figure 2	100	-	-	ns
CE Hold Time *	tch	CE, CLK: Figure 2	100	-	-	ns
High Level Clock Pulse Width *	toH	CLK: Figure 2	100	-	-	ns
Low Level Clock Pulse Width *	toL	CLK: Figure 2	100	-	-	ns
Rise Time *	tr	CE, CLK, DI: Figure 2	-	100	-	ns
Fall Time*	tf	CE, CLK, DI: Figure 2	-	100	-	ns
/INH, Switching Time	t2	/INH, CE: Figure 1	10	-	-	μs

Note: * = Refer to the diagrams below.

CONDITION 1: CLK IS TERMINATED AT "LOW" LEVEL



CONDITION 2: WHEN CLK IS TERMINATED AT "HIGH" LEVEL

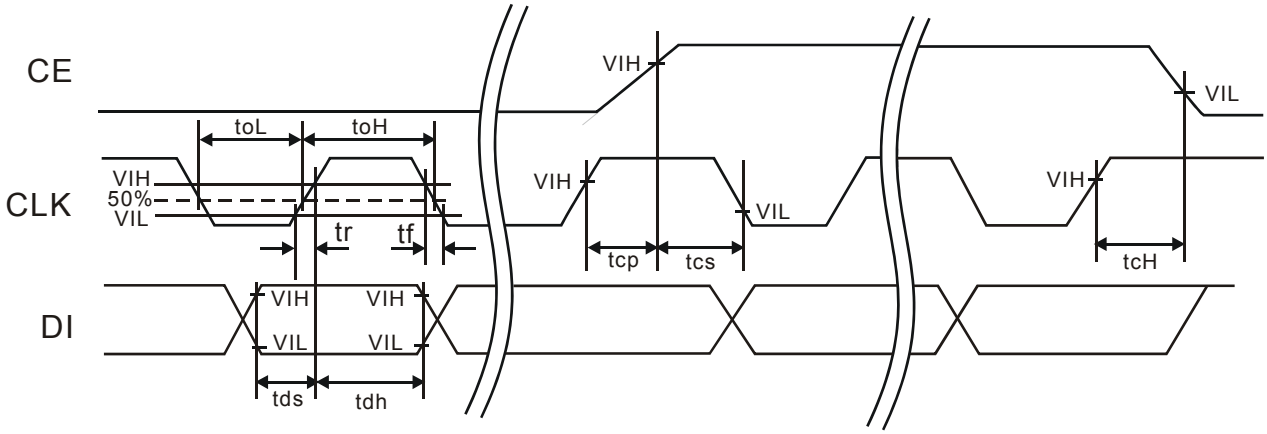


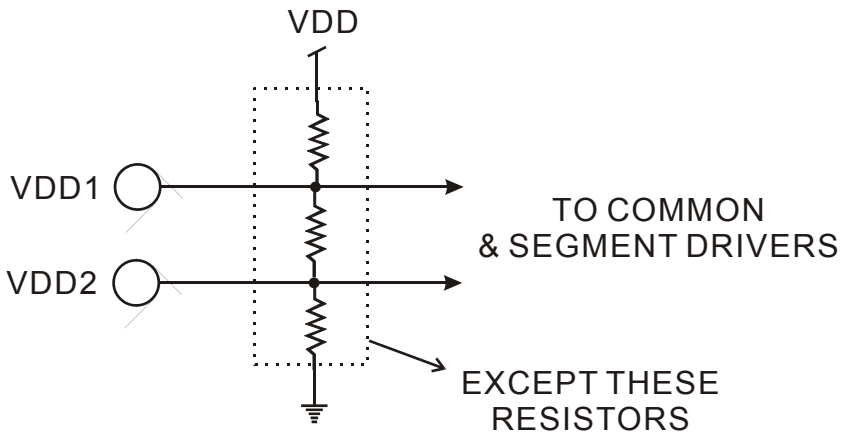
Figure 2

ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, Ta=25℃, VSS=0V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
High level input current	I_{IH}	CE, CLK, DI, /INH, VI=6V	-	-	5	μA
Low level input current	I_{IL}	CE, CLK, DI, /INH, VI=0V	-5	-	-	μA
Oscillator frequency	fosc	OSC Rosc=47KΩ	-	38	-	KHz
Hysteresis width	VH	CE, CLK, DI, /INH,VDD=5V	0.3	-	-	V
High level output voltage	VOH1	SG1 to SG52 Io=-20μA	VDD-1.0	-	-	V
Low level output voltage	VOL1	SG1 to SG52 Io=20μA	-	-	1.0	V
High level output voltage	VOH2	COM1 to COM3 Io=-100μA	VDD-1.0	-	-	V
Low level output voltage	VOL2	COM1 to COM3 Io=100μA	-	-	1.0	V
Intermediate level voltage *	VMID1	1/2 Bias, COM1 to COM3 Io=±100μA	1/2VDD-1.0	-	1/2VDD+1.0	V
	VMID2	1/3 Bias COM1 to COM3 Io=±100μA	2/3VDD -1.0	-	2/3VDD +1.0	V
	VMID3	1/3 Bias COM1 to COM3 Io=±100μA	1/3VDD-1.0	-	1/3VDD+1.0	V
	VMID4	1/3 Bias SG1 to SG52 Io=±20μA	2/3VDD-1.0	-	2/3VDD+1.0	V
	VMID5	1/3 Bias SG1 to SG52 Io=±20μA	1/3VDD-1.0	-	1/3VDD+1.0	V
Supply current	IDD1	Power Saving Mode	-	-	5	μA
	IDD2	f=38KHz, 1/2 Bias VDD=5V	-	400	800	μA
	IDD3	f=38KHz, 1/3 Bias VDD=5V	-	300	600	μA
	IDD2	f=38KHz, 1/2Bias VDD=6V	-	650	1300	μA
	IDD3	f=38KHz, 1/3 Bias VDD=6V	-	580	1200	μA

Note: * = Except the Bias Voltage Generation Divider Resistors that are built-into the VDD1 and VDD2 (Please refer to the figures below)



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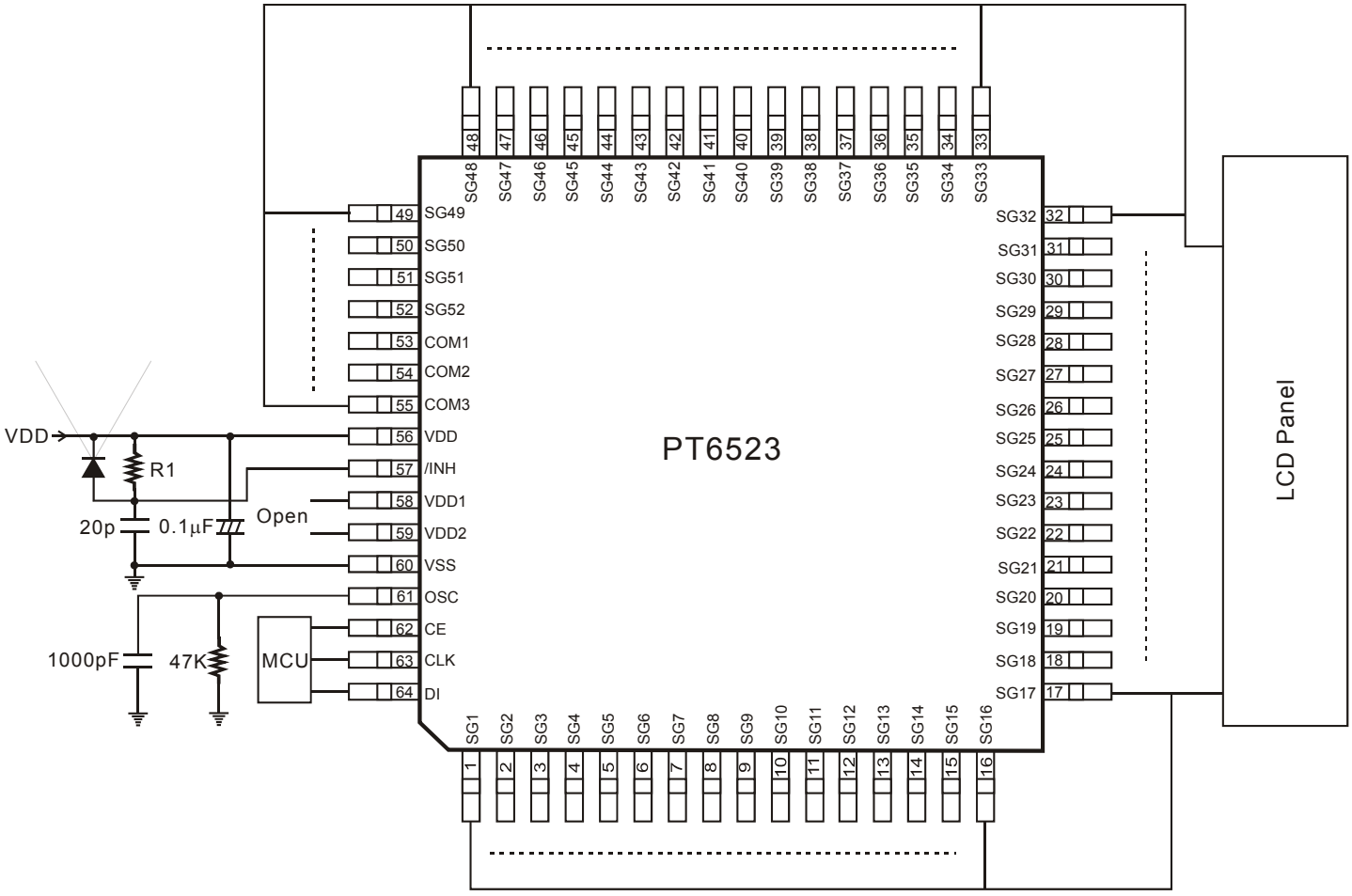
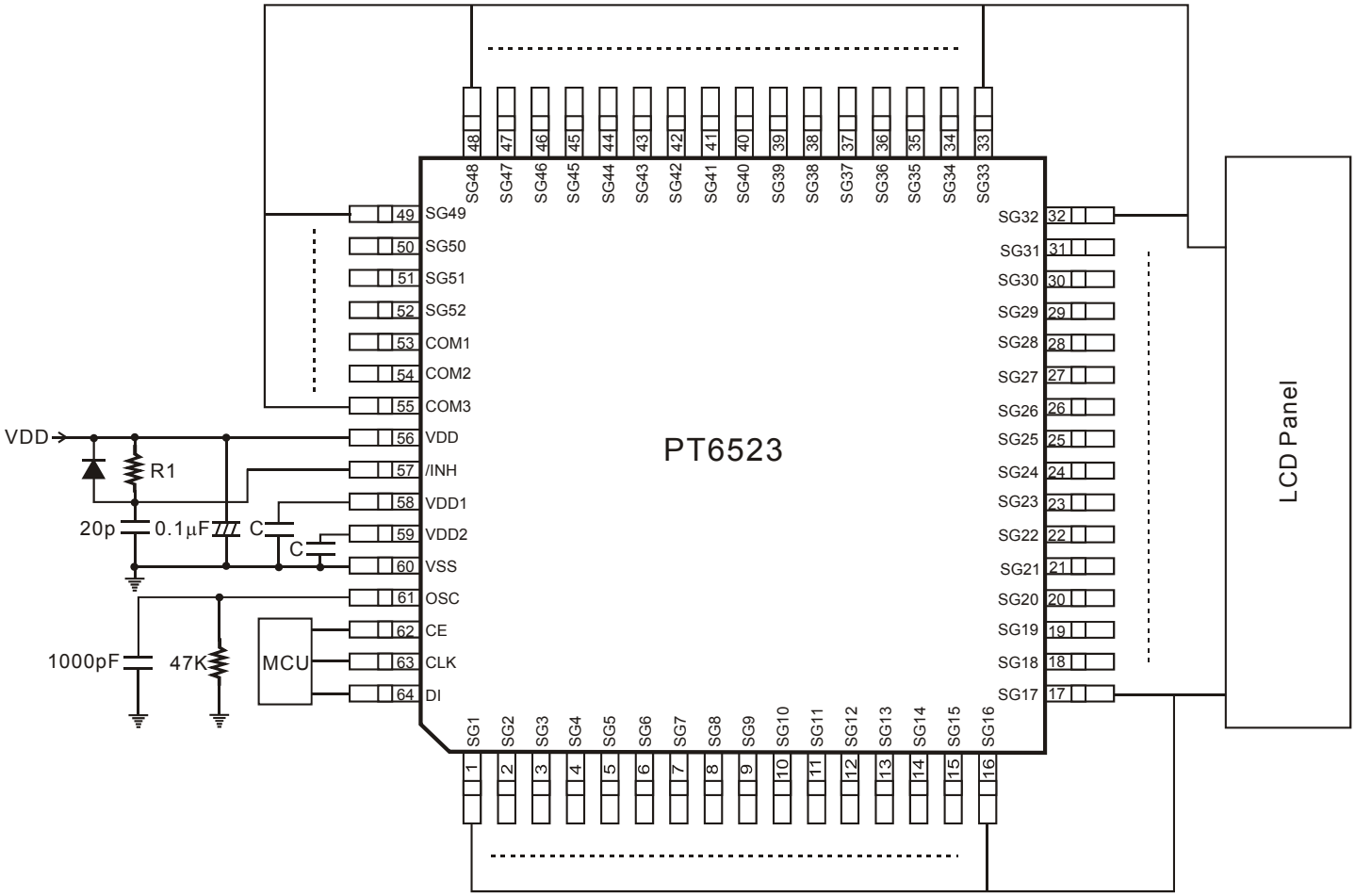
APPLICATION CIRCUITS

1/3 BIAS (FOR SMALL DISPLAY PANEL)



Note: 39KΩ ≥ R1 ≥ 10KΩ

1/3 BIAS (FOR NORMAL SIZE DISPLAY PANELS)



Notes:
1. 39KΩ ≥ R1 ≥ 10KΩ
2. C ≥ 0.047μF

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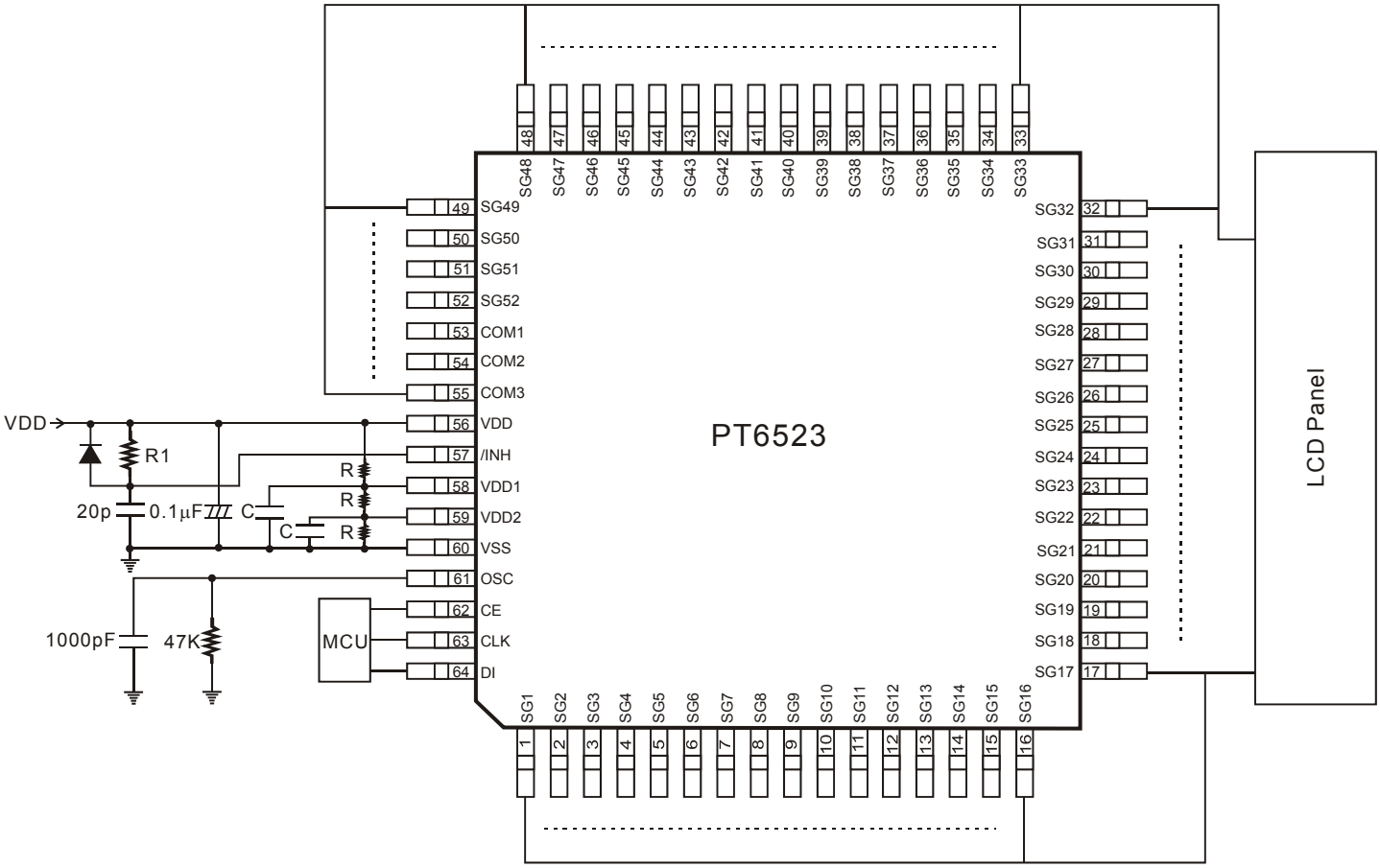
1/3 BIAS (FOR LARGE PANELS)



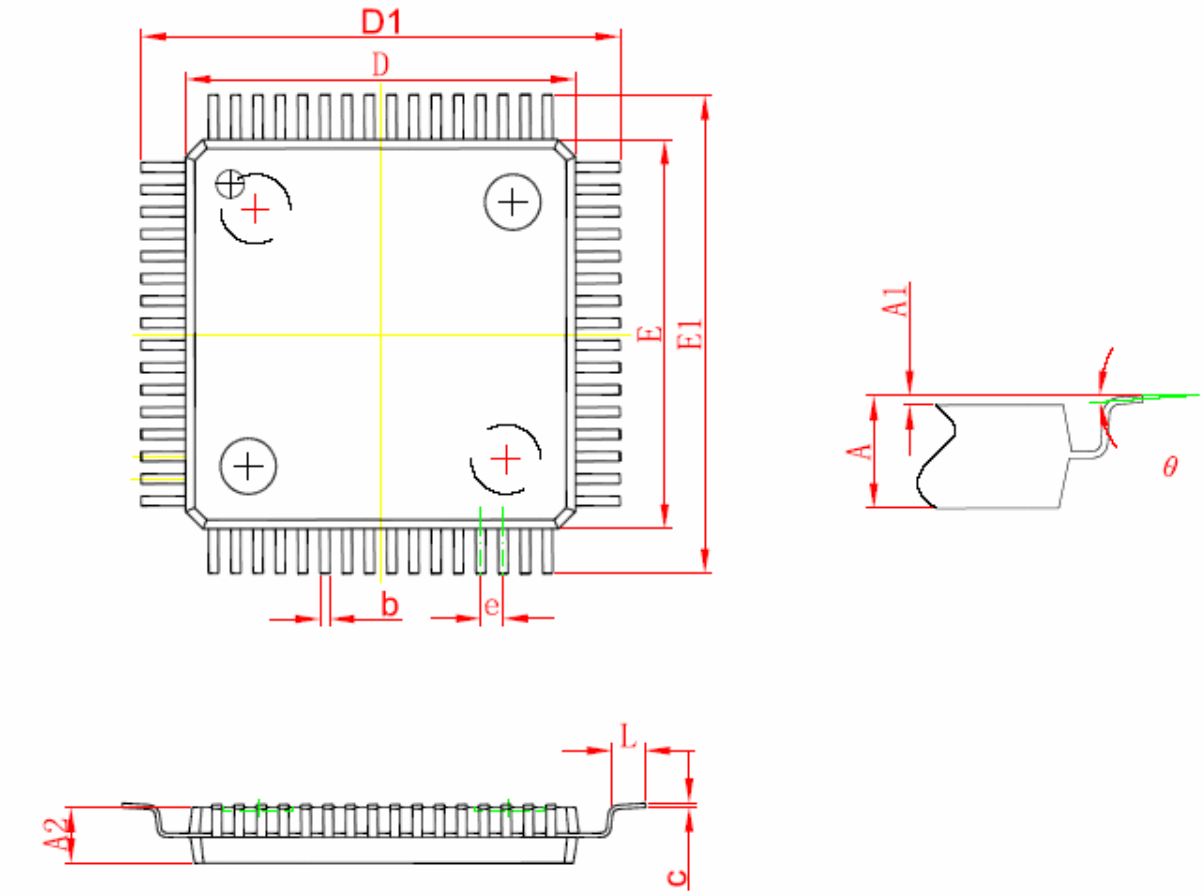
Notes:
1. 39KΩ ≥ R1 ≥ 10KΩ
2. C ≥ 0.047μF
3. 10KΩ ≥ R ≥ 1KΩ

ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT6523-HQ	64 Pins, LQFP(14x14mm)	PT6523-HQ
PT6523-LQ	64 Pins, LQFP(10x10mm)	PT6523-LQ

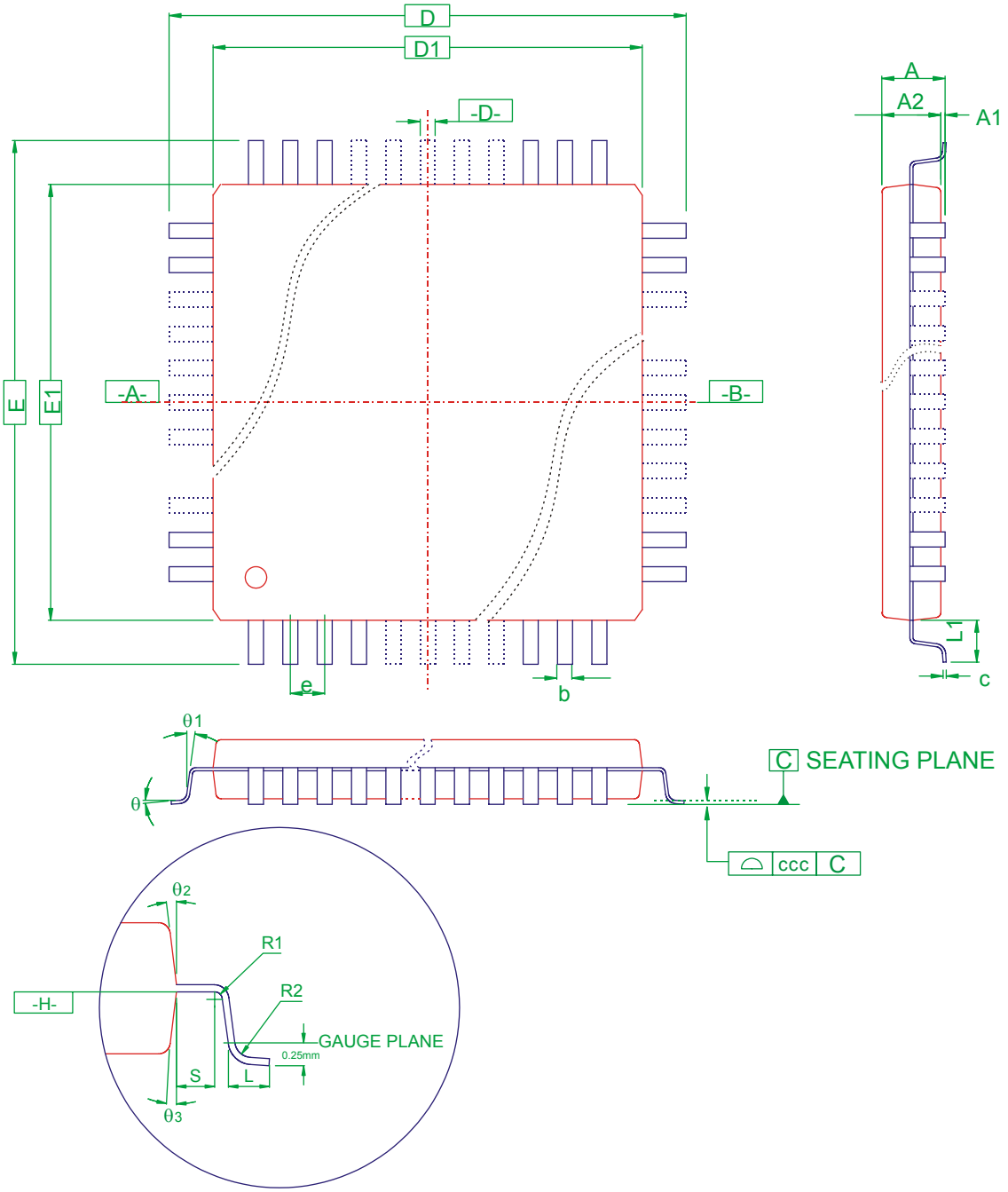
PACKAGE INFORMATION

64 PINS, LQFP PACKAGE (BODY SIZE: 14MM X 14MM, PITCH: 0.80MM)



Symbol	Min.	Max.
A	-	2.45
A1	0.05	0.250
A2	1.80	2.200
b	0.300	0.420
c	0.110	0.230
D	13.900	14.100
D1	17.050	17.350
E	13.900	14.100
E1	17.050	17.350
e	0.80BSC.	
L	0.730	1.030
θ	0°	7°

64 PINS, LQFP PACKAGE (BODY SIZE: 10MM X 10MM, PITCH:0.50MM, THK BODY: 1.40MM)



Symbol	Min.	Nom.	Max.
c	0.09	-	0.20
L	0.45	0.60	0.75
L1		1.00 REF.	
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
D		12.00 BSC.	
D1		10.00 BSC.	
E		12.00 BSC.	
E1		10.00 BSC.	
e		0.50 BSC.	
R1	0.08	-	-
R2	0.08	-	0.20
S	0.20	-	-
θ	0°	3.5°	7°
θ1	0°	-	-
θ2	11°	12°	13°
θ3	11°	12°	13°
ccc		0.08	

Notes:
1. All dimensioning and tolerancing conform to ASME Y14.5M - 1994.
2. Datums A-B and D to be determined at datum plane H.
3. Dimensions D1 and E1 do not include mold prortrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 do include mold mismatch and are determined at the datum plane H.
4. Controlling Dimension: MILLIMETERS.
5. Dimension b does not include dambar protrusion. The dambar protrusion (s) shall not cause the lead width to exceed b maximum by more than 0.08 mm. Dambar cannot be located on the lower radius or the lead foot. minimum space between protrusion and as adjacent lead is 0.07 mm for 0.4mm and 0.5mm pitch packages.
6. A1 is defined as the distance from the seating plane to the lowest point of the package body.
7. Refer to JEDEC MS-026 Variation BCD.

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