AU6353

USB2.0 Hub-Reader Controller

Technical Reference Manual

Rev. 1.01

Apr, 2015

AU6353

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Revision History

Date	Revision	Description
Jul 2014	1.00	Official Release
Apr 2015	1.01	Modify 1.2 Feature and Table 3.1 Pin Descriptions

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1. Introduction

1.1 Description

AU6353 is a single chip integrated USB2.0 hub and SD/MMC/MS card reader controller.

1.2 Features

HUB

- Fully compliant with USB Hub Specification version 2.0 and is also backward compatible with USB Hub specification 1.1
- Single chip USB 2.0 hub controller.
- Supports four bus-powered/self-powered downstream ports.
- Supports automatic switching between bus-power and self-power modes.
- Cost effective design using one transaction translator for all downstream ports.
- Extra low power consumption.
- Built-in USB 2.0 transceiver.
- Supports gang modes of power management.
- Built-in power enabling control and over current sensing control for power switch application.
- Built-in 1.8V regulator for core logic.
- Embedded in PLL (Phase Lock Loop) circuit for 12MHz operation precision.
- Available in two different form factors: 48-pin LQFP package.

Card Reader

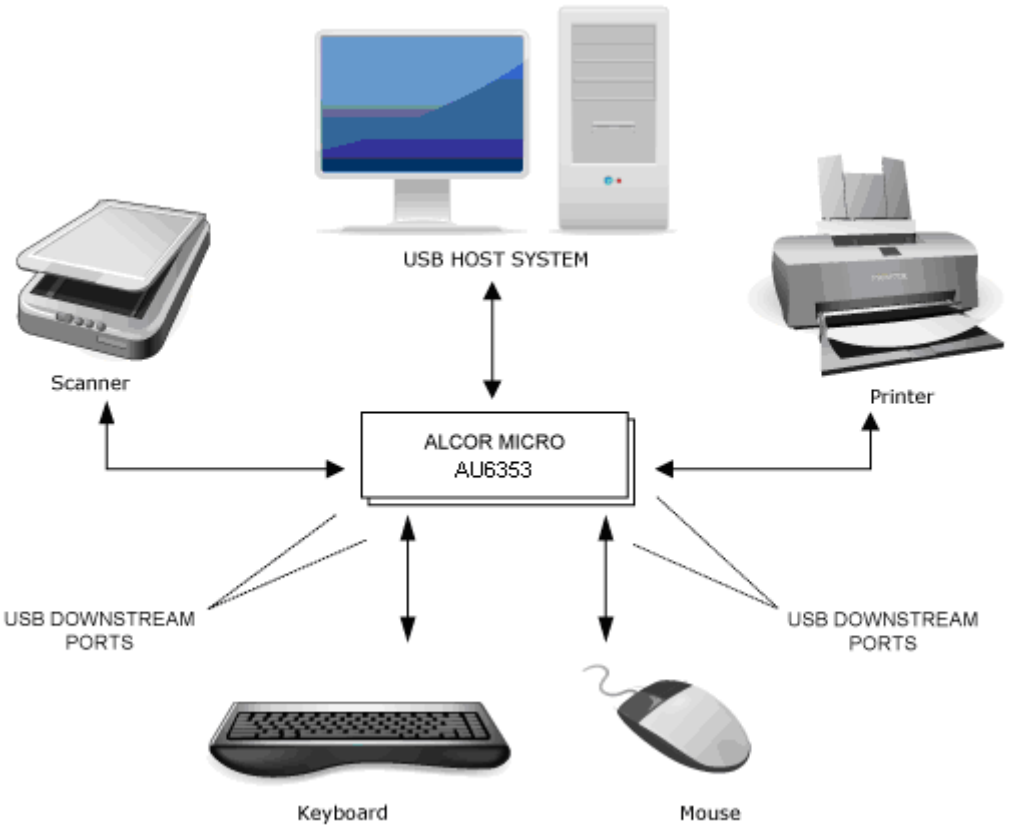
- Supports both Windows
  -Default Mass Storage Class driver comes from Windows ME/2000/XP/Vista/ Windows 7/ Windows 8
  -Windows 98 is supported by vendor driver from Alcor
- Complies with USB Device Class Definition for Mass Storage and Bulk-Transport V1.0
- Complies with Secure Digital Card (SD) specification up to ver. 3.0(SDXC)
- Complies with MultiMedia Card (MMC) specification up to ver. 4.4 and supports 8-bit data bus.

- Complies with Memory Stick (MS) specification up to ver. 1.43
- Complies with Memory Stick PRO (MS_Pro) specification up to ver. 1.05
- Complies with Memory Stick PRO-HG (MS PRO-HG) specification up to ver. 1.03 and supports 8-bit data bus.
- Complies with Memory Stick XC(MSXC) specification up to ver. 1.00-00
- Integrated hardware DMA engine enhances overall performance of data transfers
- 1K bytes of ping-pong FIFO buffs the data transmission between transmitter and receiver
- User-friendly Dynamic icon utility software can display icon message upon insertion/removal of compatible flash cards under Windows
- Optimizes performance via multiple sectors transfer
- Built-in 3.3V to 1.8V regulators offer customers lower BOM cost
- Built-in MOSFET with 400mA capability for card power control of all types memory cards

2. Application Block Diagram

AU6353 is a single chip 3-port USB Hub-Reader controller. Its upstream port is connected to a USB Host system. The downstream ports can be used for a mouse, joystick, scanner, printer or other devices.

Figure 2.1 Block Diagram



3. Pin Assignment

AU6353 is available in 48-pin LQFP package. Below diagram shows signal name of each pin and table in the following page describes each pin in detail.

Figure 3.1 AU6353 Pin Assignment Diagram

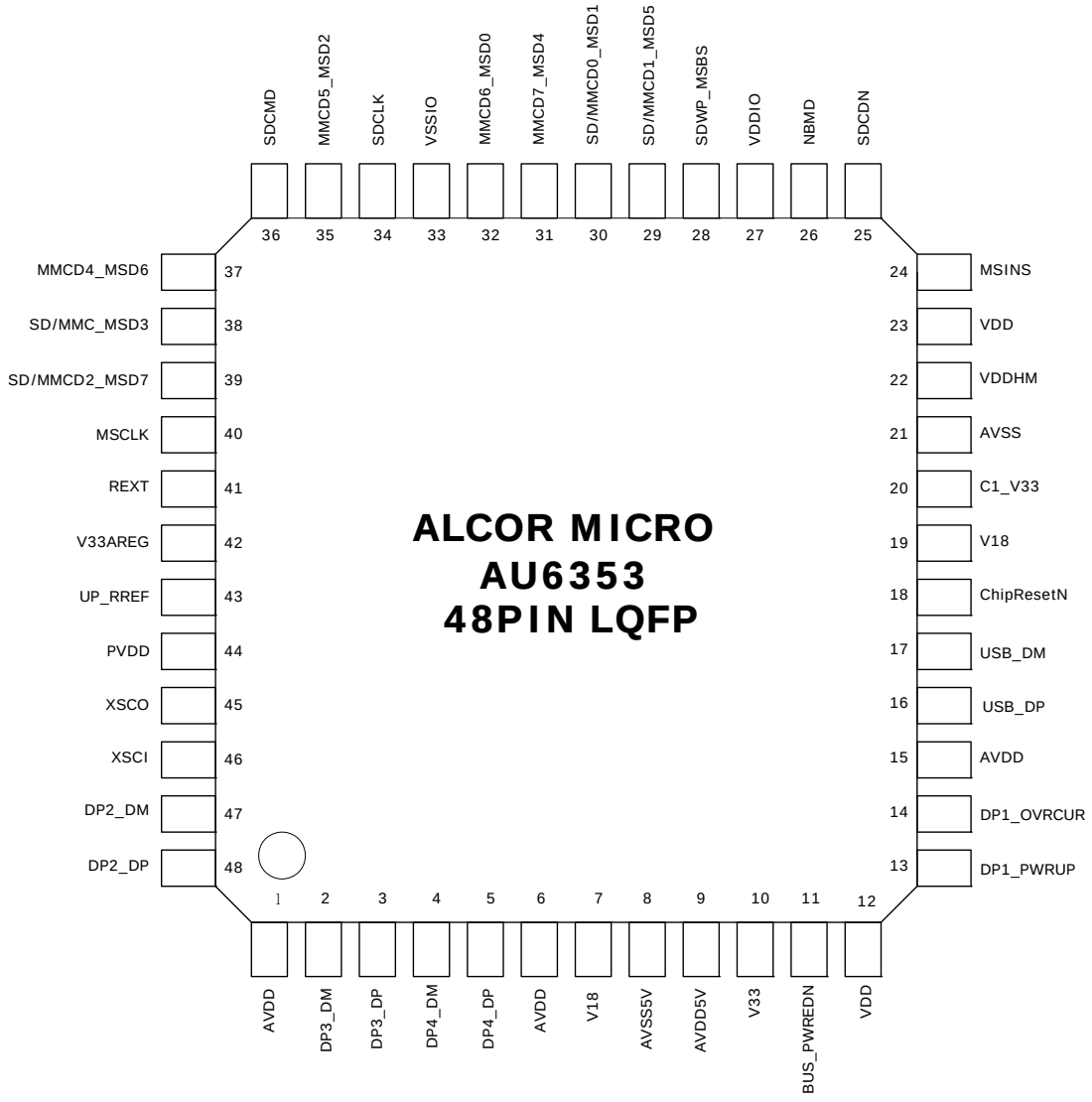


Table 3.1 AU6353 Pin Descriptions

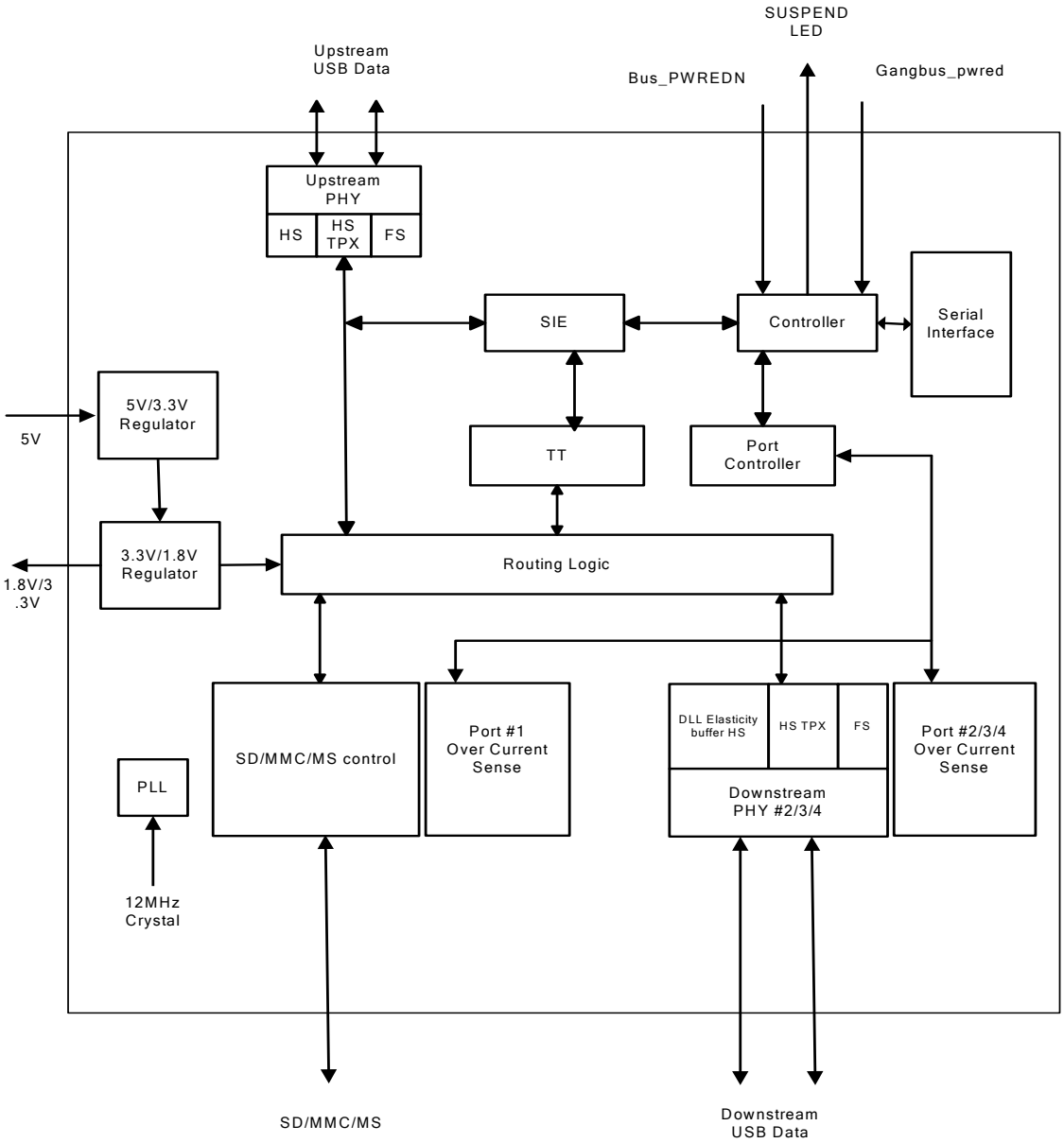
Pin #	Pin Name	I/O	Description
1	AVDD	UTMI	UTMI Power input 3.3V
2	DP3_DM	UTMI	Port3 USB bus
3	DP3_DP	UTMI	Port3 USB bus
4	DP4_DM	UTMI	Port4 USB bus
5	DP4_DP	UTMI	Port4 USB bus
6	AVDD	UTMI	UTMI Power input 3.3V
7	V18	Power	Voltage regulator output 1.8V
8	AVSS5V	Power	Voltage regulator GND
9	AVDD5V	Power	Voltage regulator input 5V
10	V33	Power	Voltage regulator output 3.3V
11	BUS_PWREDN	O	'1' = Self Powered '0' = Bus Powered
12	VDD	Power	Core Power input 1.8V
13	DP1_PWRUP	I/O	Port1 Power Enable '0' = power on ; '1' = power off
14	DP1_OVRCUR	I	Port 1 Over current '0' = over current '1' = not over current
15	AVDD	UTMI	UTMI Power
16	USB_DP	UTMI	Upstream port USB bus
17	USB_DM	UTMI	Upstream port USB bus
18	ChipResetN	I	'0' = Reset ; '1' = Normal
19	V18	O	Regulator 1.8V Out
20	C1_V33	O	Regulator 3.3V Card Power Output
21	AVSS	I	Regulator Ground
22	VDDHM	I	Pad 3.3V Power
23	VDD	I	Core 1.8V Power
24	MSINS	I	MSINS ("0":Detected; "1":Undetected)
25	SDCDN	I	SDCDN ("0":Detected; "1":Undetected)
26	NBMD	I	Notebook mode. '0' for normal mode '1' notebook mode [Default]
27	VDDIO	I	HS IO Pad Power
28	SDWP_MSBS	I/O	SDWP/MSBS

Pin #	Pin Name	I/O	Description
29	SD/MMCD1_MSD5	I/O	SD/MMC DATA1/ MS DATA5
30	SD/MMCD0_MSD1	I/O	SD/MMC DATA0/ MS DATA1
31	MMCD7_MSD4	I/O	MMC DATA7/ MS DATA4
32	MMCD6_MSD0	I/O	MMC DATA6/ MS DATA0
33	VSSIO	I	HS IO Pad Ground
34	SDCLK	O	SD CLK
35	MMCD5_MSD2	I/O	MMC DATA5/ MS DATA2
36	SDCMD	I/O	SD CMD
37	MMCD4_MSD6	I/O	MMC DATA4/ MS DATA6
38	SD/MMC_MSD3	I/O	SD/MMC/MS DATA3
39	SD/MMCD2_MSD7	I/O	SD/MMC DATA2/ MS DATA7
40	MSCLK	O	MS CLK
41	REXT	I/O	External Resistor 330 to Ground
42	V33AREG	I	PHY Power
43	UP_RREF	UTMI	680Ω 1% current reference resistor
44	PVDD	UTMI	PLL VDD input 3.3V
45	XSCO	UTMI	12MHz Crystal oscillator output
46	XSCI	UTMI	12MHz Crystal oscillator input
47	DP2_DM	UTMI	Port2 USB bus
48	DP2_DP	UTMI	Port2 USB bus

4. System Architecture and Reference Design

4.1 AU6353 Block Diagram

Figure 4.1 AU6353 Block Diagram



5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNITS
V_{DDH}	Power Supply	-0.3 to V_{DDH} +0.3	V
V_{IN}	Input Signal Voltage	-0.3 to 3.6	V
V_{OUT}	Output Signal Voltage	-0.3 to V_{DDH} +0.3	V
T_{STG}	Storage Temperature	-40 to 150	^{O}C

5.2 Recommended Operating Conditions

Table 5.2 Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V_{DDH}	Power Supply	3.0	3.3	3.6	V
V_{DD}	Digital Supply	1.62	1.8	1.98	V
V_{IN}	Input Signal Voltage	0	3.3	3.6	V
T_{OPR}	Operating Temperature	0		85	^{O}C

5.3 General DC Characteristics

Table 5.3 General DC Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{IN}	Input current	No pull-up or pull-down	-10	±1	10	μA
I_{OZ}	Tri-state leakage current		-10	±1	10	μA
C_{IN}	Input capacitance	Pad Limit		2.8		ρF
C_{OUT}	Output capacitance	Pad Limit		2.8		ρF
C_{BID}	Bi-directional buffer capacitance	Pad Limit		2.8		ρF

5.4 DC Electrical Characteristics of 3.3V I/O Cells

Table 5.4 DC Electrical Characteristics of 3.3V I/O Cells

SYMBOL	PARAMETER	CONDITIONS	Limits			UNIT
			MIN	TYP	MAX	
V_{D33P}	Power supply	3.3V I/O	3.0	3.3	3.6	V
V_{il}	Input low voltage	LVTTL			0.8	V
V_{ih}	Input high voltage		2.0			V
V_{ol}	Output low voltage	$\lvert I_{ol} \rvert$ =2~16mA			0.4	V
V_{oh}	Output high voltage	$\lvert I_{oh} \rvert$ =2~16mA	2.4			V
R_{pu}	Input pull-up resistance	PU=high, PD=low	55	75	110	KΩ
R_{pd}	Input pull-down resistance	PU=low, PD=high	40	75	150	KΩ
I_{in}	Input leakage current	V_{in}= V_{D33P} or 0	-10	±1	10	μA
I_{oz}	Tri-state output leakage current		-10	±1	10	μA

5.5 USB Transceiver Characteristics

Table 5.5 Electrical characteristics

SYMBOL	PARAMETER	CONDITIONS	Limits			UNIT
			MIN	TYP	MAX	
V_{D33P}	Analog supply Voltage		3.0	3.3	3.6	V
V_{DD} V_{18}	Digital supply Voltage		1.62	1.8	1.98	V
I_{CC}	Operating supply current	High speed operating at 480			55	mA

Table 5.6 Static characteristic：Analog I/O pins（DP/DM）

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
USB2.0 Transceiver (HS)						
Input Levels (differential receiver)						
V_{HSDIFF}	High speed differential input sensitivity	$\lvert V_{I(DP)}-V_{I(DM)} \rvert$ measured at the connection as application circuit	300			mV
V_{HSCM}	High speed data signaling common mode voltage range		-50		500	mV
V_{HSSQ}	High speed squelch detection threshold	Squelch detected			100	mV
		No squelch detected	150			mV
V_{HSDSC}	High speed disconnection detection threshold	Disconnection detected	625			mV
		Disconnection not detected			525	mV
Output Levels						
V_{HSOI}	High speed idle level output voltage(differential)		-10		10	mV
V_{HSOL}	High speed low level output voltage(differential)		-10		10	mV
V_{HSOH}	High speed high level output voltage(differential)		360		440	mV
V_{CHIRPJ}	Chirp-J output voltage（differential）		700		1100	mV
V_{CHIRPK}	Chirp-K output voltage（differential）		-900		-500	mV
Resistance						
R_{DRV}	Driver output impedance	Equivalent resistance used as internal chip only	3	6	9	Ω
		Overall resistance including external resistor	40.5	45	49.5	
Termination						
V_{TERM}	Termination voltage for pull-up resistor on pin RPU		3.0		3.6	V
USB1.1 Transceiver (FS)						
Input Levels（differential receiver）						
V_{DI}	Differential input sensitivity	$\lvert V_{I(DP)}-V_{I(DM)} \rvert$	0.2			V
V_{CM}	Differential common mode voltage		0.8		2.5	V
Input Levels（single-ended receivers）						

V_{SE}	Single ended receiver threshold		0.8		2.0	V
Output levels						
V_{OL}	Low-level output voltage		0		0.3	V
V_{OH}	High-level output voltage		2.8		3.6	V

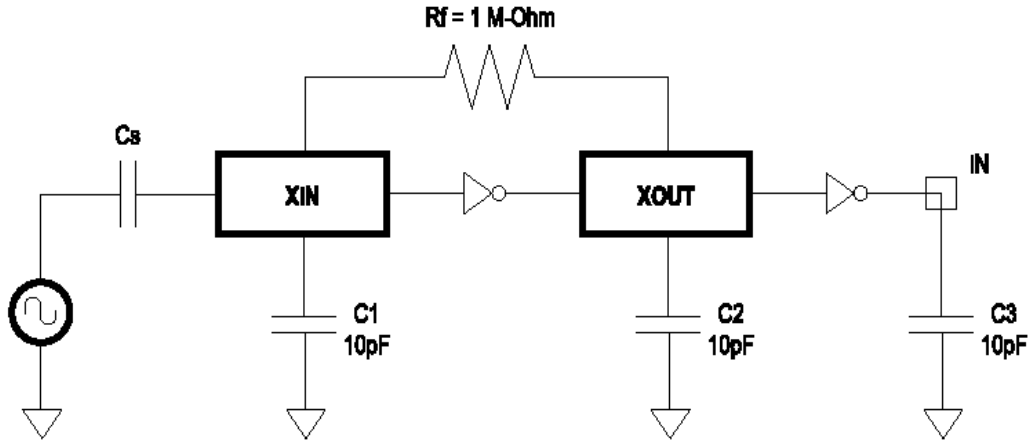
Table 5.7 Dynamic characteristic：Analog I/O pins（DP/DM）

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Driver Characteristics						
High-Speed Mode						
t_{HSR}	High-speed differential rise time		500			ps
t_{HSF}	High-speed differential fall time		500			ps
Full-Speed Mode						
t_{FR}	Rise time	CL=50pF；10 to 90％ of | V_{OH}-V_{OL} | ；	4		20	ns
t_{FF}	Fall time	CL=50pF；90 to 10％ of | V_{OH}-V_{OL} | ；	4		20	ns
t_{FRMA}	Differential rise/fall time matching（t_{FR} / t_{FF}）	Excluding the first transition from idle mode	90		110	%
V_{CRS}	Output signal crossover voltage	Excluding the first transition from idle mode	1.3		2.0	V
Low-Speed Mode						
t_{LR}	Rise time	CL=200pF-600pF；10 to 90％ of | V_{OH}-V_{OL} | ；	75		300	ns
t_{LF}	Fall time	CL=200pF-600pF；90 to 10％ of | V_{OH}-V_{OL} | ；	75		300	ns
t_{LRMA}	Differential rise/fall time matching（t_{LR} / t_{LF}）	Excluding the first transition from idle mode	80		125	%
V_{CRS}	Output signal crossover voltage	Excluding the first transition from idle mode	1.3		2.0	V
V_{OH}	High-level output voltage		2.8		3.6	V

5.6 Crystal Oscillator Circuit Setup for Characterization

The following setup was used to measure the open loop voltage gain for crystal oscillator circuits. The feedback resistor serves to bias the circuit at its quiescent operating point and the AC coupling capacitor, Cs, is much larger than C1 and C2..

Figure 5.1 Crystal Oscillator Circuit Setup for Characterization



5.7 Bus Timing/Electrical Characteristics

Table 5.8 DC Electrical Characteristics

Input Levels for Low-/Full –speed:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{IH}	High (Driven)	2.0		V
V_{IHZ}	High (floating)	2.7	3.6	V
V_{IL}	Low		0.8	V
V_{DI}	Differential Input Sensitivity	0.2		V
V_{CM}	Differential Common Mode Range	0.8	2.5	V

Input Levels for High –speed:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{HHSSQ}	High-speed squelch detection threshold (differential signal amplitude)	100	150	mV
V_{HSDSC}	High speed disconnect detection threshold (differential signal amplitude)	525	625	mV

Output Levels for Low-/Full-speed:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{OL}	Low	0.0	0.3	V
V_{OH}	High (driven)	2.8	3.6	V
V_{OSE1}	SE1	0.8		V
V_{CRS}	Output Signal Crossover Voltage	1.3	2.0	V

Output Levels for High –speed:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{HSOI}	High-speed idle level	-10	10	mV
V_{HSOH}	High-speed data signaling high	360	440	mV
V_{HSOL}	High-speed data signaling low	-10	10	mV
V_{CHIRPJ}	Chirp J level (differential voltage)	700	1100	mV
V_{CHIRPK}	Chirp K level (differential voltage)	-900	-500	mV

Terminations:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
R_{PU}	Bus Pull-up Resistor on Upstream Facing Port	1.425	1.575	kΩ
R_{PD}	Bus Pull-down Resistor on Upstream Facing Port	14.25	15.75	kΩ
Z_{INP}	Input impedance exclusive of pull-up/pull-down (for low-/full-speed)	300		kΩ
V_{TERM}	Termination voltage for upstream facing port pull-up (R_{PU})	3.0	3.6	V

Terminations in High-speed:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{HSTERM}	Termination voltage in high-speed	-10	10	mV

Table 5.9 High-speed Source Electrical Characteristics

Driver Characteristics:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
T_{HSR}	Rise Time (10%-90%)	500		ps
T_{HSF}	Fall Time (10%-90%)	500		ps
Z_{HSDRV}	Driver Output Resistance (which also serves as high-speed termination)	40.5	49.5	Ω

Clock Timings:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
T_{HSDRAT}	High-speed Data Rate	479.76	480.24	Mb/s
T_{HSFRAM}	Micorframe Interval	124.9375	125.0625	μs
T_{HSRFI}	Consecutive Microframe Interval Difference		4 high-speed bit times	

Table 5.10 Full-speed Source Electrical Characteristics

Driver Characteristics:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
T_{FR}	Rise Time	4	20	ns
T_{FF}	Fall Time	4	20	ns
T_{FRFM}	Differential Rise and Fall Time Matching	90	111.11	%
Z_{ZRV}	Driver Output Resistance for driver which is not high-speed capable	28	44	Ω

Clock Timings:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
$T_{FDRATHS}$	Full-speed Data Rate for hubs and devices which are high-speed capable	11.994	12.006	Mb/s
T_{FDRATE}	Full-speed Data Rate for devices which are not high-speed capable	11.970	12.030	Mb/s
T_{FRAME}	Frame interval	0.9995	1.0005	Ms
T_{FRI}	Consecutive Frame Interval Jitter		42	ns

Full-speed Data Timings:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
T_{DJ1} T_{DJ2}	Source Jitter Total(including frequency tolerance): To Next Transition For Paired Transitions	-3.5 -4	-3.5 -4	ns ns
T_{FDEOP}	Source Jitter for Differential Transition to SE0 Transition	-2	5	ns
T_{JR1} T_{JR2}	Receiver Jitter: To Next Transition For Paired Transitions	-18.5 -9	-18.5 -9	ns ns
T_{FEPPT}	Source SE0 interval of EOP	160	175	ns
T_{FEOPR}	Receiver SE0 interval of EOP	82		ns
T_{FST}	Width of SE0 interval during differential transition		14	ns

Table 5.11 Low-speed Source Electrical Characteristics

Driver Characteristics:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
T_{LR}	Rise Time	75	300	ns
T_{LF}	Fall Time	75	300	ns
T_{LRFM}	Differential Rise and Fall Time Matching	80	125	%
C_{LINUA}	Upstream Facing Port (w/cable, low-speed only)	200	450	pF

Clock Timings:

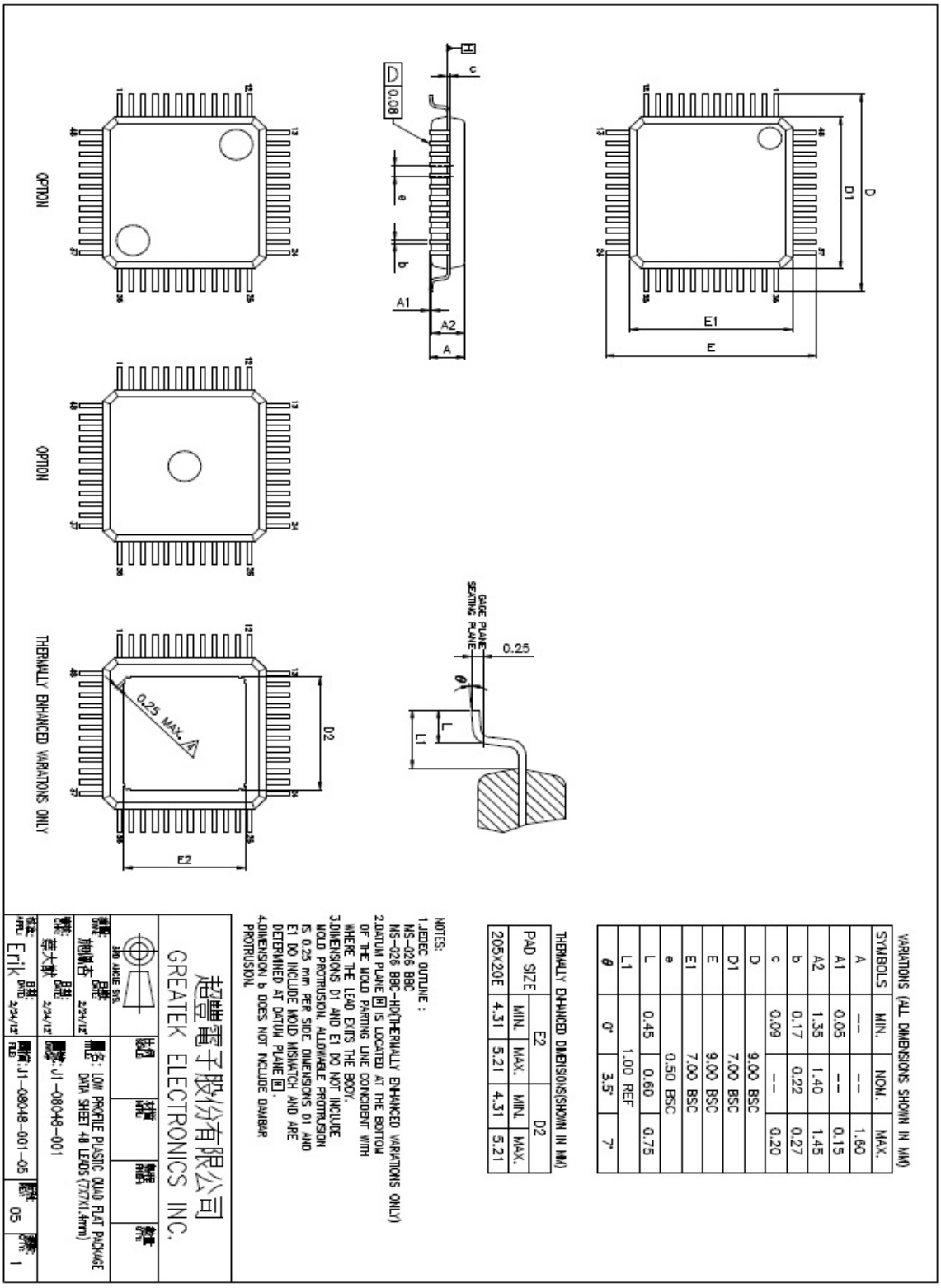
SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
$T_{LDRATHS}$	Low-speed Data Rate for hubs and devices which are high-speed capable	1.49925	1.50075	Mb/s
T_{LDRATE}	Low-speed Data Rate for devices which are not high-speed capable	1.4775	1.5225	Mb/s

Low-speed Data Timings:

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
T_{UDJ1} T_{UDJ2}	Upstream facing port source Jitter Total(including frequency tolerance): To Next Transition For Paired Transitions	-95 -150	95 150	ns ns
T_{LDEOP}	Upstream facing port source Jitter for Differential Transition to SE0 Transition	-40	100	ns
T_{DJR1} T_{DJR2}	Upstream facing port differential Receiver Jitter: To Next Transition For Paired Transitions	-75 -45	75 45	ns ns
T_{DDJ1} T_{DDJ2}	Upstream facing port differential Receiver Jitter: To Next Transition For Paired Transitions	-25 -14	25 14	ns ns
T_{UJR1} T_{UJR2}	Downstream facing port Differential Receiver Jitter: To Next Transition For Paired Transitions	-152 -200	152 200	ns ns
T_{LEOPT}	Source SE0 interval of EOP	1.25	1.50	μs
T_{LEOPR}	Receiver SE0 interval of EOP	670		ns
T_{LST}	Width of SE0 interval during differential transition		210	ns

6. Mechanical Information

Figure 6.1 Mechanical Information Diagram



7. Abbreviations

In this chapter some of the terms and abbreviations used throughout the technical reference manual are listed as follows.

SIE	Serial Interface Engine
SD	Secure Digital
MMC	Multimedia Card
UTMI	USB Transceiver Macrocell Interface

About Alcor Micro, Corp.

Alcor Micro, Corp. designs, develops and markets highly integrated and advanced peripheral semiconductor, and software driver solutions for the personal computer and consumer electronics markets worldwide. We specialize in USB solutions and focus on emerging technology such as USB and IEEE 1394. The company offers a range of semiconductors including controllers for USB hub, integrated keyboard/USB hub and USB Flash memory card reader…etc. Alcor Micro, Corp. is based in Taipei, Taiwan, with sales offices in Taipei, Japan, Korea and California. Alcor Micro is distinguished by its ability to provide innovative solutions for spec-driven products. Innovations like single chip solutions for traditional multiple chip products and on-board voltage regulators enable the company to provide cost-efficiency solutions for the computer peripheral device OEM customers worldwide.