Ultra-Small Package High-Precision Voltage Detector

■ General Description

The LN61C series is a series of high-precision voltage detectors developed using CMOS process. The detection voltage is fixed internally with an accuracy of ±2.0%. Two output forms, Nch open-drain and CMOS output, are available. Ultra-low current consumption and miniature package lineup can meet demand from the portable device applications.

■ Features

- Ultra-low current consumption 2.0 μA typ. (Vin=1.5V)
- High-precision detection voltage ±2.0 %
- Operating voltage range 0.7 V to 8.0 V
- Detection voltage 1.0V to 6.0 V (0.1 V step)
- Output form Nch open-drain output (Active Low) or CMOS output (Active Low)

■ Applications

- Battery checkers
- Power failure detectors
- Power monitor for portable equipments such as pagers, calculators, electronic notebooks and remote controllers.
- Constant voltage power monitor for cameras, video equipments and communication devices.
- Power monitor for microcomputers and reset for CPUs.

■ Package

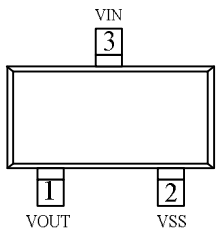
- SOT-23-3L
- SOT-343
- SOT-89-3L
- TO-92

■ Ordering Information

LN61C ①②③④⑤⑥⑦

符号	描述	符号	描述
①	Output Configuration: C=CMOS N=N-ch open drain	⑤	Detect Accuracy: 2=with±2%
②③	Detect Voltage Eg: 10=1.0V 38=3.8V	⑥	Package Type: M=SOT-23-3L
④	Output Delay 0=No delay	⑦	Device Orientation: R=Embossed Taped(Right) L=Embossed Taped(Left)

■ Pin Configurations

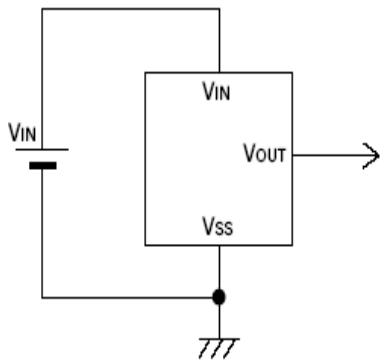


SOT-23-3L
(TOP VIEW)

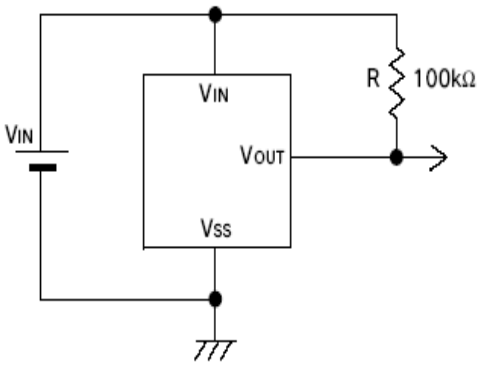
■ Pin Assignment

Pin No. SOT-23-3L	Pin name	Pin description
3	VIN	Voltage input pin
2	VSS	GND pin
1	VOUT	output pin

■ Typical Application Circuit



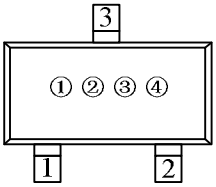
CMOS Output



Nch Open-drain OutputTest circuit

■ Marking Rule

I SOT-23-3L



SOT-23-3L
(TOP VIEW)

① Represents the product name

Symbol	Product Description
C	LN61C◆◆◆◆◆◆◆

② Represents the Output configuration and detect voltage range

Designator	Output Configuration	Voltage Range（V）
A	CMOS	0.1～3.0
B	CMOS	3.1～6.0
N	OPEN DRAIN	0.1～3.0
P	OPEN DRAIN	3.1～6.0

③ Represents the detect voltage

Designatior	Detect Voltage（V）	
0	-	3.1
1	-	3.2
2	-	3.3
3	-	3.4
4	-	3.5
5	-	3.6
6	-	3.7
7	-	3.8
8	0.9	3.9
9	1.0	4
A	1.1	4.1
B	1.2	4.2
C	1.3	4.3
D	1.4	4.4
E	1.5	4.5

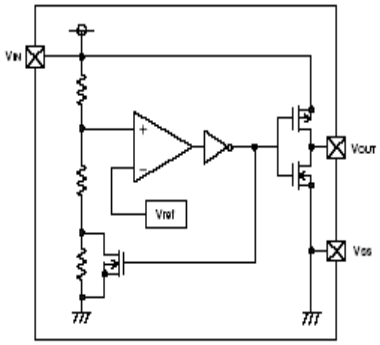
Designatior	Detect Voltage（V）	
F	1.6	4.6
H	1.7	4.7
K	1.8	4.8
L	1.9	4.9
M	2	5
N	2.1	
P	2.2	
R	2.3	
S	2.4	
T	2.5	
U	2.6	
V	2.7	
X	2.8	
Y	2.9	
Z	3	

④ Based on internal standards

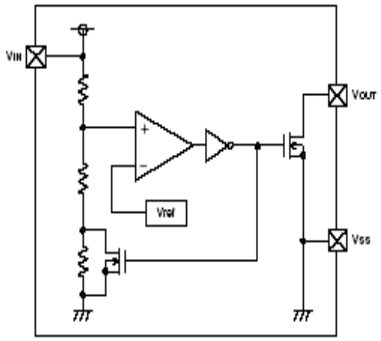
0～9，A～Z repeated G，I，J，O，Q，W are excepted）

■ Function Block Diagram

(1) **CMOS Output Products**



(2) **Nch Open-drain Output Products**



■ Absolute Maximum Ratings (Ta=25°C)

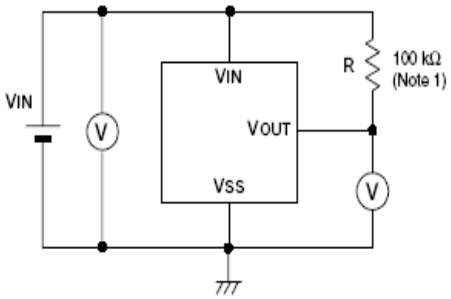
Item		Symbol	Absolute maximum ratings	unit
Power supply voltage		Vin	8	V
Output current		Iout	50	mA
Output voltage	CMOS	Vout	Vss-0.3～Vin+0.3	V
	N-ch		Vss-0.3～8	
Power dissipation	SOT-23-3L	Pd	150	mW
Operating ambient temperature		Topr	-40～+85	°C

■ Electrical Characteristics

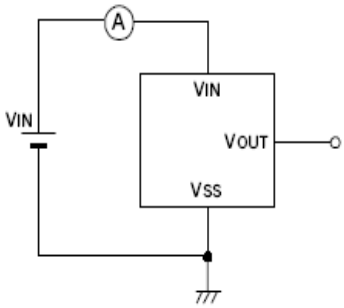
(VDF (T) = 1.0 to 6.0V ±2% Ta=25°C)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Detection voltage	VDF			VDF x0.98	VDF	VDF x1.02	V	1
Release voltage	VHYS				VDF x0.05		V	1
Current consumption	Iss	Vin=1.0V			2.0	2.2	μA	2
		=1.5V			2.0	2.4		
		=2.0V			2.0	2.8		
		=3.0V			2.0	3.1		
		=4.0V			2.0	3.3		
		=5.0V			2.0	3.7		
Operating voltage	Vin	VDF=1.0～6.0V		0.7		8	V	1
Output current	Iout	Nch Vds=0.5V	Vin=1.0V	1.0	2.2		mA	3
			Vin=1.5V	2.0	5.7			
			Vin=2.0V	3.0	7.7			
			Vin=3.0V	5.0	10.1			
			Vin=4.0V	6.0	11.5			
			Vin=5.0V	7.0	13.0			
		Pch vds=2.1 vin=8.0			-10	-2		4
Temperature coefficient		-40～+85°C			±100		ppm/°C	

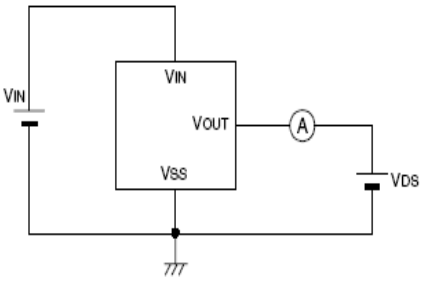
■ Test Circuit



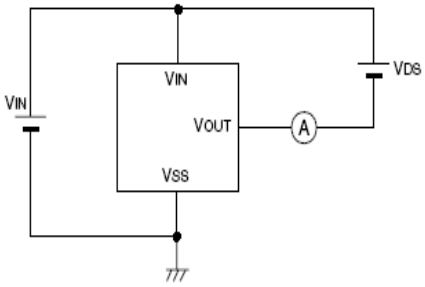
circuit 1



circuit 2

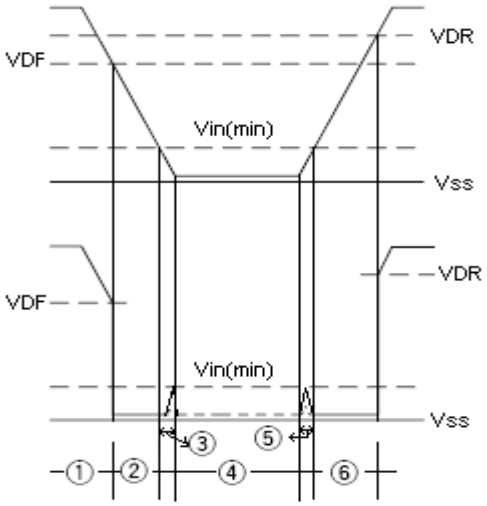


circuit 3

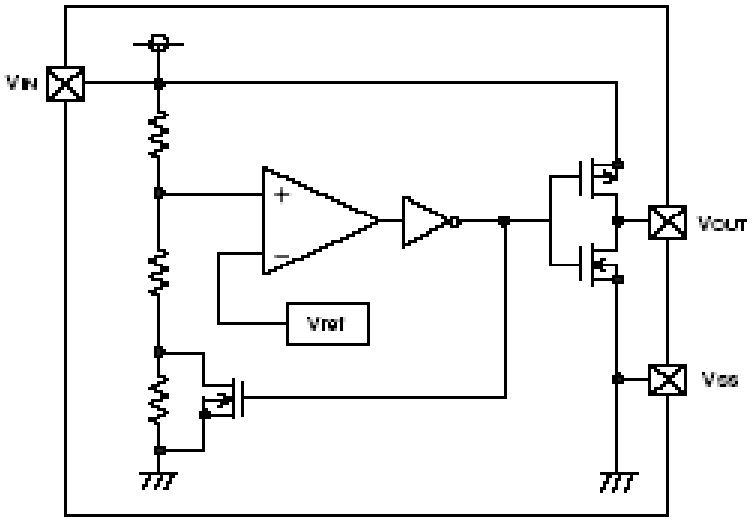


circuit4

■ Timing Chart



■ Operation



1-1. When the power supply voltage (VDD) is higher than the release voltage (VDF), the Nch transistor is OFF and the Pch transistor is ON to provide VDD (high) at the output.

1-2. When the power supply voltage (VDD) is lower than the release voltage (VDF), the Nch transistor is ON and the Pch transistor is OFF to provide VSS (low) at the output.

1-3. When the VDD falls below the minimum operating voltage, the output becomes undefined, or goes to the VDD when the output is pulled up to the VDD.

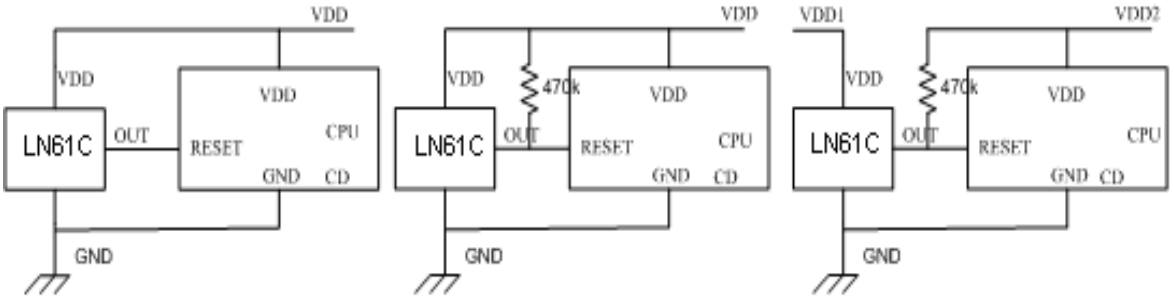
1-4. The VSS level appears when the VDD is VSS level.

1-5. The VSS level appears when the VDD rises above the minimum operating voltage. The VSS level still appears even when the VDD surpasses – VDF, as long as it does not exceed the release voltage + VDF.

1-6. When the VDD rises above + VDF the Nch transistor becomes OFF and the Pch transistor becomes ON to provide VDD level at the output.

■ Application Circuit Examples

l **Microcomputer Reset Circuits**

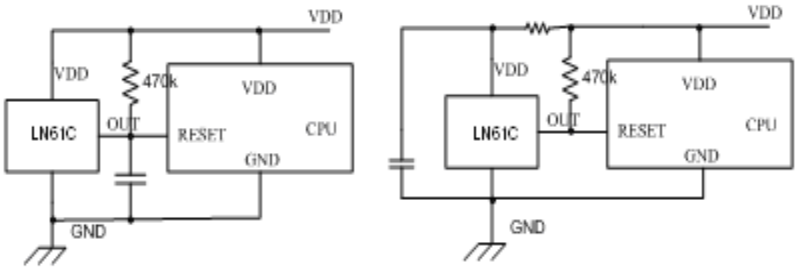


The Same supply voltage with CPU (CMOS output)

The same supply voltage with CPU (Nch Open drain output)

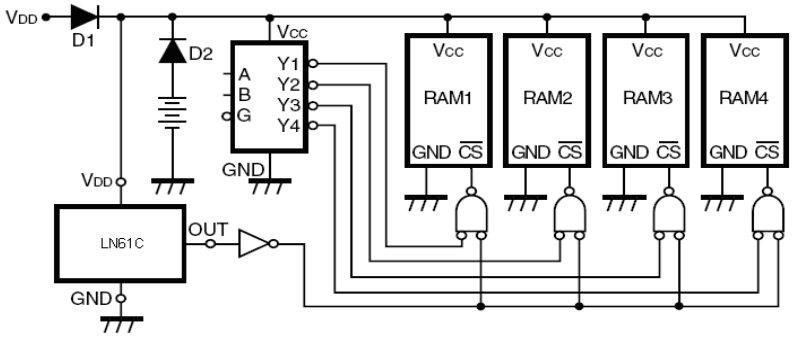
The different supply voltage with CPU (Nch Open drain output)

l Power-on Reset Circuit

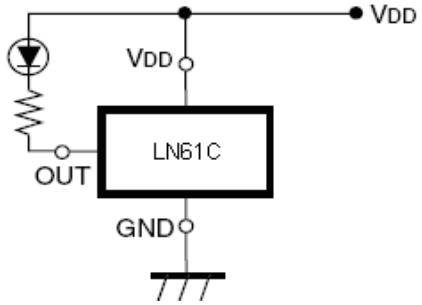


Nch Open drain output　　Nch Open drain output

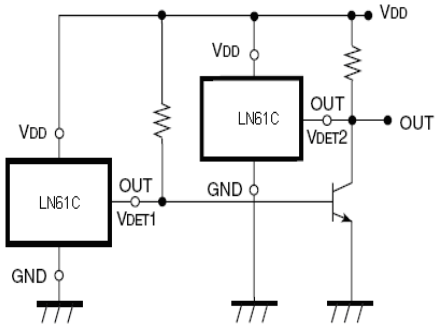
l Mermory back-up circuit



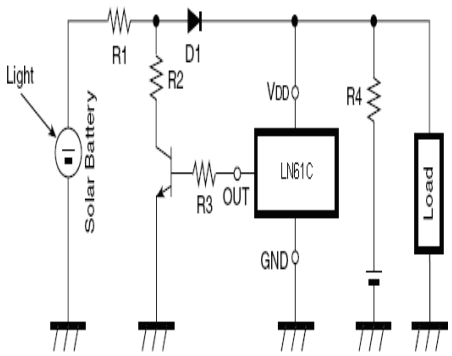
l Power failure detectors



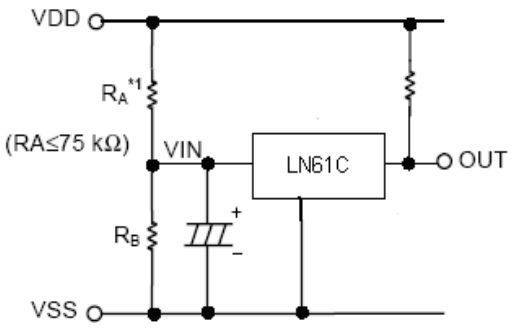
l Window Comparator Circuit



l Overcharge protect circuit

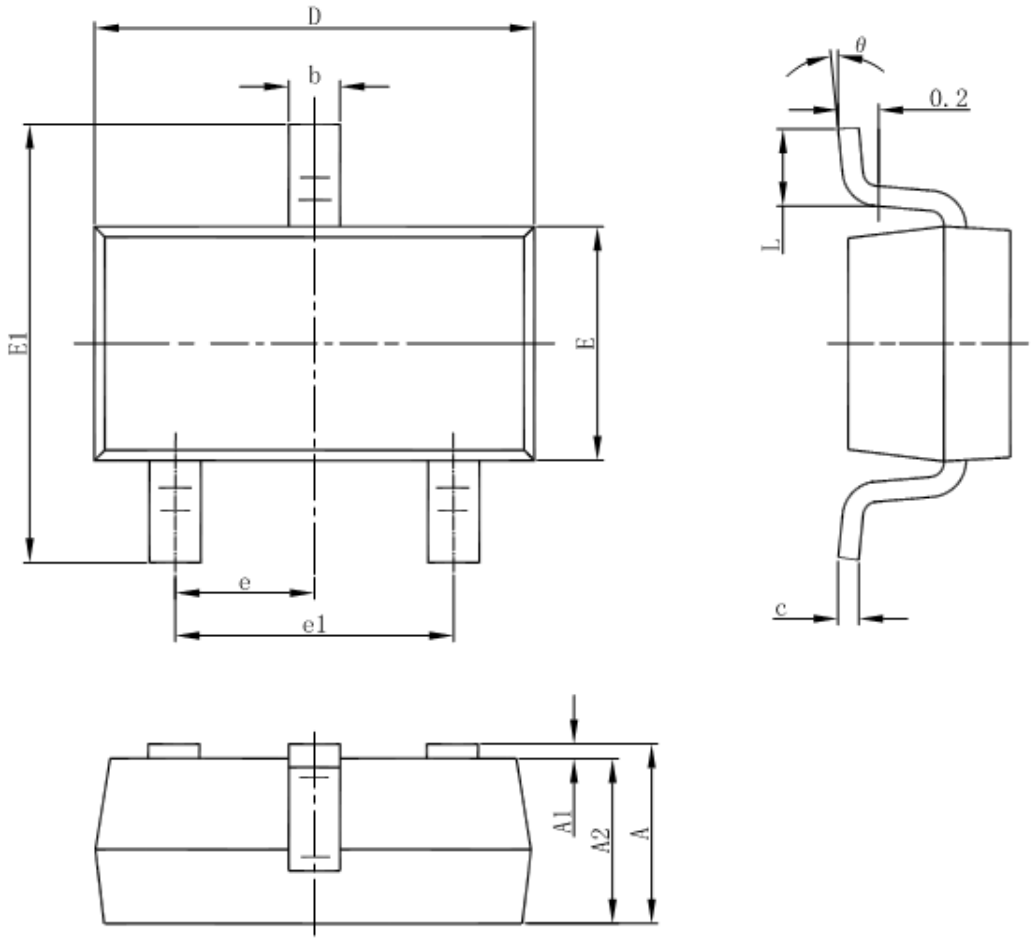


l Detector Adjustable Circuit



■ Package

I SOT-23-3L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°