REVISION HISTORY

Revision	Description	Issue Date
Rev. 1.0	Initial Issue	Aug.28.2005
Rev. 1.1	Revised I_{SB1} LL/LLI-LLE(max)= 50/100 μA => 20/50 μA I_{DR} LL/LLI-LLE(max)= 20/40 μA => 12/30 μA	Mar.30.2006
Rev. 1.2	Added SL Spec.	Nov.2.2007
Rev. 1.3	Revised typos in **FEATURES**	May.6.2008
Rev. 1.4	Revised I_{SB1}/$I_{DR(MAX.)}$ Added I_{SB1}/I_{DR} values when T_A = 25℃ and T_A = 40℃ Revised **FEATURES** & **ORDERING INFORMATION** **Lead free and green package available** to **Green package available** Added packing type in **ORDERING INFORMATION** Revised V_{TERM} to V_{T1} and V_{T2} Deleted T_{SOLDER} in **ABSOLUTE MAXIMUN RATINGS**	Mar.30.2009
Rev. 1.5	Revised **PACKAGE OUTLINE DIMENSION** in page 10/11/12/13	May.7.2010
Rev. 1.6	Revised **ORDERING INFORMATION** in page 14	Aug.30.2010
Rev. 1.7	Deleted E Grade	Aug.9.2011
Rev. 1.8	Revised **PIN CONFIGURATION** in page 2	Apr.06.2012
Rev. 1.9	Correct **ORDERING INFORMATION** Typo. Added top view of BGA in **PIN CONFIGURATION** Deleted E Grade in **ORDERING INFORMATION**	May.20.2016
Rev. 1.10	Deleted **WRITE CYCLE** Notes : 1. WE#, CE# must be high or CE2 must be low during all address transitions in page 7	Jun.28.2016
Rev. 1.11	Revised **GENERAL DESCRIPTION** in page 1 Revised **32-pin TSOP I & 36-ball TFBGA Package Outline Dimension**	Feb.06.2017

LY62W1024

Rev. 1.11

128K X 8 BIT LOW POWER CMOS SRAM

FEATURES

- Fast access time : 35/55/70ns
- Low power consumption:
  Operating current : 12/10/7mA (TYP.)
  Standby current : 1μA (TYP.) LL-version
  0.8μA (TYP.) SL-version
- Single 2.7V ~ 5.5V power supply
- All outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage : 1.5V (MIN.)
- **Green package available**
- Package : 32-pin 450mil SOP
  32-pin 600mil PDIP
  32-pin 8mm x 20mm TSOP I
  32-pin 8mm x 13.4mm sTSOP
  36-ball 6mm x 8mm TFBGA

GENERAL DESCRIPTION

The LY62W1024 is a 1,048,576-bit low power CMOS static random access memory organized as 131,072 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

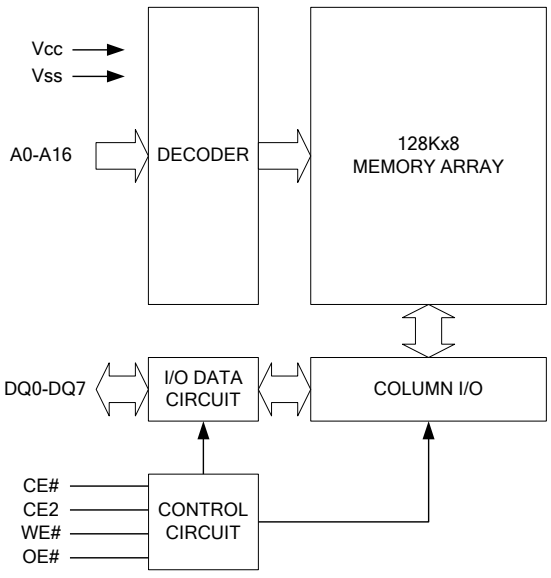
The LY62W1024 is well designed for very low power system applications, and particularly well suited for battery back-up nonvolatile memory application.

The LY62W1024 operates from a single power supply of 2.7V ~ 5.5V and all outputs are fully TTL compatible.

PRODUCT FAMILY

Product Family	Operating Temperature	V_{CC} Range	Speed	Power Dissipation	
				Standby(I_{SB1},TYP.)	Operating(I_{CC},TYP.)
LY62W1024	0 ~ 70℃	2.7 ~ 5.5V	35/55/70ns	1μA(LL)/0.8μA(SL)	12/10/7mA
LY62W1024(I)	-40 ~ 85℃	2.7 ~ 5.5V	35/55/70ns	1μA(LL)/0.8μA(SL)	12/10/7mA

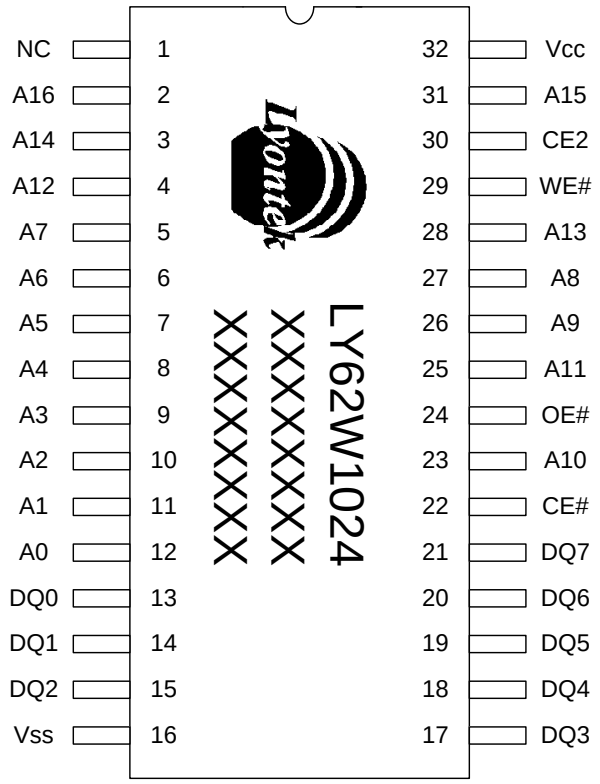
FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

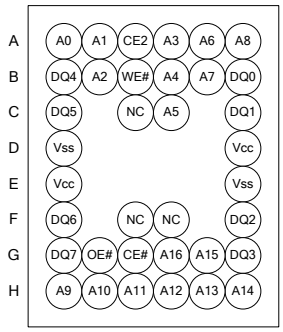
SYMBOL	DESCRIPTION
A0 - A16	Address Inputs
DQ0 - DQ7	Data Inputs/Outputs
CE#, CE2	Chip Enable Inputs
WE#	Write Enable Input
OE#	Output Enable Input
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

PIN CONFIGURATION

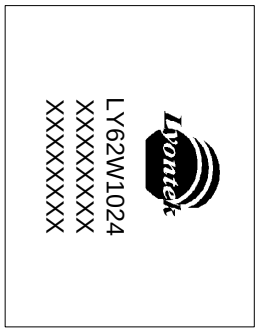


SOP / PDIP

TSOP I / sTSOP



TFBGA(See through with top view)



TFBGA(Top View)

PS: All pin out definition are relative with “Lyontek logo” orientation.

ABSOLUTE MAXIMUN RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V_{CC} relative to V_{SS}	V_{T1}	-0.5 to 6.5	V
Voltage on any other pin relative to V_{SS}	V_{T2}	-0.5 to V_{CC}+0.5	V
Operating Temperature	T_A	0 to 70(C grade)	℃
		-40 to 85(I grade)	
Storage Temperature	T_{STG}	-65 to 150	℃
Power Dissipation	P_D	1	W
DC Output Current	I_{OUT}	50	mA

*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	CE2	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	X	High-Z	I_{SB1}
	X	L	X	X	High-Z	I_{SB1}
Output Disable	L	H	H	H	High-Z	I_{CC},I_{CC1}
Read	L	H	L	H	D_{OUT}	I_{CC},I_{CC1}
Write	L	H	X	L	D_{IN}	I_{CC},I_{CC1}

Note: H = V_{IH}, L = V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP. *4	MAX.	UNIT
Supply Voltage	V_{CC}			2.7	3.0	5.5	V
Input High Voltage	V_{IH} *1			0.7*V_{CC}	-	V_{CC}+0.3	V
Input Low Voltage	V_{IL} *2			- 0.2	-	0.6	V
Input Leakage Current	I_{LI}	$V_{CC} \geqq V_{IN} \geqq V_{SS}$		- 1	-	1	µA
Output Leakage Current	I_{LO}	$V_{CC} \geqq V_{OUT} \geqq V_{SS}$, Output Disabled		- 1	-	1	µA
Output High Voltage	V_{OH}	I_{OH} = -1mA		2.4	2.7	-	V
Output Low Voltage	V_{OL}	I_{OL} = 2mA		-	-	0.4	V
Average Operating Power supply Current	I_{CC}	Cycle time = MIN. CE# = V_{IL} and CE2 = V_{IH}, $I_{I/O}$ = 0mA Other pins at V_{IL} or V_{IH}	- 35	-	12	80	mA
			- 55	-	10	60	mA
			- 70	-	7	50	mA
	I_{CC1}	Cycle time = 1µs CE# = 0.2V and CE2$\geqq$ V_{CC}-0.2V, $I_{I/O}$ = 0mA Other pins at 0.2V or V_{CC} - 0.2V		-	1	10	mA
Standby Power Supply Current	I_{SB1}	CE# $\geqq$ V_{CC}-0.2V or CE2$\leqq$ 0.2V Others at 0.2V or V_{CC} - 0.2V	LL	-	1	15	µA
			LLI	-	1	30	µA
			SL*5 25℃	-	0.8	2	µA
			SLI*5 40℃	-	1	2	µA
			SL	-	0.8	7	µA
			SLI	-	0.8	10	µA

Notes:
1. V_{IH}(max) = V_{CC} + 3.0V for pulse width less than 10ns.
2. V_{IL}(min) = V_{SS} - 3.0V for pulse width less than 10ns.
3. Over/Undershoot specifications are characterized, not 100% tested.
4. Typical values are included for reference only and are not guaranteed or tested.
   Typical values are measured at V_{CC} = $V_{CC(TYP.)}$ and T_A = 25℃
5. This parameter is measured at V_{CC} = 3.0V

CAPACITANCE (T_A = 25℃, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance	C_{IN}	-	6	pF
Input/Output Capacitance	$C_{I/O}$	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to V_{CC} - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C_L = 50pF + 1TTL, I_{OH}/I_{OL} = -1mA/2mA

AC ELECTRICAL CHARACTERISTICS

(1) READ CYCLE

PARAMETER	SYM.	LY62W1024-35		LY62W1024-55		LY62W1024-70		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	35	-	55	-	70	-	ns
Address Access Time	t_{AA}	-	35	-	55	-	70	ns
Chip Enable Access Time	t_{ACE}	-	35	-	55	-	70	ns
Output Enable Access Time	t_{OE}	-	25	-	30	-	35	ns
Chip Enable to Output in Low-Z	t_{CLZ}*	10	-	10	-	10	-	ns
Output Enable to Output in Low-Z	t_{OLZ}*	5	-	5	-	5	-	ns
Chip Disable to Output in High-Z	t_{CHZ}*	-	15	-	20	-	25	ns
Output Disable to Output in High-Z	t_{OHZ}*	-	15	-	20	-	25	ns
Output Hold from Address Change	t_{OH}	10	-	10	-	10	-	ns

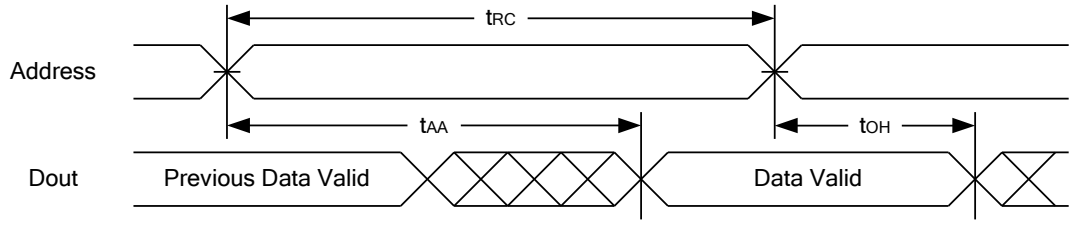
(2) WRITE CYCLE

PARAMETER	SYM.	LY62W1024-35		LY62W1024-55		LY62W1024-70		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	35	-	55	-	70	-	ns
Address Valid to End of Write	t_{AW}	30	-	50	-	60	-	ns
Chip Enable to End of Write	t_{CW}	30	-	50	-	60	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	25	-	45	-	55	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Data to Write Time Overlap	t_{DW}	20	-	25	-	30	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	0	-	0	-	ns
Output Active from End of Write	t_{OW}*	5	-	5	-	5	-	ns
Write to Output in High-Z	t_{WHZ}*	-	15	-	20	-	25	ns

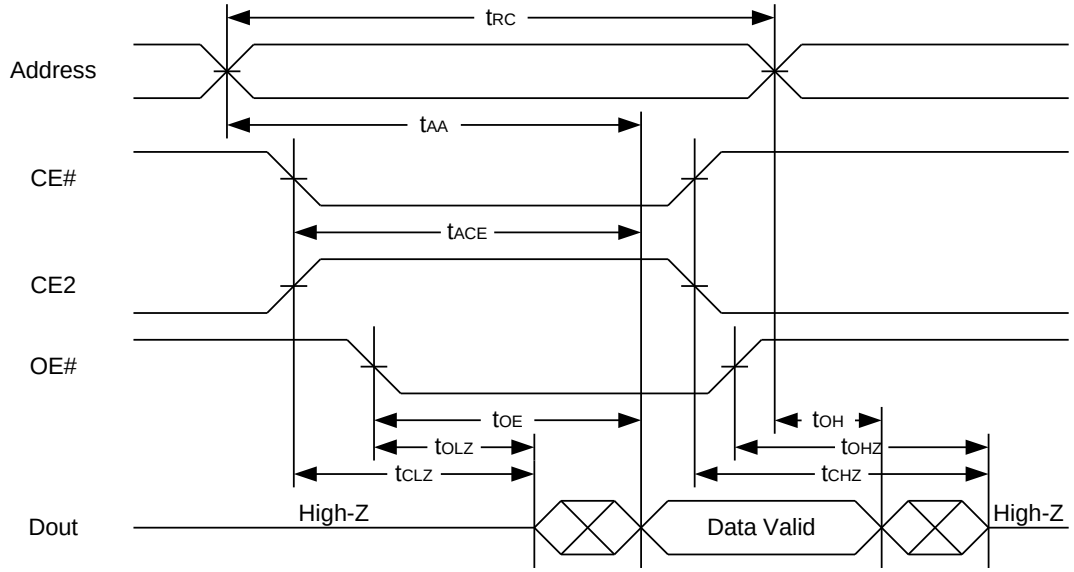
*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)

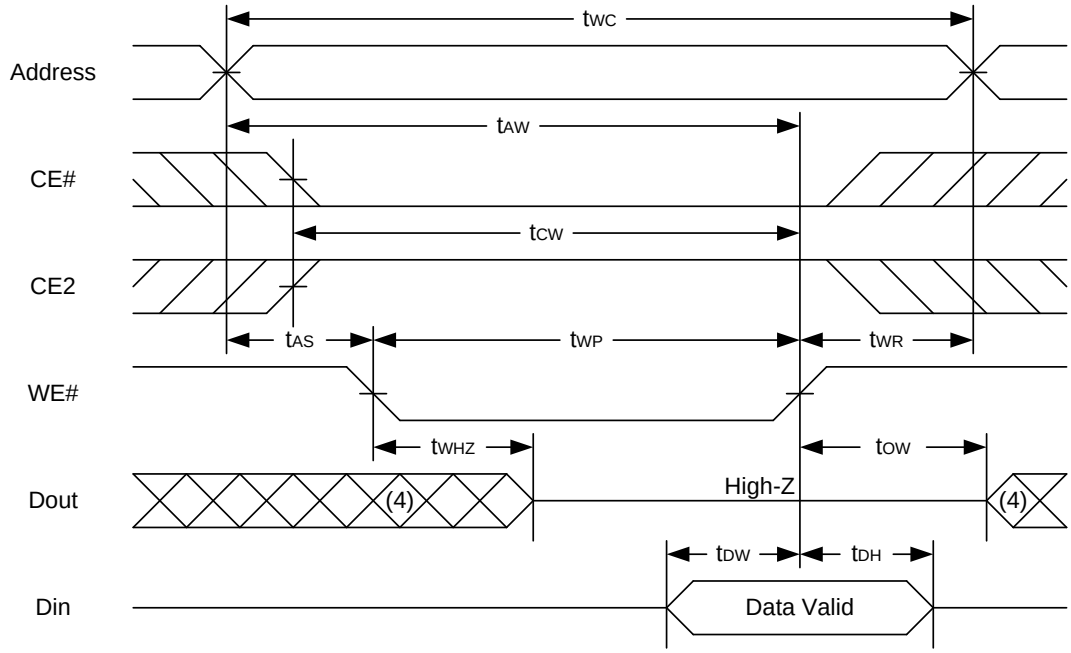


READ CYCLE 2 (CE# and CE2 and OE# Controlled) (1,3,4,5)

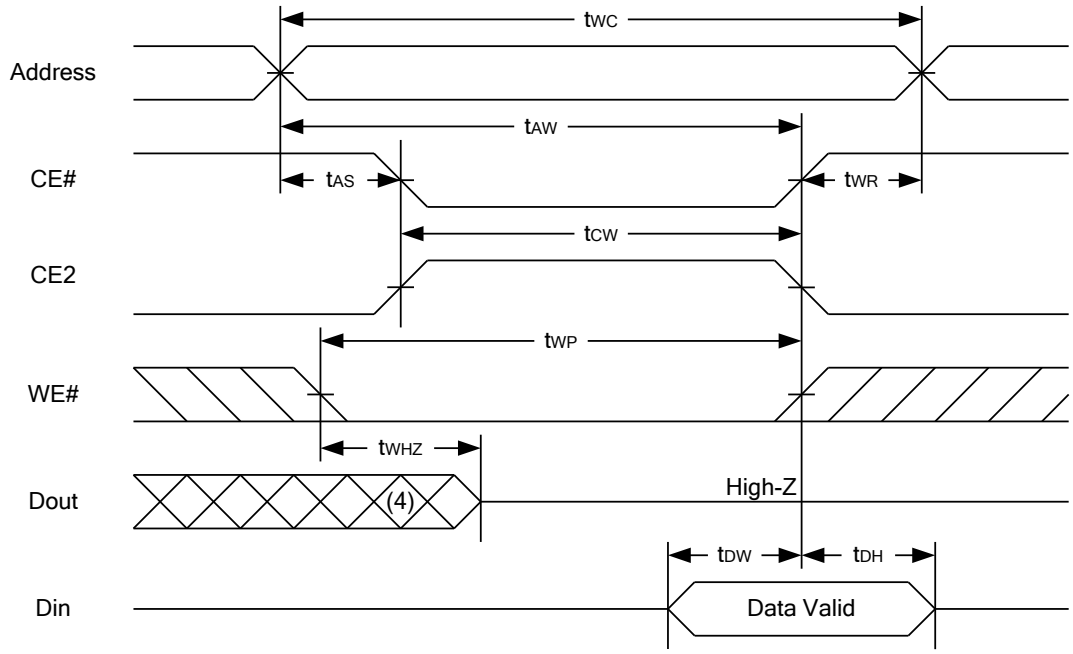


Notes :
1.WE# is high for read cycle.
2.Device is continuously selected OE# = low, CE# = low., CE2 = high.
3.Address must be valid prior to or coincident with CE# = low, CE2 = high; otherwise t_{AA} is the limiting parameter.
4.t_{CLZ}, t_{OLZ}, t_{CHZ} and t_{OHZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.
5.At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{OHZ} is less than t_{OLZ}.

WRITE CYCLE 1 (WE# Controlled) (1,2,4,5)



WRITE CYCLE 2 (CE# and CE2 Controlled) (1,4,5)



Notes :
1.A write occurs during the overlap of a low CE#, high CE2, low WE#.
2.During a WE# controlled write cycle with OE# low, t_{WP} must be greater than $t_{WHZ} + t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
3.During this period, I/O pins are in the output state, and input signals must not be applied.
4.If the CE# low transition and CE2 high transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
5.t_{OW} and t_{WHZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.

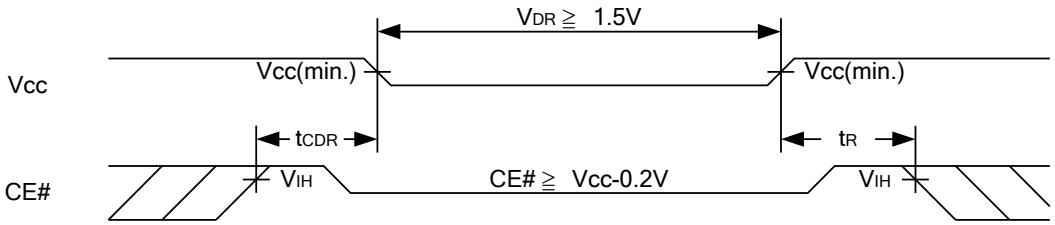
DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
V_{CC} for Data Retention	V_{DR}	CE# ≧ V_{CC} - 0.2V or CE2 ≦ 0.2V			1.5	-	5.5	V
Data Retention Current	I_{DR}	V_{CC} = 1.5V CE# ≧ V_{CC} - 0.2V or CE2 ≦ 0.2V Other pins at 0.2V or V_{CC}-0.2V	LL		-	0.5	12	µA
			LLI		-	0.5	30	µA
			SL	25℃	-	0.4	2	µA
			SLI	40℃	-	0.5	2	µA
			SL		-	0.4	5	µA
			SLI		-	0.4	8	µA
Chip Disable to Data Retention Time	t_{CDR}	See Data Retention Waveforms (below)			0	-	-	ns
Recovery Time	t_R				t_{RC*}	-	-	ns

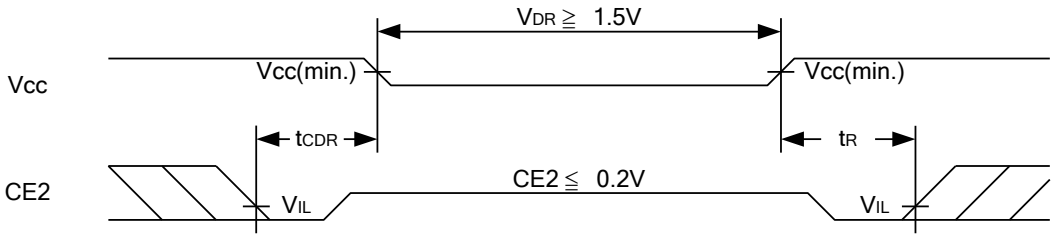
t_{RC*} = Read Cycle Time

DATA RETENTION WAVEFORM

Low V_{CC} Data Retention Waveform (1) (CE# controlled)

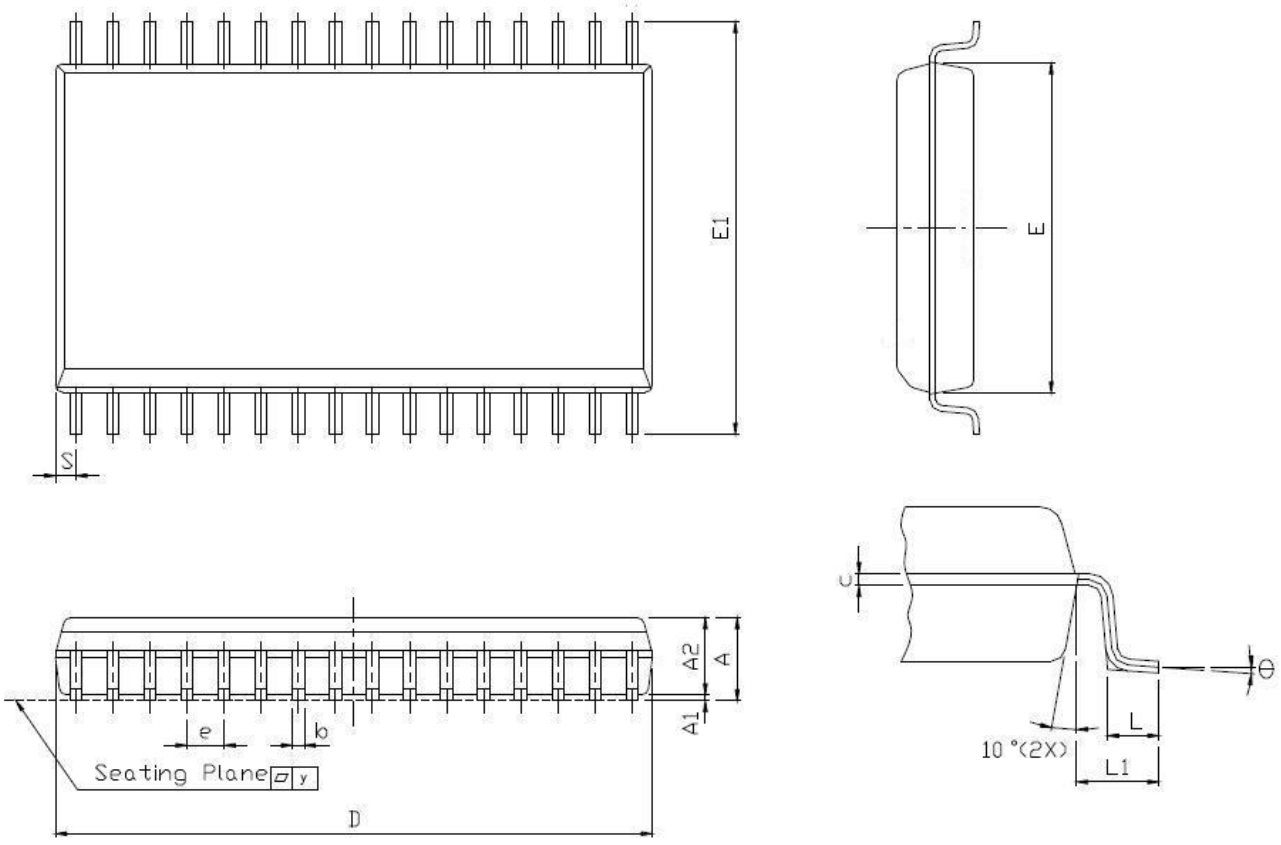


Low V_{CC} Data Retention Waveform (2) (CE2 controlled)



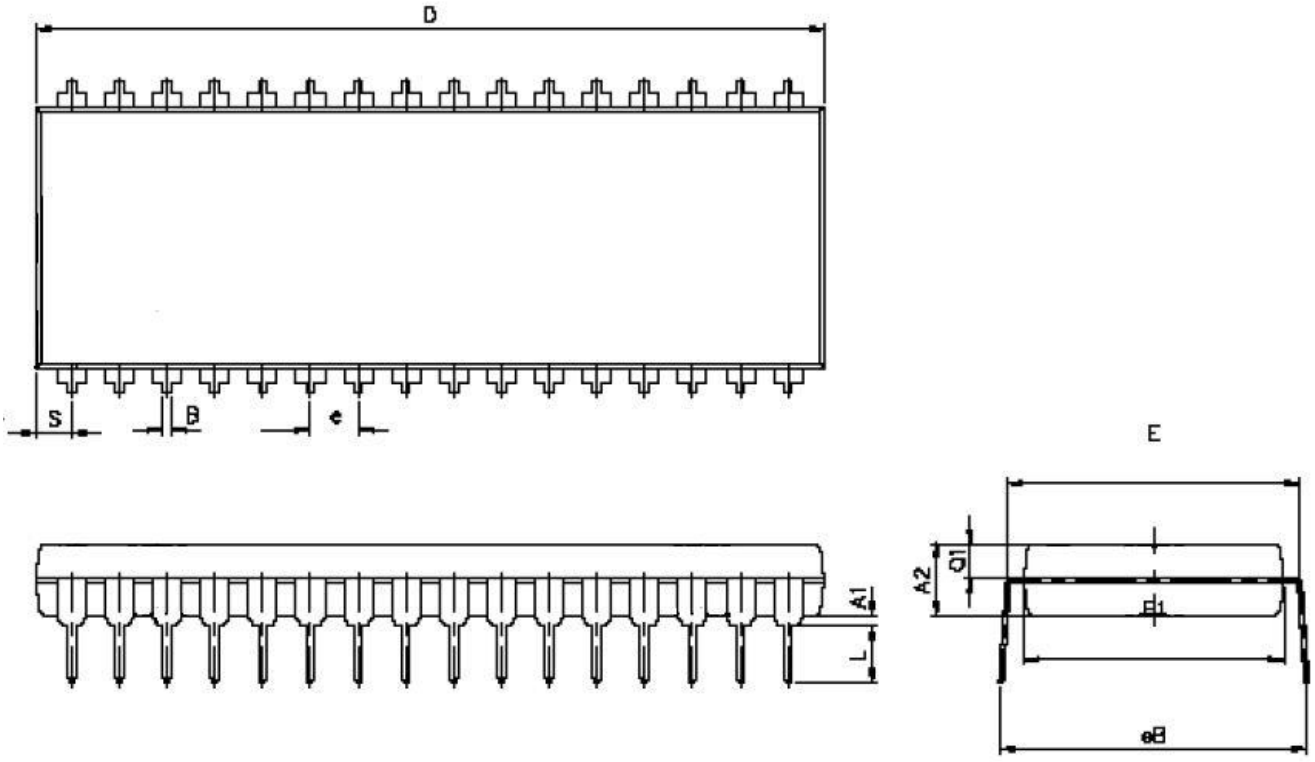
PACKAGE OUTLINE DIMENSION

32-pin 450 mil SOP Package Outline Dimension



UNIT / SYM.	INCH.(BASE)	MM(REF)
A	0.120(MAX)	3.048(MAX)
A1	0.004(MIN)	0.102(MIN)
A2	0.116(MAX)	2.946(MAX)
b	0.016(TYP)	0.406(TYP)
c	0.008(TYP)	0.203(TYP)
D	0.817(MAX)	20.75(MAX)
E	0.445±0.006	11.303±0.152
E1	0.555±0.025	14.097±0.635
e	0.050(TYP)	1.270(TYP)
L	0.033±0.017	0.838±0.432
L1	0.055±0.008	1.397±0.203
S	0.026(MAX)	0.660(MAX)
y	0.004(MAX)	0.101(MAX)
Θ	0° -10°	0° -10°

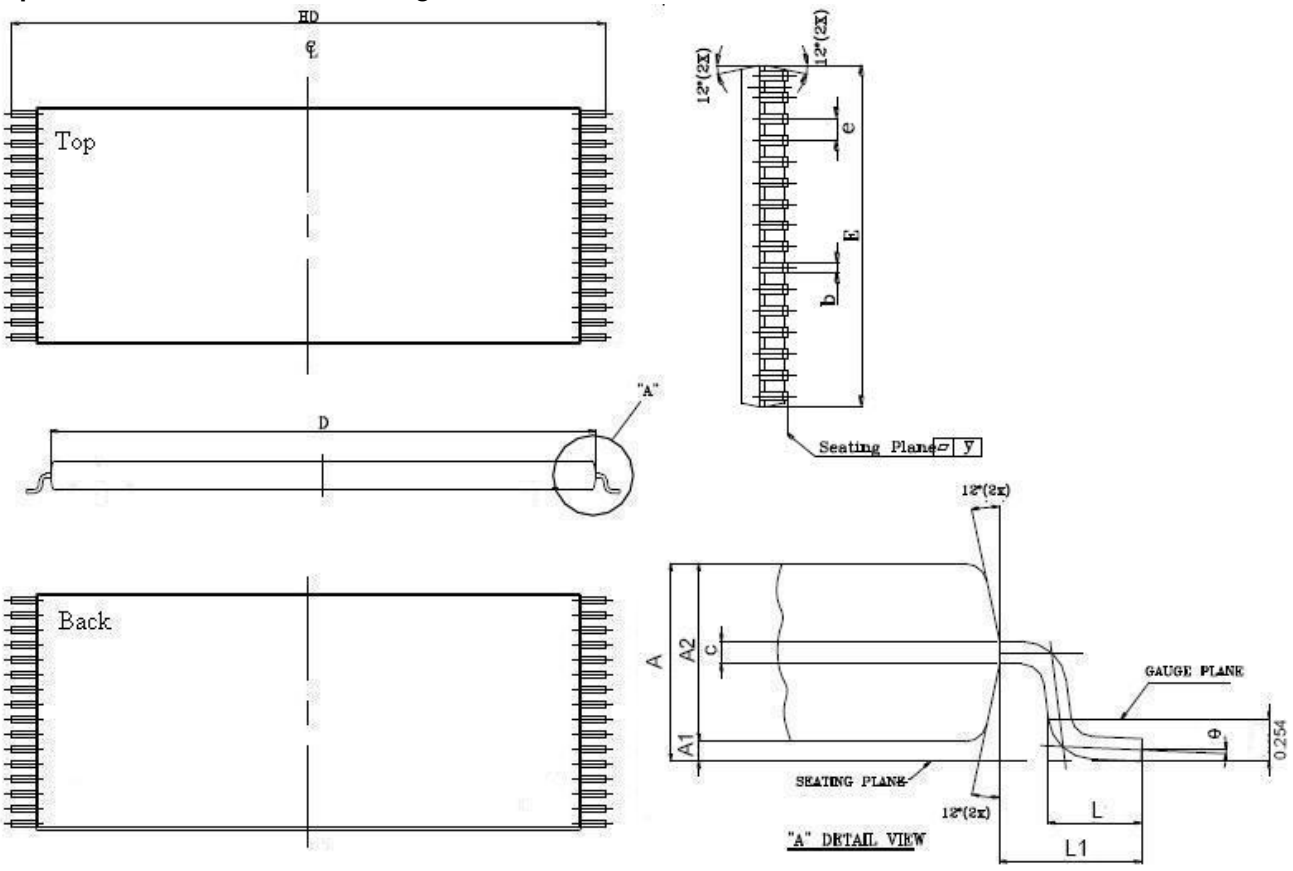
32-pin 600 mil PDIP Package Outline Dimension



UNIT / SYM.	INCH(BASE)	MM(REF)
A1	0.015(MIN)	0.381(MIN)
A2	0.155±0.005	3.937±0.127
B	0.018±0.005	0.457±0.127
D	1.650±0.01	41.910±0.254
E	0.600±0.010	15.240±0.254
E1	0.545±0.005	13.843±0.127
e	0.100(TYP)	2.540(TYP)
eB	0.650±0.020	16.510±0.508.
L	0.158±0.043	4.013±1.092
S	0.075±0.010	1.905±0.254
Q1	0.070±0.005	1.778±0.127

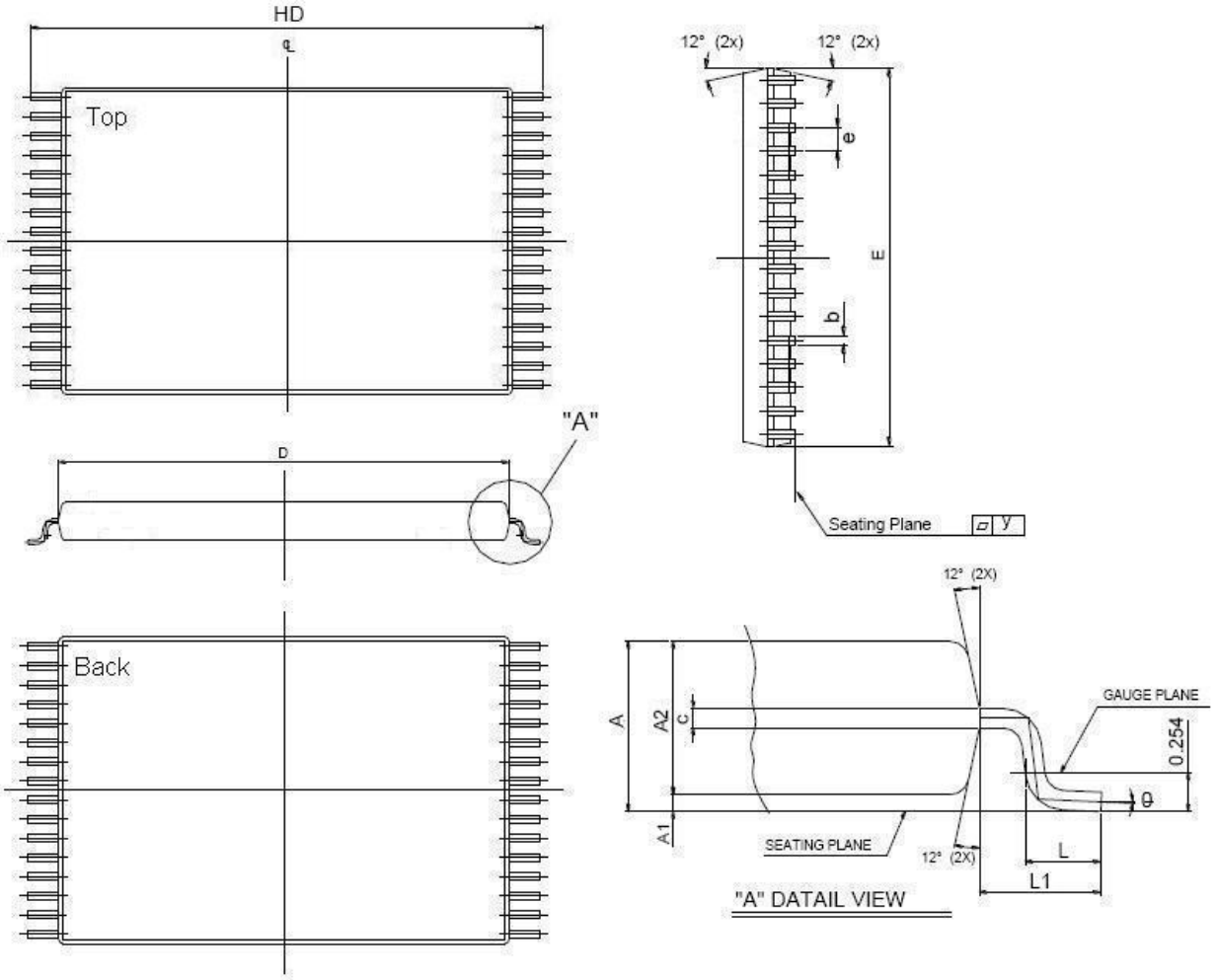
Note : D/E1/S dimension do not include mold flash.

32-pin 8mm x 20mm TSOP I Package Outline Dimension



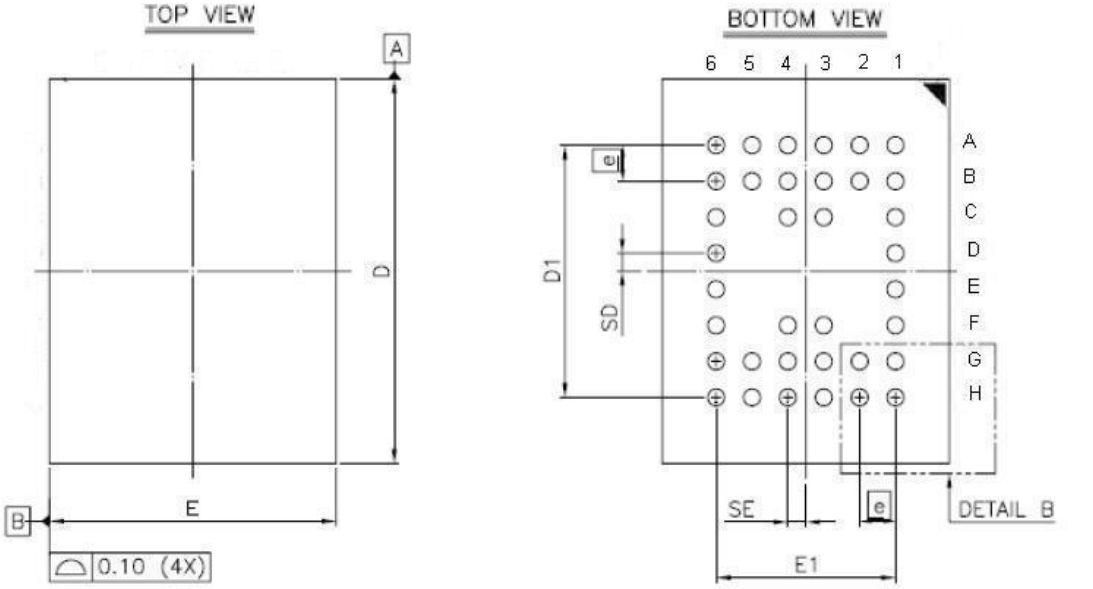
SYM. \ UNIT	INCH(BASE)	MM(REF)
A	0.047 (MAX)	1.20 (MAX)
A1	0.004 ±0.002	0.10 ±0.05
A2	0.039 ±0.002	1.00 ±0.05
b	0.009 ±0.002	0.22 ±0.05
c	0.006 ±0.002	0.155 ±0.055
D	0.724 ±0.008	18.40 ±0.20
E	0.315 ±0.008	8.00 ±0.20
e	0.020 (TYP)	0.50 (TYP)
HD	0.787 ±0.008	20.00 ±0.20
L	0.024 ±0.004	0.60 ±0.10
L1	0.0315 ±0.004	0.08 ±0.10
y	0.003 (MAX)	0.08 (MAX)
Θ	0°～5°	0°～5°

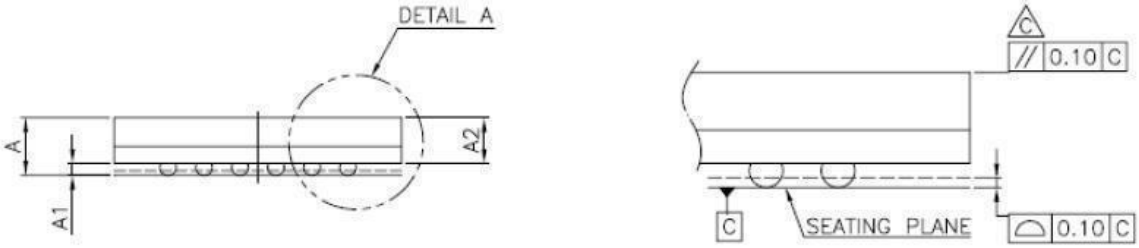
32-pin 8mm x 13.4mm sTSOP Package Outline Dimension



SYM. \ UNIT	INCH(BASE)	MM(REF)
A	0.049 (MAX)	1.25 (MAX)
A1	0.004 ±0.002	0.10 ±0.05
A2	0.039 ±0.002	1.00 ±0.05
b	0.009 ±0.002	0.22 ±0.05
c	0.006 ±0.002	0.155 ±0.055
D	0.465 ±0.008	11.80 ±0.20
E	0.315 ±0.008	8.00 ±0.20
e	0.020 (TYP)	0.50 (TYP)
HD	0.528±0.008	13.40 ±0.20.
L	0.02 ±0.008	0.50 ±0.20
L1	0.031 ±0.005	0.8 ±0.125
y	0.003 (MAX)	0.076 (MAX)
Θ	0°～5°	0°～5°

36-ball 6mm × 8mm TFBGA Package Outline Dimension

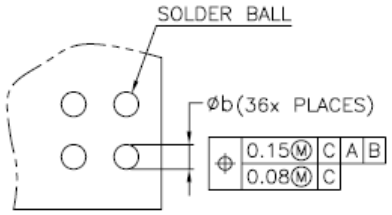




SIDE VIEW

DETAIL A

SYM.	DIMENSION (mm)			DIMENSION (inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.20	0.25	0.30	0.008	0.010	0.012
A2	—	—	0.94	—	—	0.037
b	0.30	0.35	0.40	0.012	0.014	0.016
B D	7.95	8.00	8.05	0.313	0.315	0.317
D1	5.25 BSC			0.207 BSC		
B E	5.95	6.00	6.05	0.234	0.236	0.238
E1	3.75 BSC			0.148 BSC		
SE	0.375 TYP			0.015 TYP		
SD	0.375 TYP			0.015 TYP		
e	0.75 BSC			0.030 BSC		



DETAIL B

NOTE:
1. CONTROLLING DIMENSION : MILLIMETER.
2. REFERENCE DOCUMENT : JEDEC MO-207.

ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(℃)	Packing Type	Lyontek Item No.
32-pin (450mil) SOP	35	Special Ultra Low Power	0℃ ~ 70℃	Tube	LY62W1024SL-35SL
				Tape Reel	LY62W1024SL-35SLT
			-40℃ ~ 85℃	Tube	LY62W1024SL-35SLI
				Tape Reel	LY62W1024SL-35SLIT
		Ultra Low Power	0℃ ~ 70℃	Tube	LY62W1024SL-35LL
				Tape Reel	LY62W1024SL-35LLT
			-40℃ ~ 85℃	Tube	LY62W1024SL-35LLI
				Tape Reel	LY62W1024SL-35LLIT
	55	Special Ultra Low Power	0℃ ~ 70℃	Tube	LY62W1024SL-55SL
				Tape Reel	LY62W1024SL-55SLT
			-40℃ ~ 85℃	Tube	LY62W1024SL-55SLI
				Tape Reel	LY62W1024SL-55SLIT
		Ultra Low Power	0℃ ~ 70℃	Tube	LY62W1024SL-55LL
				Tape Reel	LY62W1024SL-55LLT
			-40℃ ~ 85℃	Tube	LY62W1024SL-55LLI
				Tape Reel	LY62W1024SL-55LLIT
	70	Special Ultra Low Power	0℃ ~ 70℃	Tube	LY62W1024SL-70SL
				Tape Reel	LY62W1024SL-70SLT
			-40℃ ~ 85℃	Tube	LY62W1024SL-70SLI
				Tape Reel	LY62W1024SL-70SLIT
		Ultra Low Power	0℃ ~ 70℃	Tube	LY62W1024SL-70LL
				Tape Reel	LY62W1024SL-70LLT
			-40℃ ~ 85℃	Tube	LY62W1024SL-70LLI
				Tape Reel	LY62W1024SL-70LLIT

ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(℃)	Packing Type	Lyontek Item No.
32-pin (600mil) PDIP	35	Special	0℃ ~ 70℃	Tube	LY62W1024PL-35SL
		Ultra Low Power	-40℃ ~ 85℃	Tube	LY62W1024PL-35SLI
		Ultra Low Power	0℃ ~ 70℃	Tube	LY62W1024PL-35LL
			-40℃ ~ 85℃	Tube	LY62W1024PL-35LLI
	55	Special	0℃ ~ 70℃	Tube	LY62W1024PL-55SL
		Ultra Low Power	-40℃ ~ 85℃	Tube	LY62W1024PL-55SLI
		Ultra Low Power	0℃ ~ 70℃	Tube	LY62W1024PL-55LL
			-40℃ ~ 85℃	Tube	LY62W1024PL-55LLI
	70	Special	0℃ ~ 70℃	Tube	LY62W1024PL-70SL
		Ultra Low Power	-40℃ ~ 85℃	Tube	LY62W1024PL-70SLI
		Ultra Low Power	0℃ ~ 70℃	Tube	LY62W1024PL-70LL
			-40℃ ~ 85℃	Tube	LY62W1024PL-70LLI

ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(℃)	Packing Type	Lyontek Item No.
32-pin (8mm x 20mm) TSOP I	35	Special Ultra Low Power	0℃ ~ 70℃	Tray	LY62W1024LL-35SL
				Tape Reel	LY62W1024LL-35SLT
			-40℃ ~ 85℃	Tray	LY62W1024LL-35SLI
				Tape Reel	LY62W1024LL-35SLIT
		Ultra Low Power	0℃ ~ 70℃	Tray	LY62W1024LL-35LL
				Tape Reel	LY62W1024LL-35LLT
			-40℃ ~ 85℃	Tray	LY62W1024LL-35LLI
				Tape Reel	LY62W1024LL-35LLIT
	55	Special Ultra Low Power	0℃ ~ 70℃	Tray	LY62W1024LL-55SL
				Tape Reel	LY62W1024LL-55SLT
			-40℃ ~ 85℃	Tray	LY62W1024LL-55SLI
				Tape Reel	LY62W1024LL-55SLIT
		Ultra Low Power	0℃ ~ 70℃	Tray	LY62W1024LL-55LL
				Tape Reel	LY62W1024LL-55LLT
			-40℃ ~ 85℃	Tray	LY62W1024LL-55LLI
				Tape Reel	LY62W1024LL-55LLIT
	70	Special Ultra Low Power	0℃ ~ 70℃	Tray	LY62W1024LL-70SL
				Tape Reel	LY62W1024LL-70SLT
			-40℃ ~ 85℃	Tray	LY62W1024LL-70SLI
				Tape Reel	LY62W1024LL-70SLIT
		Ultra Low Power	0℃ ~ 70℃	Tray	LY62W1024LL-70LL
				Tape Reel	LY62W1024LL-70LLT
			-40℃ ~ 85℃	Tray	LY62W1024LL-70LLI
				Tape Reel	LY62W1024LL-70LLIT

ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(℃)	Packing Type	Lyontek Item No.
32-pin (8mm x 13.4mm) sTSOP	35	Special Ultra Low Power	0℃ ~ 70℃	Tray	LY62W1024RL-35SL
				Tape Reel	LY62W1024RL-35SLT
			-40℃ ~ 85℃	Tray	LY62W1024RL-35SLI
				Tape Reel	LY62W1024RL-35SLIT
		Ultra Low Power	0℃ ~ 70℃	Tray	LY62W1024RL-35LL
				Tape Reel	LY62W1024RL-35LLT
			-40℃ ~ 85℃	Tray	LY62W1024RL-35LLI
				Tape Reel	LY62W1024RL-35LLIT
	55	Special Ultra Low Power	0℃ ~ 70℃	Tray	LY62W1024RL-55SL
				Tape Reel	LY62W1024RL-55SLT
			-40℃ ~ 85℃	Tray	LY62W1024RL-55SLI
				Tape Reel	LY62W1024RL-55SLIT
		Ultra Low Power	0℃ ~ 70℃	Tray	LY62W1024RL-55LL
				Tape Reel	LY62W1024RL-55LLT
			-40℃ ~ 85℃	Tray	LY62W1024RL-55LLI
				Tape Reel	LY62W1024RL-55LLIT
	70	Special Ultra Low Power	0℃ ~ 70℃	Tray	LY62W1024RL-70SL
				Tape Reel	LY62W1024RL-70SLT
			-40℃ ~ 85℃	Tray	LY62W1024RL-70SLI
				Tape Reel	LY62W1024RL-70SLIT
		Ultra Low Power	0℃ ~ 70℃	Tray	LY62W1024RL-70LL
				Tape Reel	LY62W1024RL-70LLT
			-40℃ ~ 85℃	Tray	LY62W1024RL-70LLI
				Tape Reel	LY62W1024RL-70LLIT

ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(℃)	Packing Type	Lyontek Item No.
36-ball (6mm x 8mm) TFBGA	35	Special Ultra Low Power	0℃ ~ 70℃	Tray	LY62W1024GL-35SL
				Tape Reel	LY62W1024GL-35SLT
			-40℃ ~ 85℃	Tray	LY62W1024GL-35SLI
				Tape Reel	LY62W1024GL-35SLIT
		Ultra Low Power	0℃ ~ 70℃	Tray	LY62W1024GL-35LL
				Tape Reel	LY62W1024GL-35LLT
			-40℃ ~ 85℃	Tray	LY62W1024GL-35LLI
				Tape Reel	LY62W1024GL-35LLIT
	55	Special Ultra Low Power	0℃ ~ 70℃	Tray	LY62W1024GL-55SL
				Tape Reel	LY62W1024GL-55SLT
			-40℃ ~ 85℃	Tray	LY62W1024GL-55SLI
				Tape Reel	LY62W1024GL-55SLIT
		Ultra Low Power	0℃ ~ 70℃	Tray	LY62W1024GL-55LL
				Tape Reel	LY62W1024GL-55LLT
			-40℃ ~ 85℃	Tray	LY62W1024GL-55LLI
				Tape Reel	LY62W1024GL-55LLIT
	70	Special Ultra Low Power	0℃ ~ 70℃	Tray	LY62W1024GL-70SL
				Tape Reel	LY62W1024GL-70SLT
			-40℃ ~ 85℃	Tray	LY62W1024GL-70SLI
				Tape Reel	LY62W1024GL-70SLIT
		Ultra Low Power	0℃ ~ 70℃	Tray	LY62W1024GL-70LL
				Tape Reel	LY62W1024GL-70LLT
			-40℃ ~ 85℃	Tray	LY62W1024GL-70LLI
				Tape Reel	LY62W1024GL-70LLIT

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