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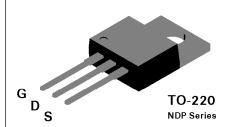
# NDP6020P / NDB6020P P-Channel Logic Level Enhancement Mode Field Effect Transistor

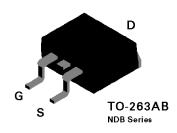
#### **General Description**

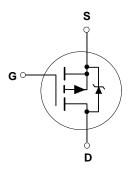
These logic level P-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as automotive, DC/DC converters, PWM motor controls, and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

#### **Features**

- $\begin{array}{ll} \bullet & \text{-24 A, -20 V. } R_{\text{DS(ON)}} = 0.05 \; \Omega \; @ \; V_{\text{GS}} = \text{-4.5 V.} \\ R_{\text{DS(ON)}} = 0.07 \Omega \; @ \; V_{\text{GS}} = \text{-2.7 V.} \\ R_{\text{DS(ON)}} = 0.075 \; \Omega \; @ \; V_{\text{GS}} = \text{-2.5 V.} \end{array}$
- Critical DC electrical parameters specified at elevated temperature.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- 175°C maximum junction temperature rating.
- High density cell design for extremely low R<sub>DS(ON)</sub>.
- TO-220 and TO-263 (D<sup>2</sup>PAK) package for both through hole and surface mount applications.







#### **Absolute Maximum Ratings** T<sub>o</sub> = 25°C unless otherwise noted

Symbol	Parameter	NDP6020P	NDB6020P	Units
V <sub>DSS</sub>	Drain-Source Voltage	-20		V
V <sub>GSS</sub>	Gate-Source Voltage - Continuous	±8		V
I <sub>D</sub>	Drain Current - Continuous	-24		А
	- Pulsed	-70		
P <sub>D</sub>	Total Power Dissipation @ T <sub>C</sub> = 25°C	60		W
	Derate above 25°C	0.4		W/°C
$T_J, T_{STG}$	Operating and Storage Temperature Range	-65 to 17	75	°C

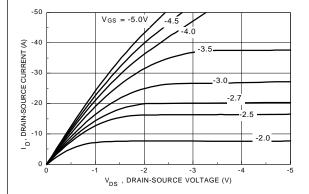
Symbol	Parameter	Conditions		Min	Тур	Max	Units
OFF CH	ARACTERISTICS						-
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_{D} = -250 \mu\text{A}$		-20			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}$				-1	μΑ
			$T_J = 55^{\circ}C$			-10	μΑ
I <sub>GSSF</sub>	Gate - Body Leakage, Forward	$V_{GS} = 8 \text{ V}, V_{DS} = 0 \text{ V}$				100	nA
I <sub>GSSR</sub>	Gate - Body Leakage, Reverse	$V_{GS} = -8 \text{ V}, V_{DS} = 0 \text{ V}$				-100	nA
ON CHA	RACTERISTICS (Note 1)						-
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = -250 \ \mu A$		-0.4	-0.7	-1	V
			T <sub>J</sub> = 125°C	-0.3	-0.56	-0.7	
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	$V_{GS} = -4.5 \text{ V}, I_D = -12 \text{ A}$ $T_J = 125^{\circ}\text{C}$	<del>-</del>		0.041	0.05	Ω
			T <sub>J</sub> = 125°C		0.06	0.08	
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	$V_{GS} = -2.7 \text{ V}, I_{D} = -10 \text{ A}$			0.059	0.07	
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	$V_{GS} = -2.5 \text{ V}, I_{D} = -10 \text{ A}$			0.064	0.075	
I <sub>D(on)</sub>	On-State Drain Current	$V_{GS} = -4.5 \text{ V}, V_{DS} = -5 \text{ V}$		-24			Α
g <sub>FS</sub>	Forward Transconductance	$V_{DS} = -5 \text{ V}, I_{D} = -12 \text{ A}$			14		S
DYNAMI	C CHARACTERISTICS						
C <sub>iss</sub>	Input Capacitance	$V_{DS} = -10 \text{ V}, \ V_{GS} = 0 \text{ V}, $ f = 1.0 MHz			1590		pF
C <sub>oss</sub>	Output Capacitance				725		pF
C <sub>rss</sub>	Reverse Transfer Capacitance				215		pF
	NG CHARACTERISTICS (Note 1)	·					
t <sub>D(on)</sub>	Turn - On Delay Time	$V_{DD} = -20 \text{ V}, I_{D} = -3 \text{ A},$			15	30	nS
t <sub>r</sub>	Turn - On Rise Time	$V_{GS} = -5 \text{ V}, R_{GEN} = 6 \Omega$		27	60	nS	
t <sub>D(off)</sub>	Turn - Off Delay Time				120	250	nS
t <sub>f</sub>	Turn - Off Fall Time				70	150	nS
$\overline{Q_g}$	Total Gate Charge	$V_{DS} = -10 \text{ V},$ $I_{D} = -24 \text{ A}, \ V_{GS} = -5 \text{ V}$			25	35	nC
$\overline{Q_{gs}}$	Gate-Source Charge				5		nC
$\overline{Q_{gd}}$	Gate-Drain Charge				10		nC

Symbol	Parameter	Conditions	Min	Тур	Max	Units
DRAIN-S	OURCE DIODE CHARACTERISTICS		•			
I <sub>s</sub>	Maximum Continuous Drain-Source Diode Forward Current				-24	Α
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current				-80	Α
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = -12 A (Note 1)		-1.1	-1.3	V
t <sub>rr</sub>	Reverse Recovery Time	$V_{GS} = 0 \text{ V}, I_{F} = -24 \text{ A},$ $dI_{F}/dt = 100 \text{ A/}\mu\text{s}$		60		ns
I <sub>rr</sub>	Reverse Recovery Current			-1.7		Α
THERMA	AL CHARACTERISTICS				•	
R <sub>BJC</sub>	Thermal Resistance, Junction-to-Case				2.5	°C/W
R <sub>eJA</sub>	Thermal Resistance, Junction-to-Ambient				62.5	°C/W

Note:

<sup>1.</sup> Pulse Test: Pulse Width  $\leq$  300  $\mu$ s, Duty Cycle  $\leq$  2.0%.

# **Typical Electrical Characteristics**



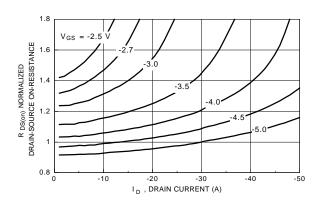


Figure 1. On-Region Characteristics.

Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

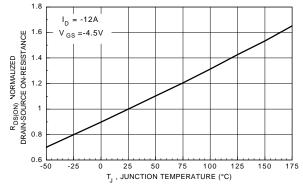


Figure 3. On-Resistance Variation with Temperature.

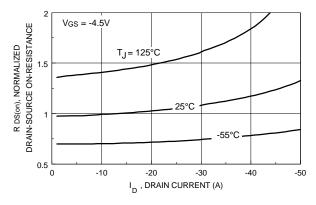


Figure 4. On-Resistance Variation with Drain Current and Temperature.

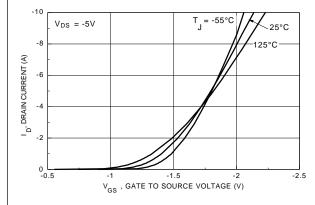


Figure 5. Transfer Characteristics.

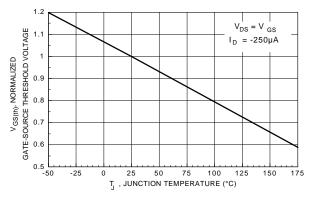


Figure 6. Gate Threshold Variation with Temperature.

# **Typical Electrical Characteristics (continued)**

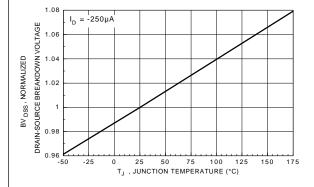


Figure 7. Breakdown Voltage Variation with Temperature.

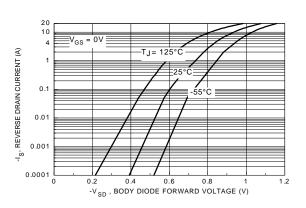


Figure 8. Body Diode Forward Voltage
Variation with Current and Temperature.

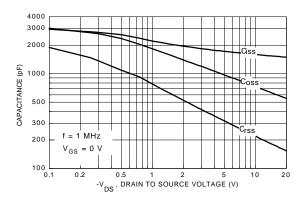


Figure 9. Capacitance Characteristics.

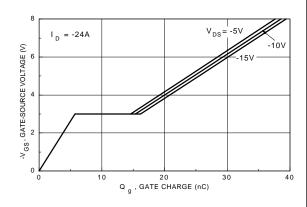


Figure 10. Gate Charge Characteristics.

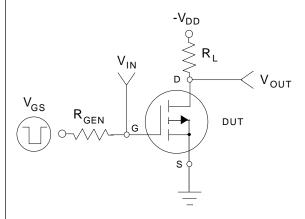


Figure 11. Switching Test Circuit.

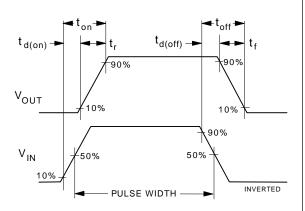
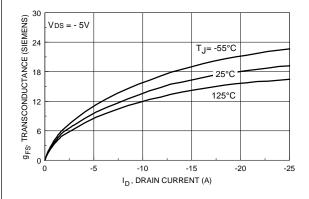


Figure 12. Switching Waveforms.

# **Typical Electrical Characteristics (continued)**



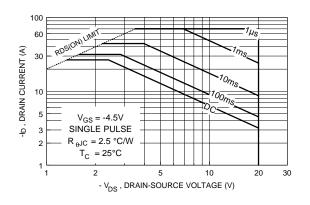


Figure 13. Transconductance Variation with Drain Current and Temperature.

Figure 14. Maximum Safe Operating Area.

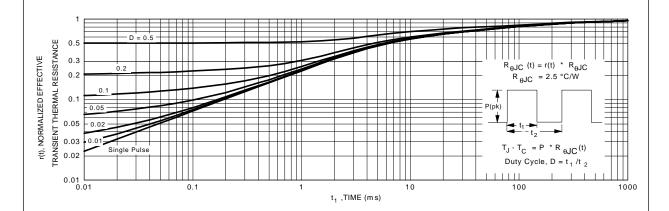


Figure 15. Transient Thermal Response Curve.

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