15V, 75mA High Efficient Buck Converter

Check for Samples: TPS62120 , TPS62122

FEATURES

- **Wide Input Voltage Range 2V to 15V**
- **Up to 96% Efficiency**
- **Power Save Mode with 11 µA Quiescent Current**
- **Output Current 75mA**
- **Output Voltage Range 1.2V to 5.5V**
- **Up to 800kHz Switch Frequency**
- **Synchronous Converter, no External Rectifier**
- **Low Output Ripple Voltage**
- **100% Duty Cycle for Lowest Dropout**
- **Small SOT 8 pin (TPS62120) and 2x2 SON 6 pin (TPS62122) Package**
- **Internal Soft Start**
- **Power Good Open Drain Output TPS62120**
- **Open Drain Output for Output Discharge TPS62120**
- **2.5V Rising / 1.85V Falling UVLO Thresholds**

APPLICATIONS

- **Low Power RF Applications**
- **Ultra Low Power Microprocessor**
- **Energy Harvesting**
- **Industrial Measuring**

DESCRIPTION

The TPS6212X device family is a high efficient synchronous step down DC-DC converter optimized for low power applications. It supports up to 75mA output current and allows the use of tiny external inductors and capacitors.

The wide operating input voltage range of 2V to 15V supports energy harvesting, battery powered and as well 9V or 12V line powered applications.

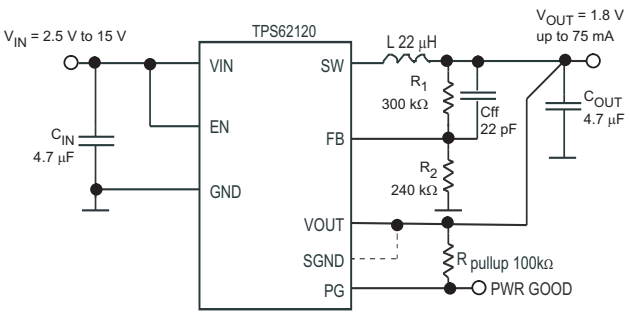
With its advanced hysteretic control scheme the converter provides power save mode operation. At light loads the converter operates in PFM mode (pulse frequency modulation) and transitions automatically in PWM (pulse width modulation) mode at higher load currents. The Power Save Mode maintains high efficiency over the entire load current range. The hysteretic control scheme is optimized for low output ripple voltage in PFM mode in order to reduce output noise to a minimum. It consumes only 10uA quiescent current from VIN in PFM mode operation.

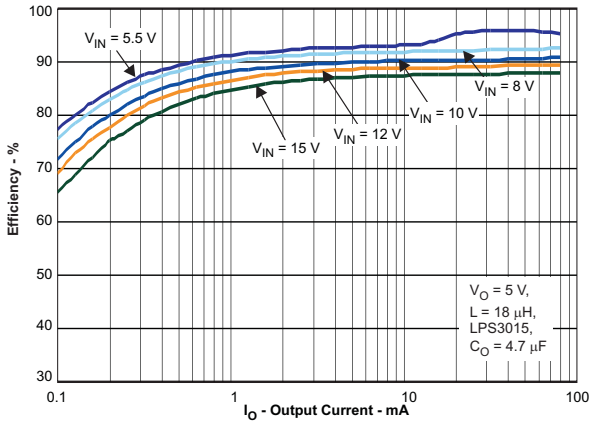
In shutdown mode, the device is turned off.

An open drain power good output is available in the TPS62120 and indicates once the output voltage is in regulation.

TPS62120 has an additional SGND pin which is connected to GND during shutdown mode. This output can be used to discharge the output capacitor.

The TPS62120 is available in a small 3×3 mm^2 8 pin SOT 23 package and the TPS62122 in a 2×2 mm^2 6 pin SON package.





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

TA	PART NUMBER	ACTIVE DISCHARGE SWITCH	POWER GOOD	V_{OUT}	PACKAGE	PACKAGE DESIGNATOR CODE	ORDERING(1)	PACKAGE MARKING
–40°C to 85°C	TPS62120(2)	yes	Open Drain	adjustable	SOT 23-8	DCN	TPS62120DCN	QTX
	TPS62121	yes	yes	2V fixed	SOT 23-8	DCN	samples available	-
	TPS62122(3)	no	no	adjustable	DFN 2x2-6	DRV	TPS62122DRV	OFZ

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com
(2) The DCN package is available in tape on reel. Add R suffix to order quantities of 3000 parts per reel, T suffix for 250 parts per reel.
(3) The DRV package is available in tape on reel. Add R suffix to order quantities of 3000 parts per reel, T suffix for 250 parts per reel.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			VALUE		UNIT
			MIN	MAX	
V_I	Voltage at VIN(2)		–0.3	17	V
	Voltage at SW PIN	dynamically during switching t < 10µs		17	V
		static DC	–0.3	6	
	Voltage at EN PIN(2)		–0.3	VIN +0.3, but ≤17	V
	Voltage on FB Pin		–0.3	3.6	V
	Voltage at PG , VOUT, SGND (2)		–0.3	6	V
I_{IN}	Current into PG pin			0.5	mA
ESD rating(3)	HBM Human body model			2	kV
	CDM Charge device model			1	
	Machine model			100	V
Maximum operating junction temperature, T_J			–40	125	°C
Storage temperature range, T_{stg}			–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal GND.
(3) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin. The machine model is a 200-pF capacitor discharged directly into each pin.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS62120 DCN 8 PINS	TPS62122 DRV 6 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	259.7	114.4	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	114.1	73.7	
θ_{JB}	Junction-to-board thermal resistance	185.8	201.9	
ψ_{JT}	Junction-to-top characterization parameter	21.6	0.8	
ψ_{JB}	Junction-to-board characterization parameter	121.6	94.9	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	n/a	122.7	

(1) For more information about traditional and new thermal metrics, see the *IC PackageThermal Metrics* application report, SPRA953

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage VIN, device in operation		2		15	V
Output current capability	V_{IN} = 2 V, V_{OUT} = 1.8 V, DCR_L = 0.7 Ω	25			mA
	V_{IN} ≥ 2.5 V, V_{OUT} = 1.8 V, DCR_L = 0.7 Ω	75			
Effective inductance		10	22	33	µH
Effective output capacitance		1.0	2	33	µF
Output voltage range		1.2		5.5	V
Operating ambient temperature T_A (1), (Unless Otherwise Noted)		–40		85	°C
Operating junction temperature range, T_J		–40		125	°C

(1) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A(max)}$) is dependent on the maximum operating junction temperature ($T_{J(max)}$), the maximum power dissipation of the device in the application ($P_{D(max)}$), and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A(max)} = T_{J(max)} - (\theta_{JA} \times P_{D(max)})$.

ELECTRICAL CHARACTERISTICS

V_{IN} = 8V, V_{OUT} = 1.8V, EN = V_{IN}, T_J = –40°C to 85°C, typical values are at T_J = 25°C (unless otherwise noted), C_{IN} = 4.7µF, L = 22µH, C_{OUT} = 4.7µF, see Parameter Measurement Information

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Input voltage range (1)	Device operating	2		15	V
I_Q	Quiescent current	I_{OUT} = 0mA, Device not switching, EN = VIN, regulator sleeps		11	18	µA
		I_{OUT} = 0mA, Device switching, V_{IN} = 8 V, V_{OUT} = 1.8V		13		µA
I_{Active}	Active mode current consumption	V_{IN} = 5.5 V = V_{OUT}, T_J = 25°C, high-side MOSFET switch fully turned on		240	275	µA
I_{SD}	Shutdown current	EN = GND, V_{OUT} = SW = 0 V, V_{IN} = 3.6V (2)		0.3	1.2	µA
V_{UVLO}	Undervoltage lockout threshold	Falling V_{IN}		1.85	1.95	V
		Rising V_{IN}		2.5	2.61	V
ENABLE, THRESHOLD						
$V_{IH\ TH}$	Threshold for detecting high EN	2 V ≤ VIN ≤ 15V, rising edge		0.8	1.1	V
$V_{IL\ TH\ HYS}$	Threshold for detecting low EN	2 V ≤ VIN ≤ 15 V, falling edge	0.4	0.6		V
I_{IN}	Input bias current, EN	EN = GND or V_{IN}		0	50	nA
POWER SWITCH						
$R_{DS(ON)}$	high-side MOSFET on-resistance	V_{IN} = 3.6 V		2.3	3.4	Ω
		V_{IN} = 8V		1.75	2.5	
	low-side MOSFET on-resistance	V_{IN} = 3.6 V		1.3	2.5	
		V_{IN} = 8V		1.2	1.75	
I_{LIMF}	Forward current limit MOSFET high-side	V_{IN} = 8V, Open loop	200	250	400	mA
T_{SD}	Thermal shutdown	Increasing junction temperature		150		°C
	Thermal shutdown hysteresis	Decreasing junction temperature		20		°C

(1) The typical required supply voltage for startup is 2.5V. The part is functional down to the falling UVLO (Under Voltage Lockout) threshold
(2) Shutdown current into VIN pin, includes internal leakage

ELECTRICAL CHARACTERISTICS (continued)

V_{IN} = 8V, V_{OUT} = 1.8V, EN = V_{IN}, T_J = –40°C to 85°C, typical values are at T_J = 25°C (unless otherwise noted), C_{IN} = 4.7µF, L = 22µH, C_{OUT} = 4.7µF, see Parameter Measurement Information

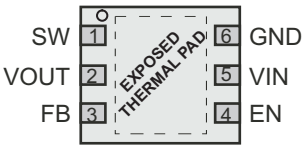
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REGULATOR						
t_{ONmin}	Minimum ON time	V_{IN} = 3.6 V, V_{OUT} = 1.8 V		700		ns
t_{OFFmin}	Minimum OFF time	V_{IN} = 3.6 V, V_{OUT} = 1.8 V		60		ns
V_{REF}	Internal reference voltage			0.8		V
V_{FB}	Feedback FB voltage comparator threshold	Referred to 0.8V internal reference	–2.5%	0%	2.5%	
	Feedback FB voltage line regulation	I_{OUT} = 50 mA, (3)		0.04		%/V
I_{IN}	Input bias current FB	V_{FB} = 0.8 V		0	50	nA
t_{Start}	Regulator start-up time	Time from active EN to device starts switching, VIN = 2.6V		50	150	µs
t_{Ramp}	Output voltage ramp time	Time to ramp up V_{OUT} = 1.8V, no load (4)		120	300	
I_{LK_SW}	Leakage current into SW pin	V_{OUT} = V_{IN} = V_{SW} = 1.8 V, EN = GND, device in shutdown mode		1	1.5	µA
POWER GOOD OUTPUT (TPS62120)						
V_{THPG}	Power Good threshold voltage	Rising V_{FB} feedback voltage	93%	95%	97%	
		Falling V_{FB} feedback voltage	87%	90%	93%	
V_{OL}	Output low voltage	Current into PG pin I = 500 µA, V_{OUT} > 1.5 V			165	mV
		Current into PG pin I = 100 µA, 1.2 V < V_{OUT} <1.5 V			50	
V_H	Output high voltage	Open drain output, external pull up resistor			5.5	V
I_{LKG}	Leakage current into PG pin	$V_{(PG)}$ = 1.8V, EN = high, FB = 0.85 V		0	50	nA
	Leakage into VOUT pin	$V_{(OUT)}$ = 1.8 V		0	50	nA
T_{PGDL}	Internal power good comparator delay time	V_{OUT} = 1.8 V		2	5	µs
SGND OPEN DRAIN OUTPUT (TPS62120)						
R_{DSON}	NMOS drain source resistance	SGND = 1.8 V, V_{IN} = 2 V		370		Ω
I_{LKG}	Leakage current into SGND pin	EN = VIN, SGND = 1.8 V		0	50	nA

(3) V_{OUT} +1V ≤ V_{IN} ; V_{OUT} ≤ 5.5V
(4) Maximum value not production tested

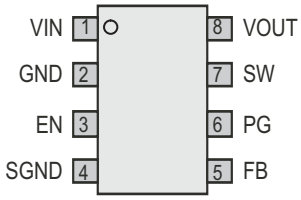
DEVICE INFORMATION

PIN ASSIGNMENTS

2x2SON 6 pin out
DRV PACKAGE
(TOP VIEW)



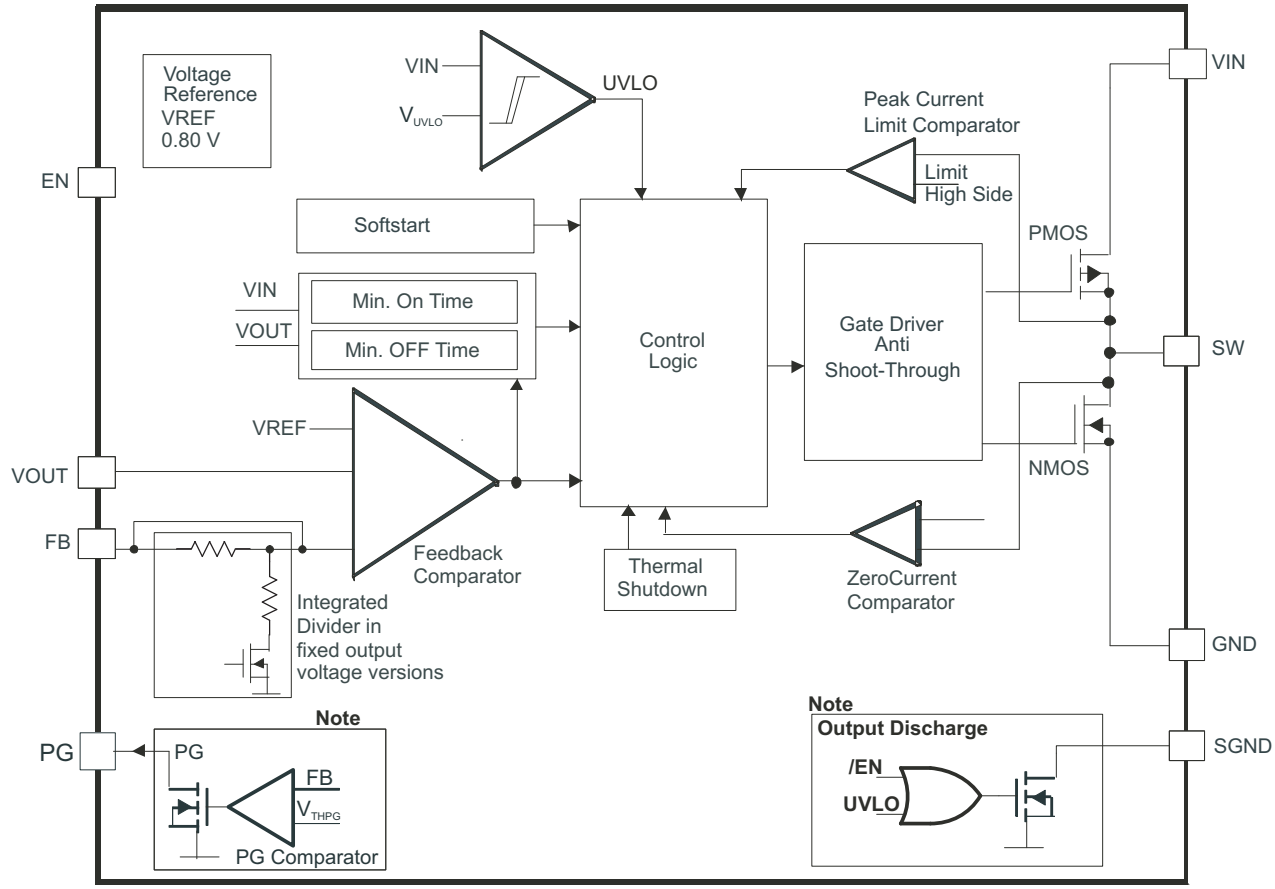
SOT-23 8 pin out
DCN PACKAGE
(TOP VIEW)



PIN FUNCTIONS

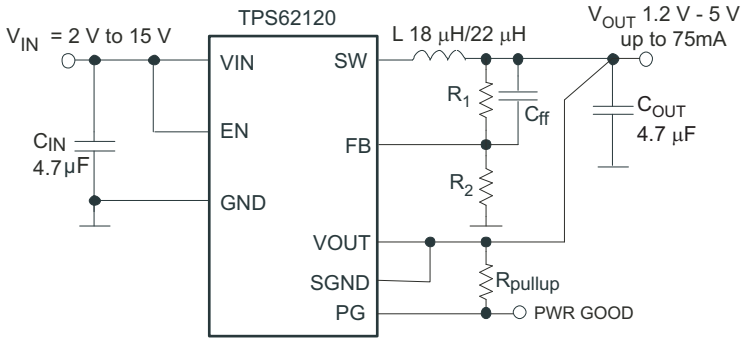
PIN			I/O	DESCRIPTION
NAME	DRV NO.	DCN NO.		
VIN	5	1	PWR	V_{IN} power supply pin.
GND	6	2	PWR	GND supply pin.
EN	4	3	IN	Pulling this pin to high activates the device. Low level shuts it down. This pin must be terminated.
SW	1	7	OUT	This is the switch pin and is connected to the internal MOSFET switches. Connect the inductor to this terminal. Do not tie this pin to VIN, VOUT or GND.
FB	3	5	IN	This is the feedback pin for the regulator. Connect external resistor divider to this pin.
SGND	–	4	IN	This pin is available in TPS62120 only. Open drain output which is turned on during shutdown mode (EN = 0) or VIN is below the UVLO threshold. It connects the SGND pin to GND via an internal MOSFET with typical 370Ω $R_{DS(ON)}$. When the device is enabled (EN = 1), this output is high impedance. To discharge the output capacitor during shutdown mode, connect this pin to VOUT (output capacitor) or leave it open.
VOUT	2	8	IN	This pin must be connected to the output capacitor.
PG	–	6	OUT	This pin is available in TPS62120 only. Open drain power good output. Connect this terminal via a pull up resistor to a voltage rail up to 5.5V or leave it open. This pin can sink 500µA.
	Exposed Thermal PAD	-		Exposed Thermal Pad available only in DRV package option. This pad must be connected to GND.

FUNCTIONAL BLOCK DIAGRAM



NOTE: Function available in TPS62120

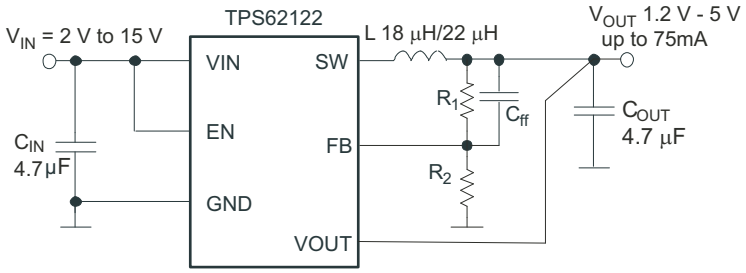
PARAMETER MEASUREMENT INFORMATION



L = 18 µH LPS3015 Coilcraft
22 µH LQH3NPN Murata

C_{IN}: 4.7µF GRM21B series X5R (0805size) 25V Murata
C_{OUT}: 4.7µF GRM188 sereis X5R (0603size) 6.3V Murata

PARAMETER MEASUREMENT INFORMATION (continued)



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TYPICAL CHARACTERISTICS

EFFICIENCY vs OUTPUT CURRENT I_{OUT} (V_{OUT} = 5V)

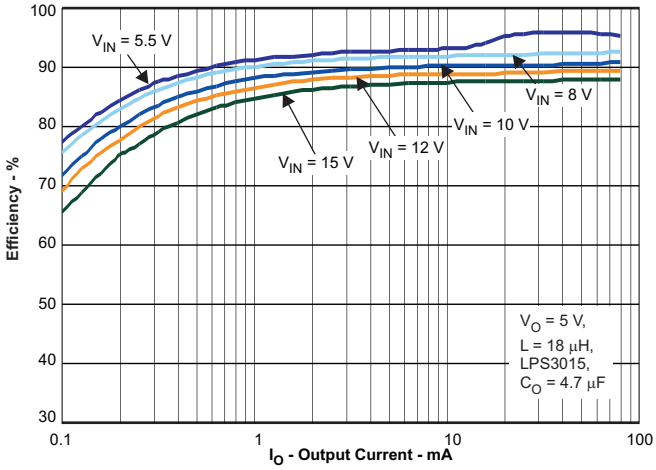


Figure 1.

EFFICIENCY vs INPUT VOLTAGE V_{IN} (V_{OUT} = 5V)

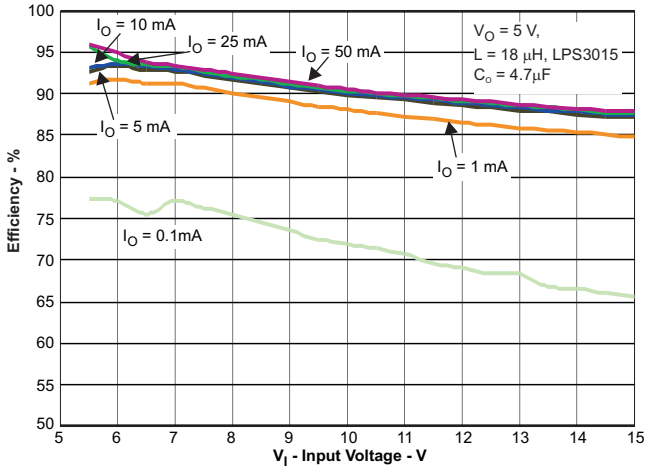


Figure 2.

EFFICIENCY vs OUTPUT CURRENT I_{OUT} (V_{OUT} = 3.3V)

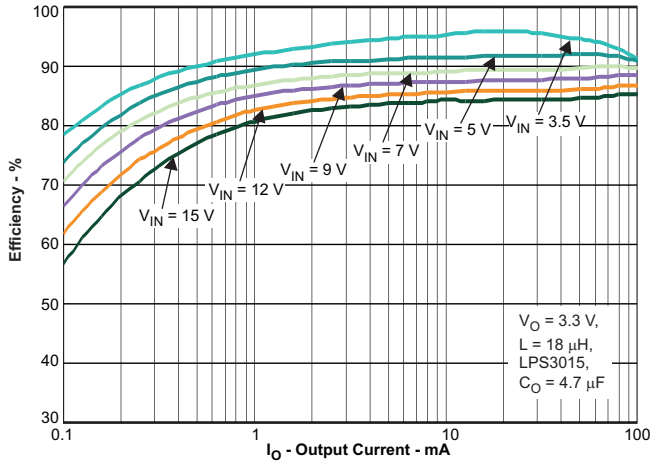


Figure 3.

EFFICIENCY vs INPUT VOLTAGE V_{IN} (V_{OUT} = 3.3V)

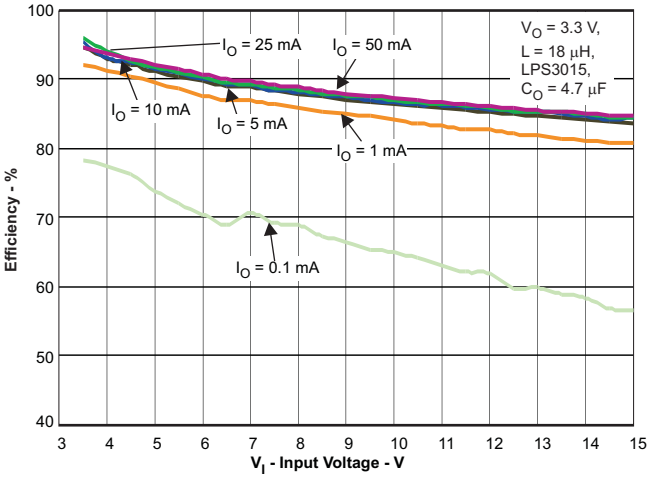


Figure 4.

TYPICAL CHARACTERISTICS (continued)

EFFICIENCY vs OUTPUT CURRENT I_{OUT} (V_{OUT} = 3.0V)

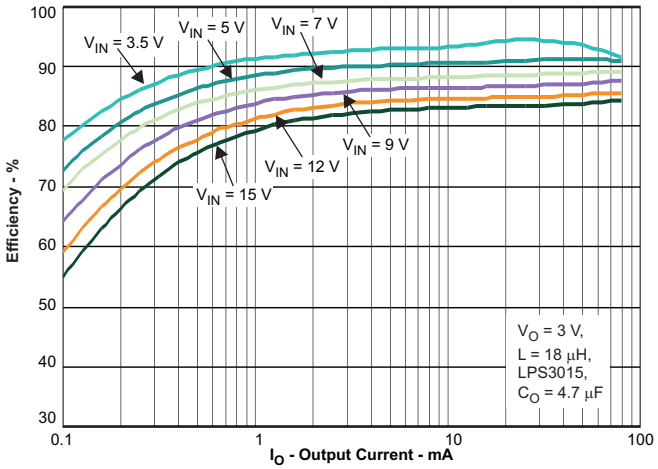


Figure 5.

EFFICIENCY vs INPUT VOLTAGE V_{IN} (V_{OUT} = 3.0V)

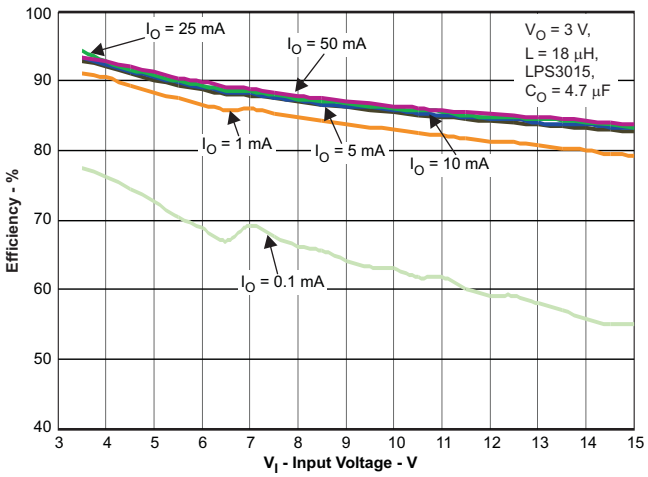


Figure 6.

EFFICIENCY vs OUTPUT CURRENT I_{OUT} (V_{OUT} = 2.0V)

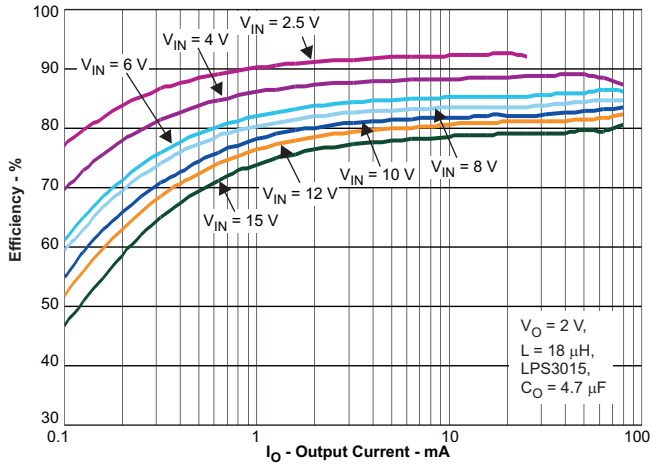


Figure 7.

EFFICIENCY vs INPUT VOLTAGE V_{IN} (V_{OUT} = 2.0V)

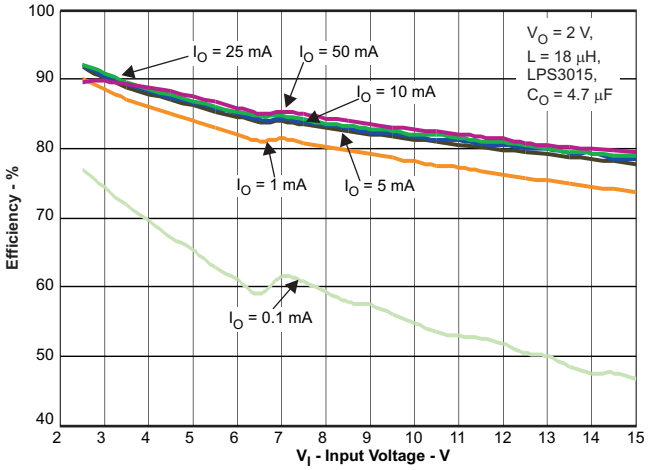


Figure 8.

TYPICAL CHARACTERISTICS (continued)

EFFICIENCY vs OUTPUT CURRENT I_{OUT} (V_{OUT} = 1.2V)

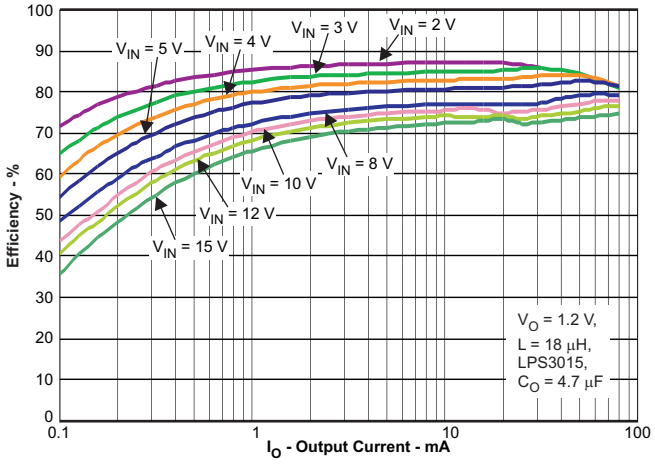


Figure 9.

EFFICIENCY vs INPUT VOLTAGE V_{IN} (V_{OUT} = 1.2V)

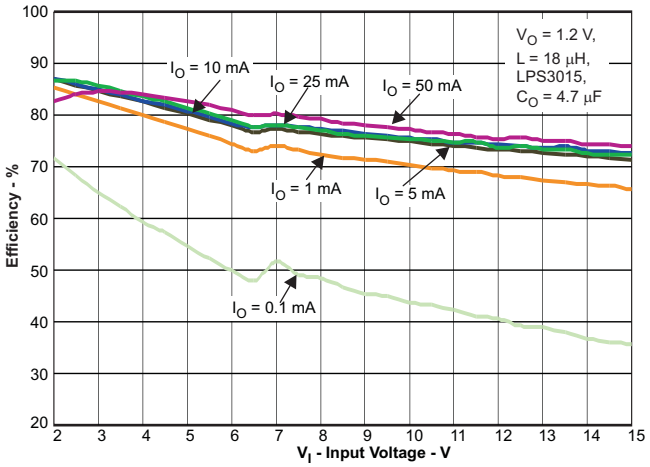


Figure 10.

3.0V OUTPUT VOLTAGE DC REGULATION

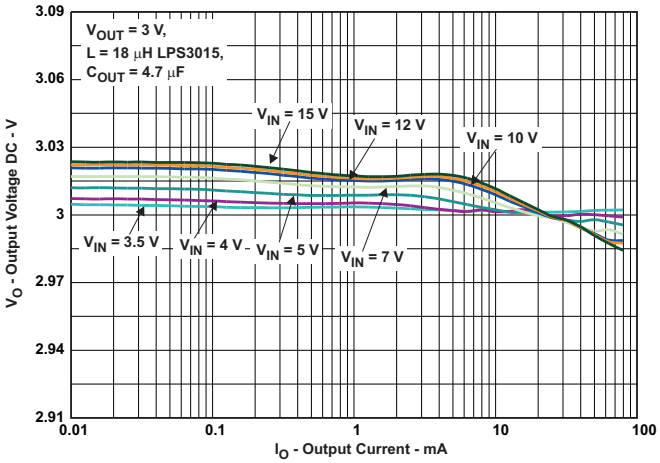


Figure 11.

2.0V OUTPUT VOLTAGE DC REGULATION

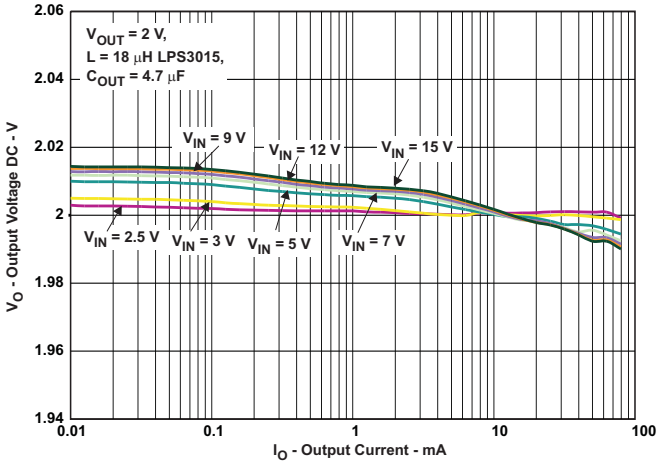


Figure 12.

TYPICAL CHARACTERISTICS (continued)

LOW-SIDE SWITCH RESISTANCE $R_{DS(ON)}$ vs VIN

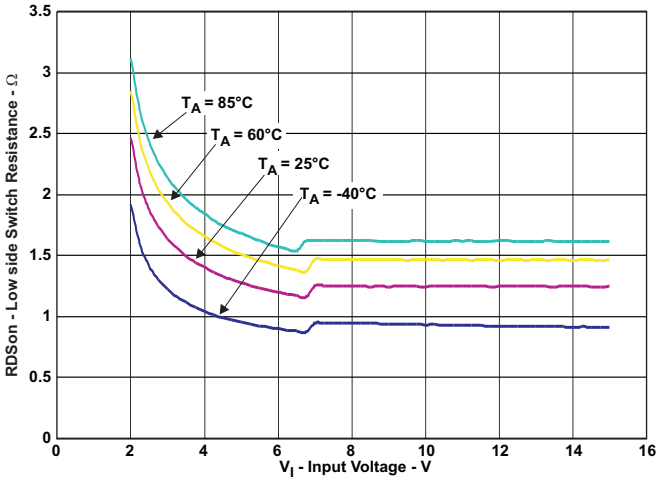


Figure 13.

QUIESCENT CURRENT vs VIN

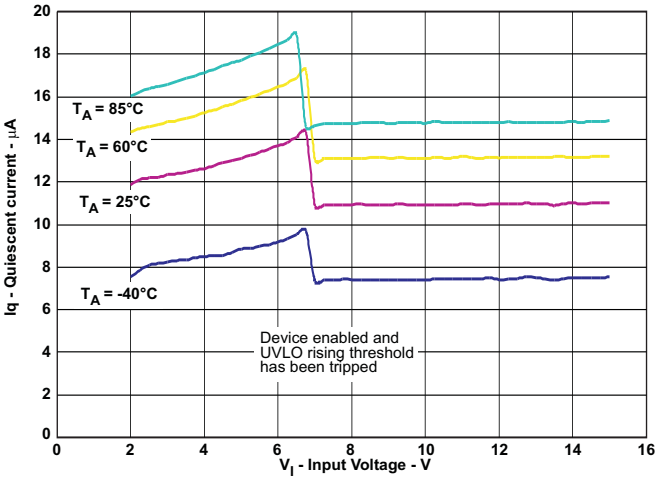


Figure 14.

SHUTDOWN CURRENT vs VIN

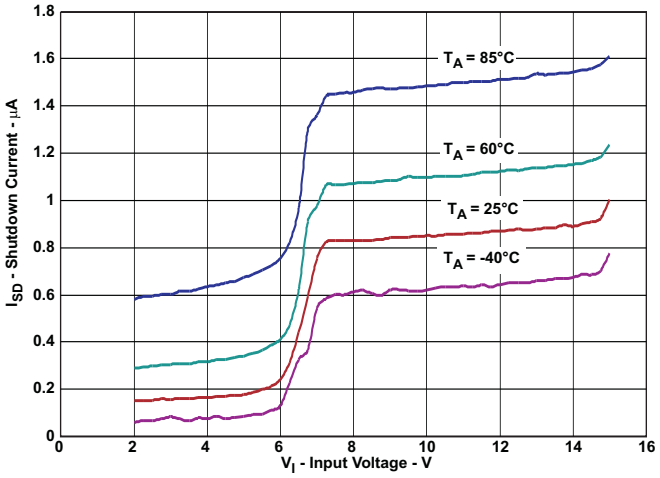


Figure 15.

SWITCH FREQUENCY vs OUTPUT CURRENT I_{OUT} (V_{OUT} = 2.0V)

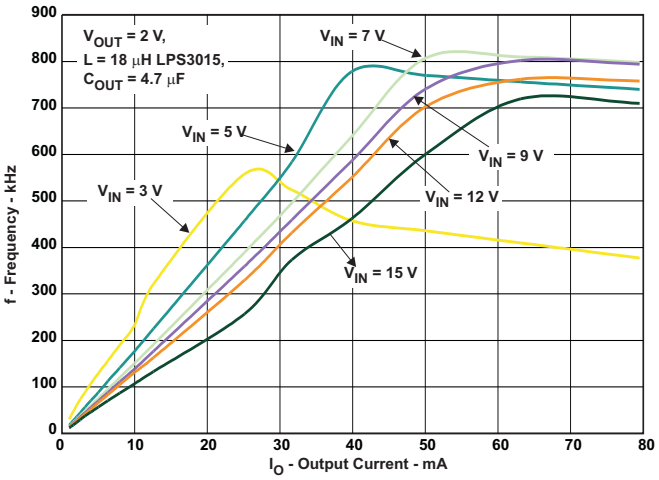


Figure 16.

TYPICAL CHARACTERISTICS (continued)

SWITCH FREQUENCY vs OUTPUT CURRENT I_{OUT} (V_{OUT} = 3.3V)

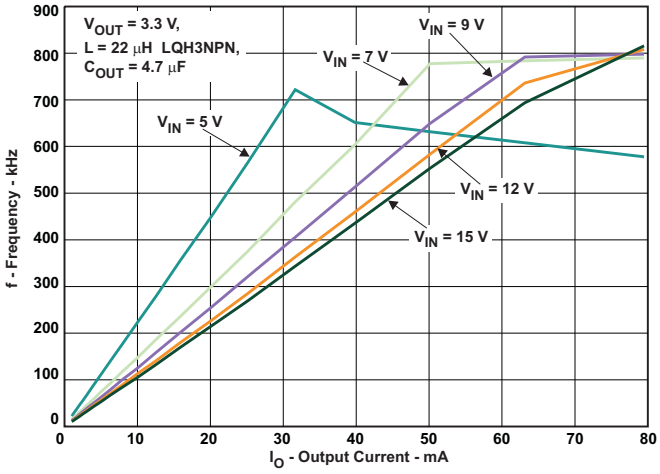


Figure 17.

SWITCH FREQUENCY vs OUTPUT CURRENT I_{OUT} (V_{OUT} = 5.0V)

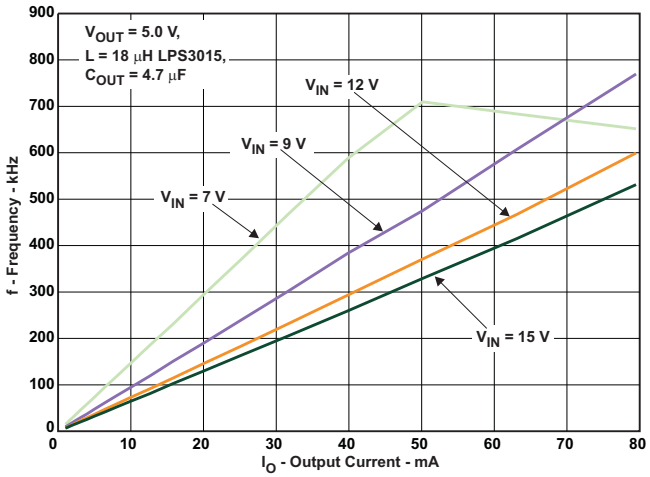


Figure 18.

V_{OUT} 2.0V OUTPUT RIPPLE VOLTAGE PEAK TO PEAK

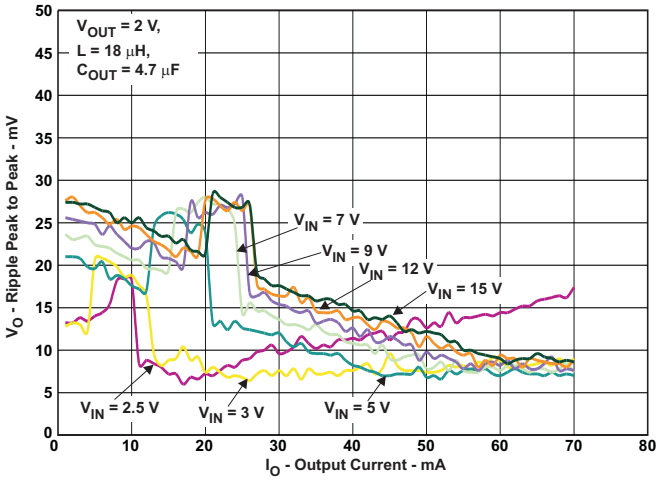


Figure 19.

TYPICAL OPERATION I_{OUT} 60mA

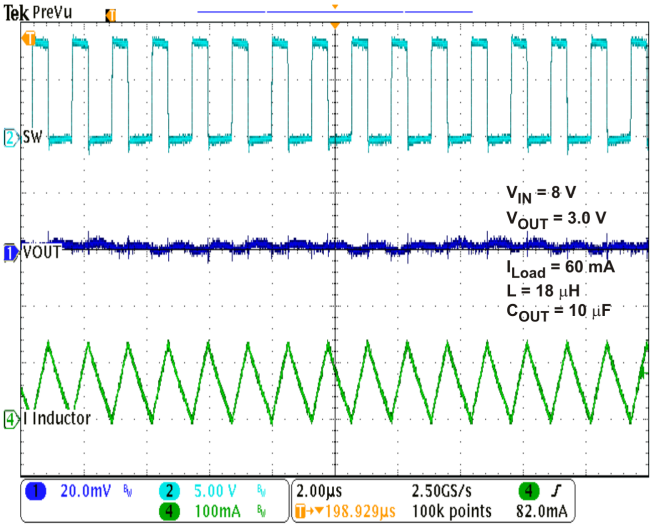


Figure 20.

TYPICAL CHARACTERISTICS (continued)

TYPICAL OPERATION I_{OUT} 10mA

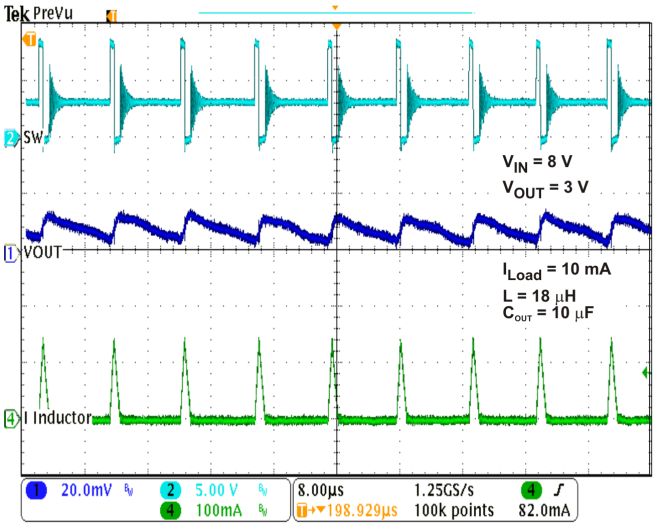


Figure 21.

LINE TRANSIENT RESPONSE FOR 3V OUTPUT VOLTAGE

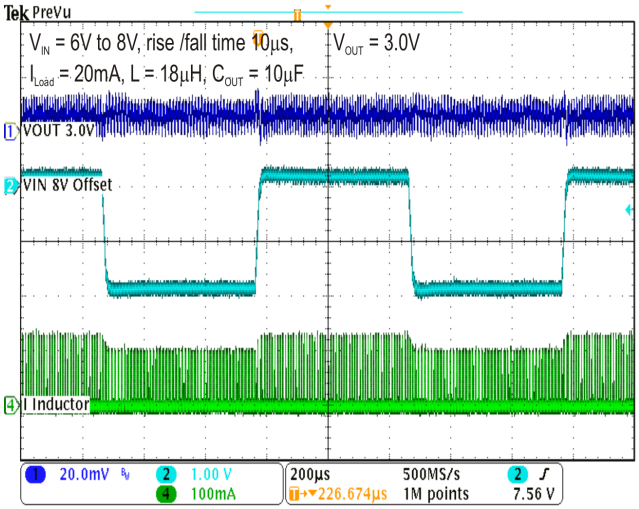


Figure 22.

LOAD TRANSIENT RESPONSE FOR 3V OUTPUT VOLTAGE

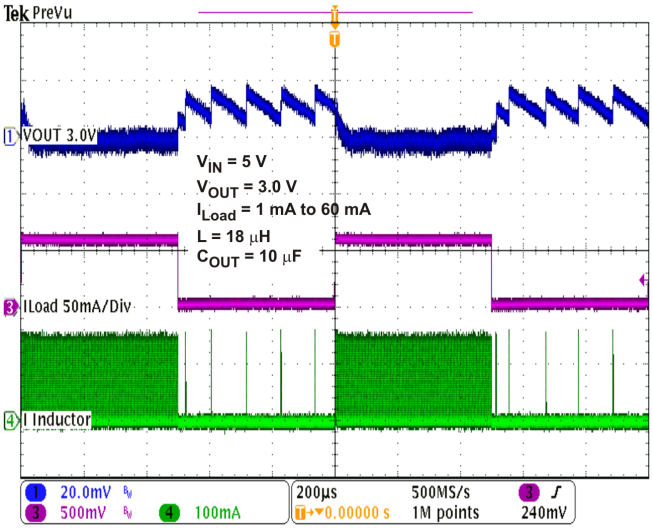


Figure 23.

AC LOAD REGULATION PERFORMANCE FOR 3V OUTPUT VOLTAGE

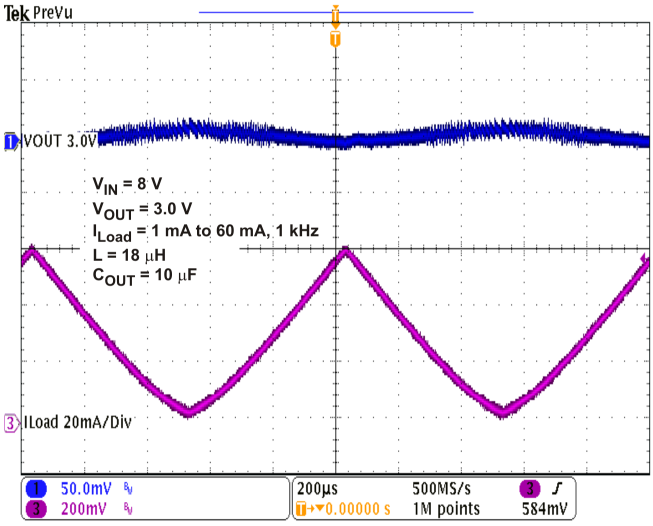


Figure 24.

TYPICAL CHARACTERISTICS (continued)

TPS62120 SPURIOUS OUTPUT NOISE
C_{OUT} = 4.7 µF

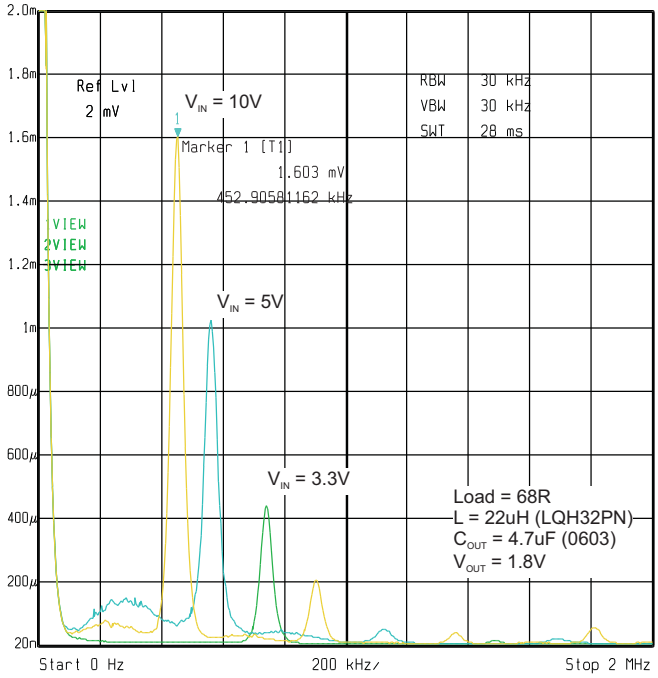


Figure 25.

TPS62120 SPURIOUS OUTPUT NOISE
C_{OUT} = 10 µF

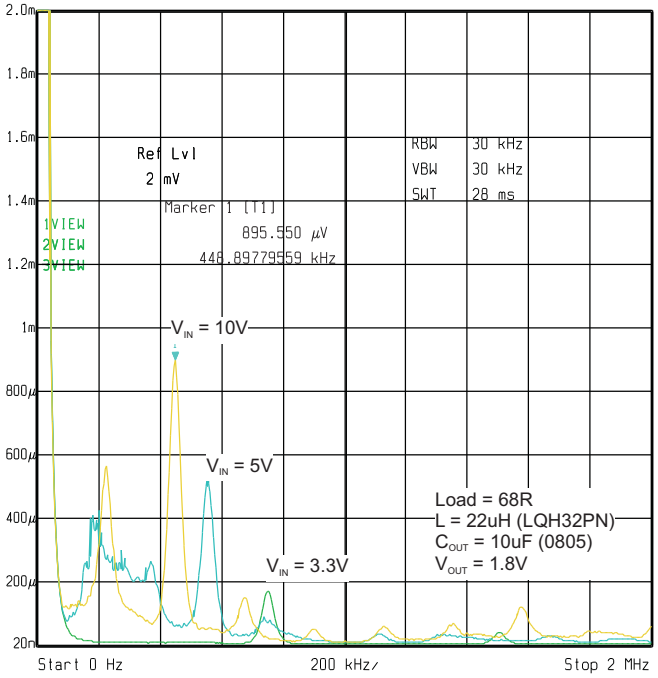


Figure 26.

AC LOAD REGULATION PERFORMANCE
FOR 1.8V OUTPUT VOLTAGE

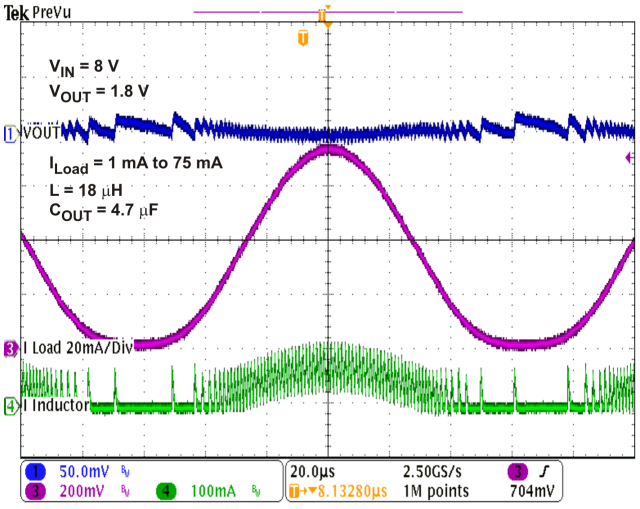


Figure 27.

OUTPUT DISCHARGE WITH SGND PIN
CONNECTED TO VOUT

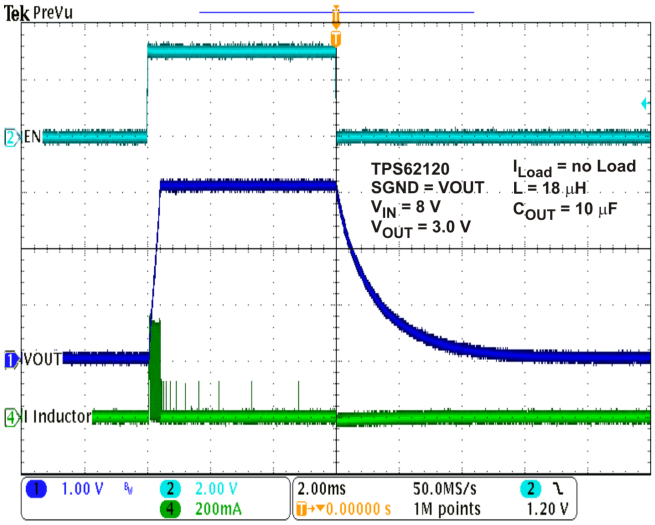


Figure 28.

TYPICAL CHARACTERISTICS (continued)

STARTUP VOUT = 3.0V

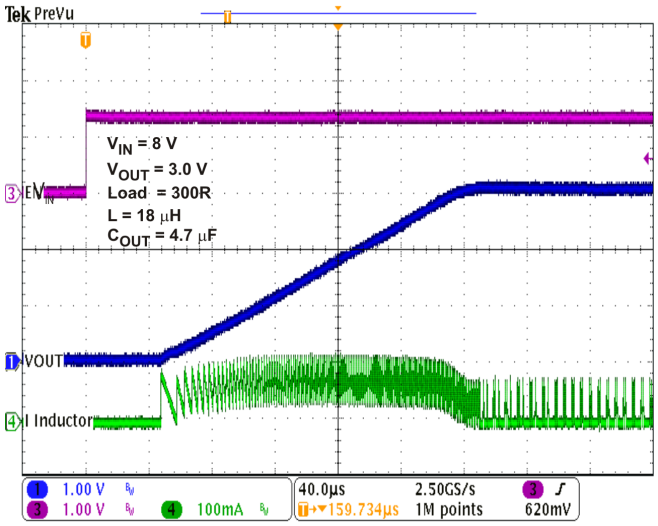


Figure 29.

POWER GOOD OUTPUT DURING STARTUP

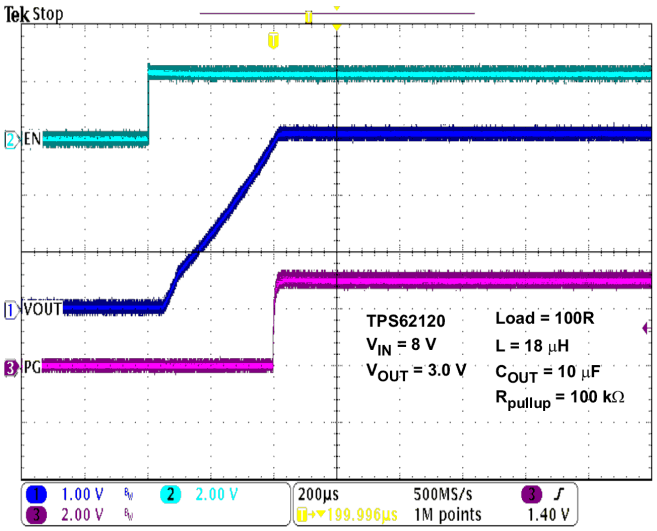


Figure 30.

STARTUP VOUT 1.8V

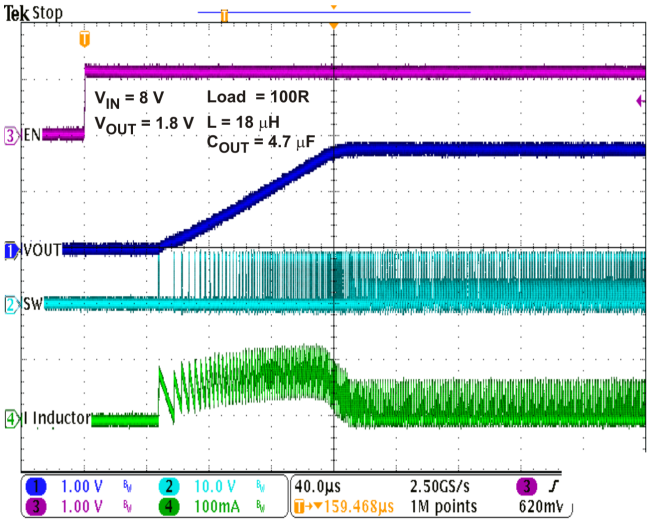


Figure 31.

OUTPUT OVERLOAD PROTECTION

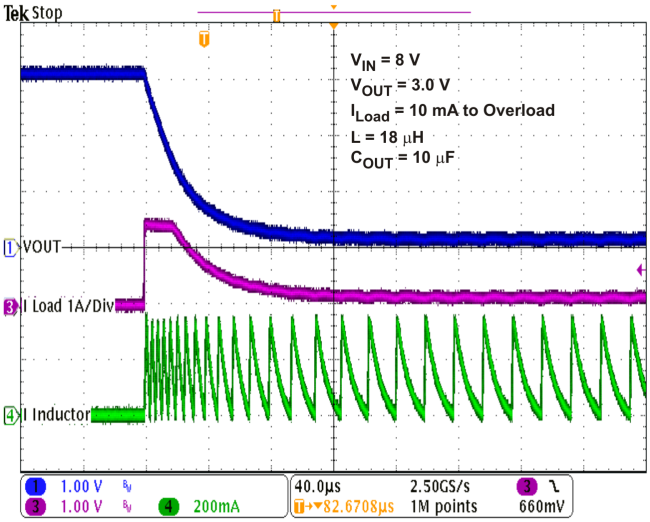


Figure 32.

TYPICAL CHARACTERISTICS (continued)

INPUT VOLTAGE RAMP UP/DOWN

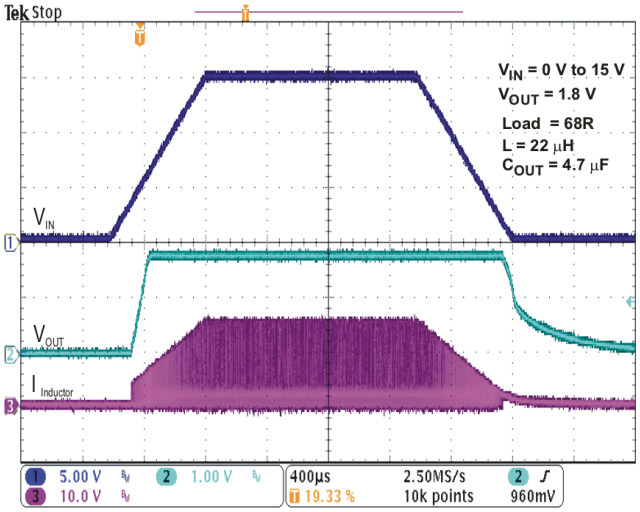


Figure 33.

STARTUP FROM A HIGH IMPEDANCE SOURCE

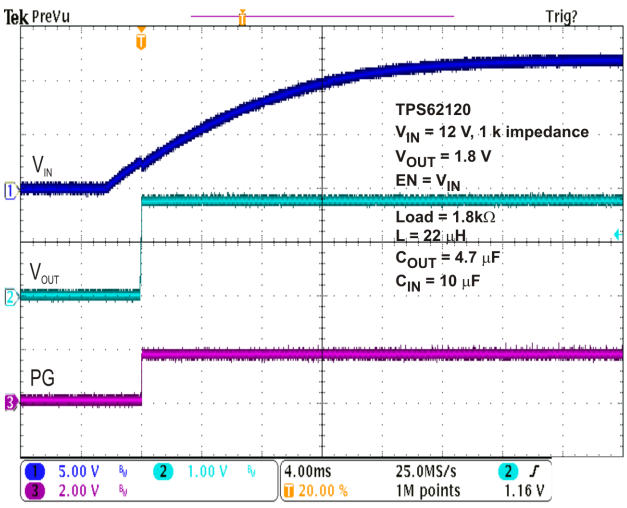


Figure 34.

DETAILED DESCRIPTION

OPERATION

The TPS6212x synchronous step down converter family uses an unique hysteretic PFM/PWM controller scheme which enables switching frequencies of up to 800kHz, excellent transient response and AC load regulation at operation with small output capacitors.

At high load currents the converter operates in quasi fixed frequency PWM mode operation and at light loads in PFM (Pulse Frequency Modulation) mode to maintain highest efficiency over the full load current range. In PFM Mode, the device generates a single switch pulse to ramp the inductor current and charge the output capacitor, followed by a sleep period where most of the internal circuits are shutdown to achieve a quiescent current of typically 10µA. During this time, the load current is supported by the output capacitor. The duration of the sleep period depends on the load current and the inductor peak current.

A significant advantage of TPS6212x compared to other hysteretic controller topologies is its excellent DC and AC load regulation capability in combination with low output voltage ripple over the entire load range which makes this part well suited for audio and RF applications.

Main Control Loop

The feedback comparator monitors the voltage on the FB pin and compares it to an internal 800mV reference voltage.

The feedback comparator trips once the FB voltage falls below the reference voltage. A switching pulse is initiated and the high-side MOSFET switch is turned on. It remains turned on at least for the minimum On Time T_{ONmin} of typical 700ns until the feedback voltage is above the reference voltage or the inductor current reaches the high-side MOSFET switch current limit I_{LIMF}. Once the high-side MOSFET switch turns off, the low-side MOSFET switch is turned on and the inductor current ramps down. It is turned on at least for the minimum Off Time T_{OFFmin} of typically 60ns. The low-side MOSFET switch stays turned on until the FB voltage falls below the internal reference and trips the FB comparator again. This will turn on the high-side MOSFET switch for a new switching cycle.

If the feedback voltage stays above the internal reference the low-side MOSFET switch is turned on until the zero current comparator trips and indicates that the inductor current has ramped down to zero. In this case, the load current is much lower than the average inductor current provided during one switching cycle. The regulator turns the low-side and high-side MOSFET switches off (high impedance state) and enters a sleep cycle with reduced quiescent current of typically 10uA until the output voltage falls below the internal reference voltage and the feedback comparator trips again. This is called PFM Mode and the switching frequency depends on the load current, input voltage, output voltage and the external inductor value.

Once the high-side switch current limit comparator has tripped its threshold of I_{LIMF}, the high-side MOSFET switch is turned off and the low-side MOSFET switch is turned on until the inductor current has ramped down to zero.

The minimum On Time T_{ONmin} for a single pulse can be estimated to:

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} \times 1.3\ \mu s \quad (1)$$

Therefore the peak inductor current in PFM mode is approximately:

$$I_{LPFMpeak} = \frac{(V_{IN} - V_{OUT})}{L} \times T_{ON} \quad (2)$$

The transition from PFM mode to PWM mode operation and back occurs at a load current of approximately ½ $I_{LPFMpeak}$.

With:

T_{ON}: high-side MOSFET switch on time [µs]
V_{IN}: Input voltage [V]
V_{OUT}: Output voltage [V]
L : Inductance [µH]
$I_{LPFMpeak}$: PFM inductor peak current [mA]

The maximum switch frequency can be estimated to:

$$f_{SWmax} \approx \frac{1}{1.3\,\mu s} = 770\ kHz \quad (3)$$

100% DUTY CYCLE LOW DROPOUT OPERATION

The device will increase the On Time of the high-side MOSFET switch once the input voltage comes close to the output voltage in order to keep the output voltage in regulation. This will reduce the switch frequency.

With further decreasing input voltage V_{IN} the high-side MOSFET switch is turned on completely. In this case the converter provides a low input-to-output voltage difference. This is particularly useful in applications with widely variable supply voltage to achieve longest operation time by taking full advantage of the whole supply voltage span.

The minimum input voltage to maintain regulation depends on the load current and output voltage, and can be calculated as:

$$Vin_{min} = Vout_{max} + Iout_{max} \times \left(R_{DSONmax} + R_L\right) \quad (4)$$

With:

I_{OUTmax} = maximum output current
$R_{DS(ON)max}$ = maximum P-channel switch $R_{DS(ON)}$.
R_L = DC resistance of the inductor
V_{OUTmax} = nominal output voltage plus maximum output voltage tolerance

UNDER-VOLTAGE LOCKOUT

The under-voltage lockout circuit prevents the device from misoperation at low input voltages. It prevents the converter from turning on the high-side MOSFET switch or low-side MOSFET under undefined conditions. The UVLO threshold is set to 2.5V typical for rising VIN and 1.85V typical for falling VIN. The hysteresis between rising and falling UVLO threshold ensures proper start up even with high impedance sources. Fully functional operation is permitted for an input voltage down to the falling UVLO threshold level. The converter starts operation again once the input voltage trips the rising UVLO threshold level.

SOFT START

The TPS6212X has an internal soft-start circuit which controls the ramp up of the output voltage and limits the inrush current during start-up. This limits input voltage drop when a battery or a high-impedance power source is connected to the input of the converter.

The soft-start system generates a monotonic ramp up of the output voltage with a ramp of typically 15mV/µs and reaches an output voltage of 1.8V in typically 170µs after EN pin was pulled high. TPS6212X is able to start into a pre biased output capacitor. The converter starts with the applied bias voltage and ramps the output voltage to its nominal value.

During start up the device can provide an output current of half of the high-side MOSFET switch current limit I_{LIMF}. Large output capacitors and high load currents may exceed the current capability of the device during start up. In this case the start up ramp of the output voltage will be slower.

ENABLE/SHUTDOWN

The device starts operation when EN pin is set high and the input voltage V_{IN} has tripped the under voltage lockout threshold UVLO for rising V_{IN}. It starts switching after the regulator start up time t_{Start} of typically 50µs has expired and enters the soft start as previously described. For proper operation, the EN pin must be terminated and must not be left floating.

EN pin low forces the device into shutdown, with a shutdown quiescent current of typically 0.3µA.

In this mode, the high-side and low-side MOSFET switches as well as the entire internal-control circuitry are switched off.

In TPS62120 the internal N-MOSFET at pin SGND is activated and connects SGND to GND.

POWER GOOD OUTPUT

The Power Good Output is an open drain output available in TPS62120. The circuit is active once the device is enabled. It is driven by an internal comparator connected to the FB voltage and internal reference. The PG output provides a high level (open drain high impedance) once the feedback voltage exceeds typical 95% of its nominal value. The PG output is driven to low level once the feedback voltage falls below typ. 90% of its nominal value. The PG output is high (high impedance) with an internal delay of typically 2µs. A pullup resistor is needed to generate a high level and limit the current into the PG pin to 0.5mA. The PG pin can be connected via an pull up resistors to a voltage up to 5.5V

The PG output is pulled low if the device is enabled but the input voltage is below the undervoltage lockout threshold UVLO or the device is turned into shutdown mode.

SGND OPEN DRAIN OUTPUT

This is an NMOS open drain output with a typical $R_{DS(on)}$ of 370Ω and can be used to discharge the output capacitor. The internal NMOS connects SGND pin to GND once the device is in shutdown mode or V_{IN} falls below the UVLO threshold during operation. SGND becomes high impedance once the device is enabled and V_{IN} is above the UVLO threshold. If SGND is connected to the output, the output capacitor is discharged through SGND.

SHORT-CIRCUIT PROTECTION

The TPS6212X integrates a high-side MOSFET switch current limit I_{LIMF} to protect the device against short circuit. The current in the high-side MOSFET switch is monitored by current limit comparator and once the current reaches the limit of I_{LIMF} , the high-side MOSFET switch is turned off and the low-side MOSFET switch is turned on to ramp down the inductor current. The high-side MOSFET switch is turned on again once the zero current comparator trips and the inductor current has become zero. In this case, the output current is limited to half of the high-side MOSFET switch current limit ½ I_{LIMF}.

THERMAL SHUTDOWN

As soon as the junction temperature, T_J, exceeds 150°C (typical) the device goes into thermal shutdown. In this mode, the high-side and low-side MOSFETs are turned-off. The device continues its operation when the junction temperature falls below the thermal shutdown hysteresis.

APPLICATION INFORMATION

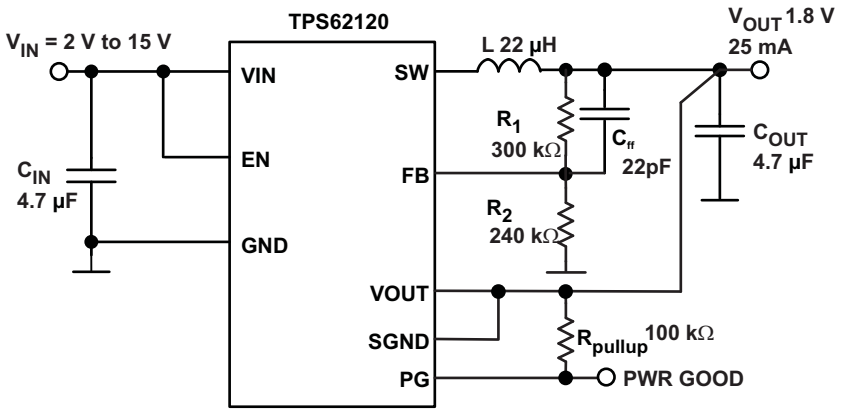


Figure 35. TPS62120 1.8V Output Voltage Configuration

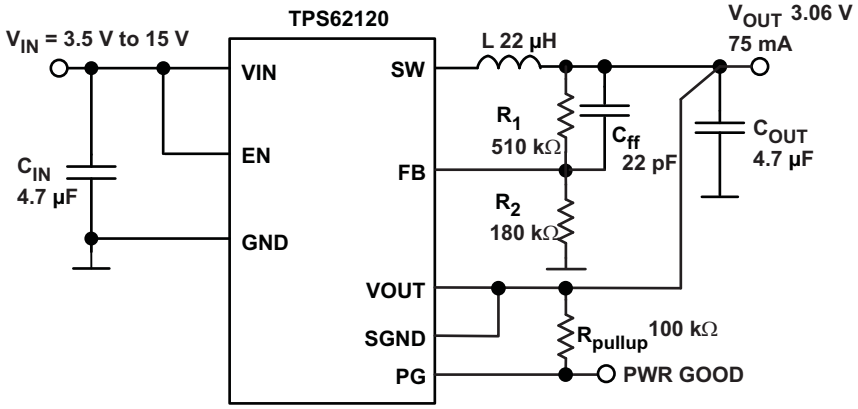


Figure 36. TPS62120 3.06V Output Voltage Configuration

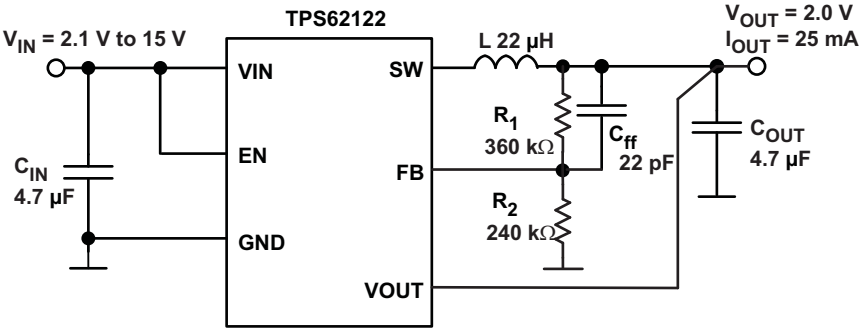


Figure 37. TPS62122 2.0V Output Voltage Configuration

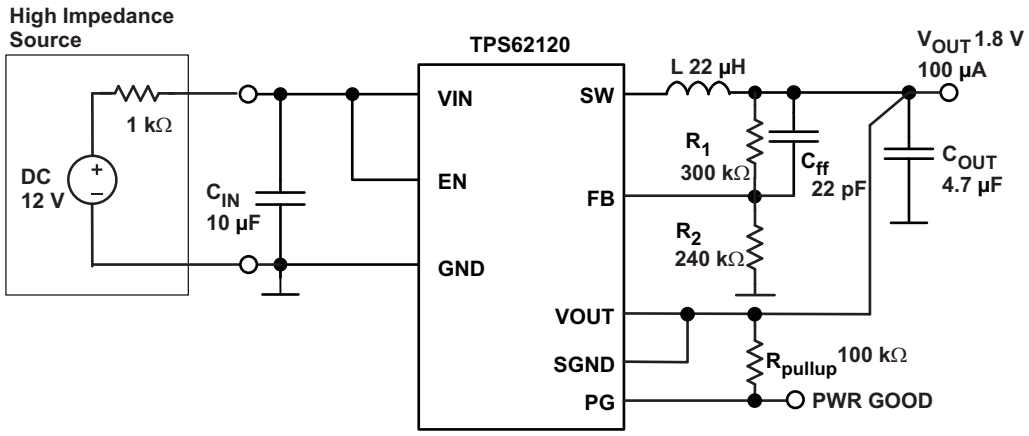


Figure 38. TPS62120 1.8V VOUT Configuration Powered from a High-Impedance Source

OUTPUT VOLTAGE SETTING

The output voltage can be calculated to:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right) \text{ with an internal reference voltage VREF typical 0.8 V}$$

$$R_1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R_2 \quad (5)$$

To minimize the current through the feedback divider network, R_2 should be within the range of 82kΩ to 360k. The sum of R_1 and R_2 should not exceed ~1MΩ, to keep the network robust against noise. An external feed-forward capacitor Cff is required for optimum regulation performance. R_1 and C_{ff} places a zero in the feedback loop.

$$f_z = \frac{1}{2 \times \pi \times R_1 \times C_{ff}} = 25 \text{ kHz} \quad (6)$$

The value for C_{ff} can be calculated as:

$$C_{ff} = \frac{1}{2 \times \pi \times R_1 \times 25 \text{ kHz}} \quad (7)$$

Table 1 shows a selection of suggested values for the feedback divider network for most common output voltages.

Table 1. Suggested Values for Feedback Divider Network

Voltage Setting [V]	3.06	3.29	2.00	1.80	1.20	5.00
R1 [kΩ]	510	560	360	300	180	430
R2 [kΩ]	180	180	240	240	360	82
Cff [pF]	15	22	22	22	27	15

OUTPUT FILTER DESIGN (INDUCTOR AND OUTPUT CAPACITOR)

The TPS6212X operates with effective inductance values in the range of 10µH to 33µH and with effective output capacitance in the range of 1µF to 33µF. The device is optimized to operate for an output filter of L = 22µH and C_{OUT} = 4.7µF. Larger or smaller inductor/capacitor values can be used to optimize the performance of the device for specific operation conditions. For more details, see the CHECKING LOOP STABILITY section.

INDUCTOR SELECTION

The inductor value affects its peak-to-peak ripple current, the PWM-to-PFM transition point, the output voltage ripple and the efficiency. The selected inductor has to be rated for its DC resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher V_{IN} or V_{OUT} and can be estimated according Equation 8.

Equation 9 calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation 9. This is recommended because during heavy load transient the inductor current will rise above the calculated value. A more conservative way is to select the inductor saturation current according to the high-side MOSFET switch current limit I_{LIMF}.

$$\Delta I_L = \frac{(V_{IN} - V_{OUT})}{L} \times T_{ON} \quad (8)$$

$$I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2} \quad (9)$$

With:

T_{ON} = see equation (3)
L = Inductor Value
ΔI_L = Peak to Peak inductor ripple current
I_{Lmax} = Maximum Inductor current

In DC/DC converter applications, the efficiency is essentially affected by the inductor AC resistance (i.e. quality factor) and by the inductor DCR value. To achieve high efficiency operation, care should be taken in selecting inductors featuring a quality factor above 25 at the switching frequency. Increasing the inductor value produces lower RMS currents, but degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current.

The total losses of the coil consist of both the losses in the DC resistance $R_{(DC)}$) and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

The following inductor series from different suppliers have been used with the TPS6212X converters.

Table 2. List of Inductors

INDUCTANCE [µH]	DIMENSIONS [mm^3]	INDUCTOR TYPE	SUPPLIER
22	3 × 3 × 1.5	LQH3NPN	Murata
18/22	3 × 3 × 1.5	LPS3015	Coilcraft

OUTPUT CAPACITOR SELECTION

The unique hysteretic PFM/PWM control scheme of the TPS6212x allows the use of ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies.

At light load currents the converter operates in Power Save Mode and the output voltage ripple is dependent on the output capacitor value and the PFM peak inductor current. Higher output capacitor values minimize the voltage ripple in PFM Mode and tighten DC output accuracy in PFM Mode.

INPUT CAPACITOR SELECTION

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. For most applications a 4.7µF to 10µF ceramic capacitor is recommended. The voltage rating and DC bias characteristic of ceramic capacitors need to be considered. The input capacitor can be increased without any limit for better input voltage filtering.

For specific applications like energy harvesting a tantalum or tantalum polymer capacitor can be used to achieve a specific DC/DC converter input capacitance. Tantalum capacitors provide much better DC bias performance compared to ceramic capacitors. In this case a 1µF or 2.2µF ceramic capacitor should be used in parallel to provide low ESR.

Take care when using only small ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output or V_{IN} step on the input can induce large ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part by exceeding the maximum ratings.

Table 3 shows a list of input/output capacitors.

Table 3. List of Capacitor

CAPACITANCE [µF]	SIZE	CAPACITOR TYPE	USAGE	SUPPLIER
4.7	0603	GRM188 series 6.3V X5R	C_{OUT}	Murata
2.2	0603	GRM188 series 6.3V X5R	C_{OUT}	Murata
4.7	0805	GRM21Bseries 25V X5R	C_{IN}	Murata
10	0805	GRM21Bseries 16V X5R	C_{IN}	Murata
8.2	B2(3.5 × 2.8 × 1.9)	20TQC8R2M (20V)	C_{IN}	Sanyo

CHECKING LOOP STABILITY

The first step of circuit and stability evaluation is to look from a steady-state perspective at the following signals:

- Switching node, SW
- Inductor current, I_L
- Output ripple voltage, $V_{O(AC)}$

These are the basic signals that need to be measured when evaluating a switching converter. When the switching waveform shows large duty cycle jitter or the output voltage or inductor current shows oscillations, the regulation loop may be unstable. This is often a result of board layout and/or L-C combination.

As a next step in the evaluation of the regulation loop, the load transient response is tested. During application of the load transient and the turn on of the high-side MOSFET switch, the output capacitor must supply all of the current required by the load. V_{OUT} immediately shifts by an amount equal to $\Delta I_{(LOAD)}$ × ESR, where ESR is the effective series resistance of C_{OUT}. $\Delta I_{(LOAD)}$ begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. The results are most easily interpreted when the device operates in PWM mode.

During this recovery time, V_{OUT} can be monitored for settling time, overshoot or ringing that helps judge the converter's stability. Without any ringing, the loop has usually more than 45° of phase margin. Because the damping factor of the circuitry is directly related to several resistive parameters (e.g., MOSFET $R_{DS(on)}$) which are temperature dependent, the loop stability analysis should be done over the input voltage range, load current range, and temperature range

LAYOUT CONSIDERATIONS

As for all switching power supplies, the layout is an important step in the design. Proper function of the device demands careful attention to PCB layout. Care must be taken in board layout to get the specified performance. If the layout is not carefully done, the regulator could show poor line and/or load regulation, stability issues as well as EMI problems. It is critical to provide a low inductance, impedance ground path. Therefore, use wide and short traces for the main current paths. The input capacitor should be placed as close as possible to the IC pins as well as the inductor and output capacitor.

Use a common Power GND node and a different node for the signal GND to minimize the effects of ground noise. Keep the common path to the GND PIN, which returns the small signal components and the high current of the output capacitors as short as possible to avoid ground noise. The FB divider network and the VOUT line must be connected to the output capacitor. The VOUT pin of the converter should be connected via a short trace to the output capacitor. The FB line must be routed away from noisy components and traces (e.g., SW line).

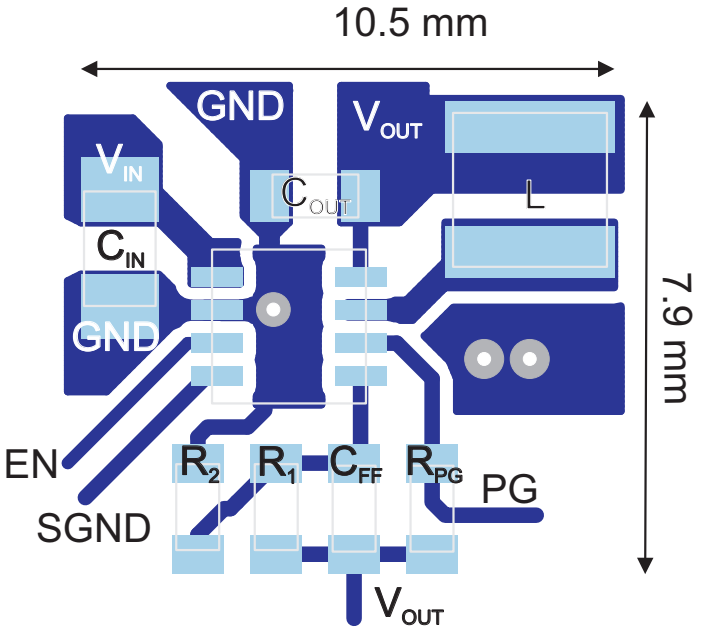


Figure 39. PCB Layout - DCN Package

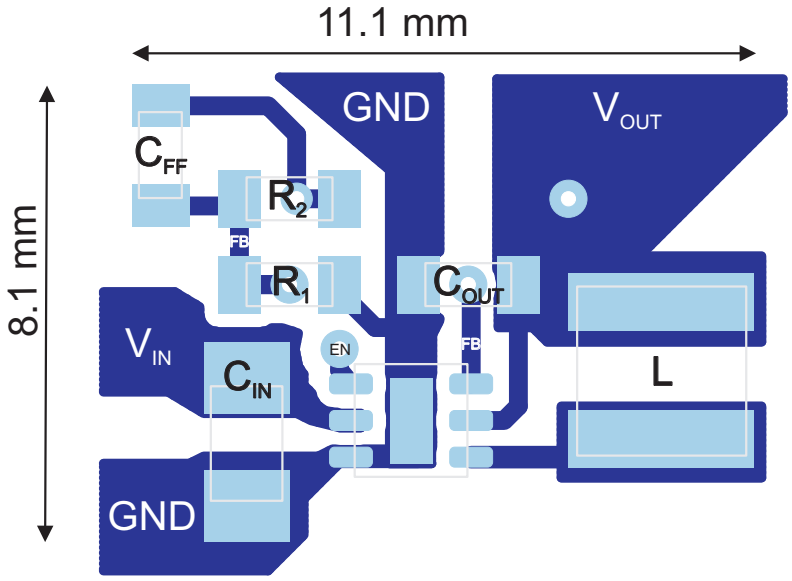


Figure 40. PCB Layout - DRV Package

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS62120DCNR	ACTIVE	SOT-23	DCN	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	QTX	Samples
TPS62120DCNT	ACTIVE	SOT-23	DCN	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	QTX	Samples
TPS62122DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OFZ	Samples
TPS62122DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OFZ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

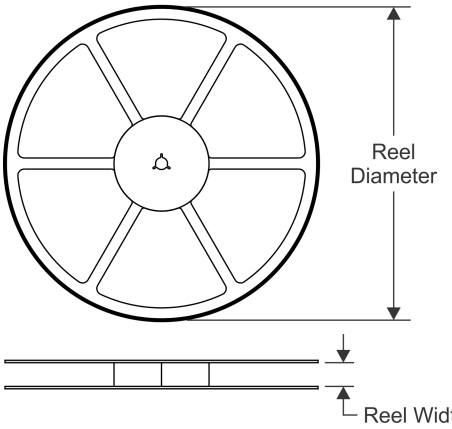
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

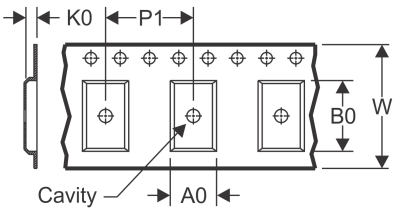
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

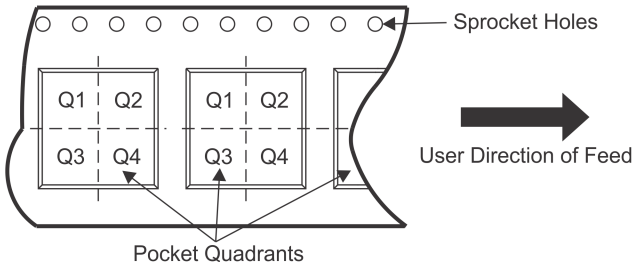


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

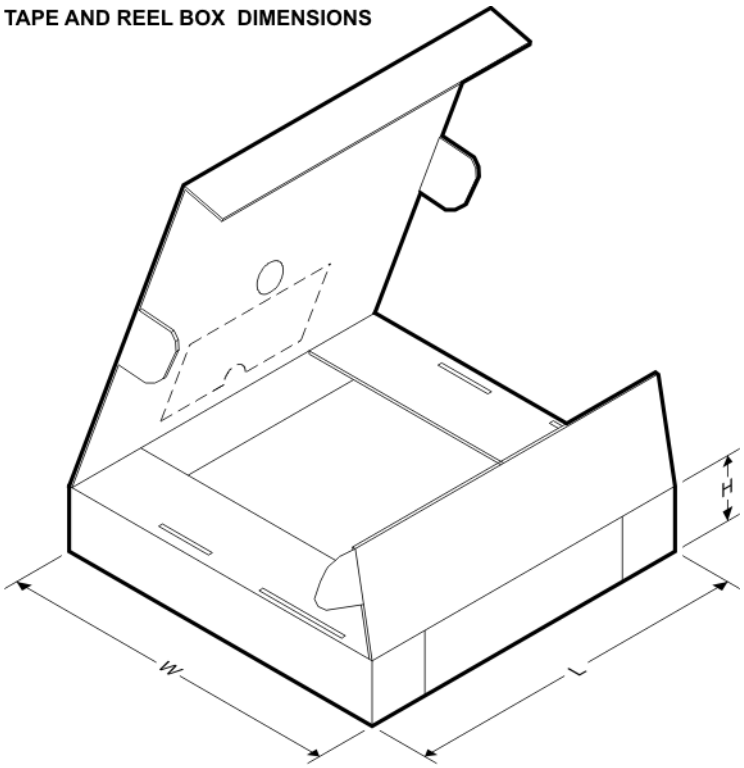
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62120DCNR	SOT-23	DCN	8	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TPS62120DCNR	SOT-23	DCN	8	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS62120DCNT	SOT-23	DCN	8	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TPS62120DCNT	SOT-23	DCN	8	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS62122DRVR	SON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62122DRVR	SON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS62122DRVT	SON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62122DRVT	SON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

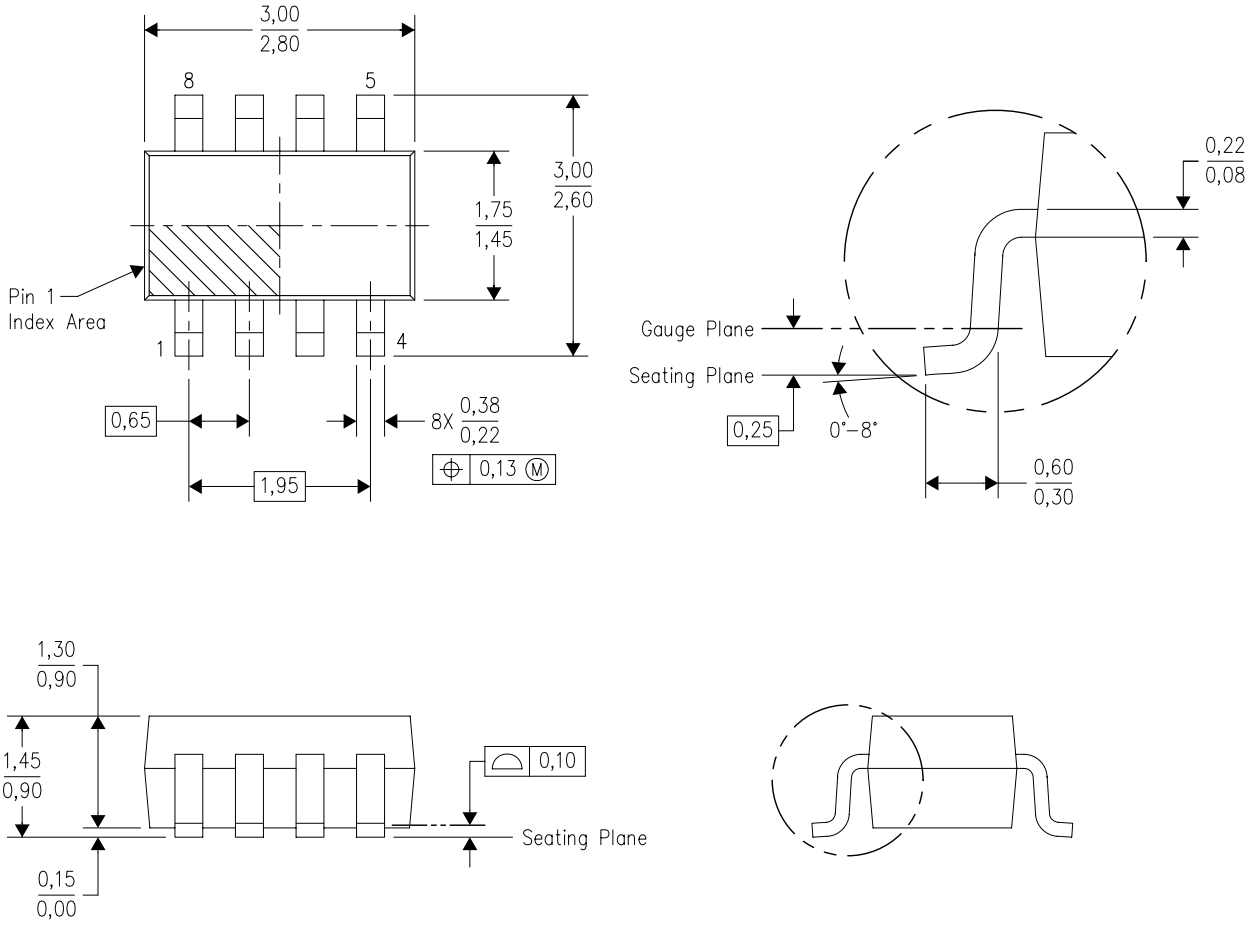
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

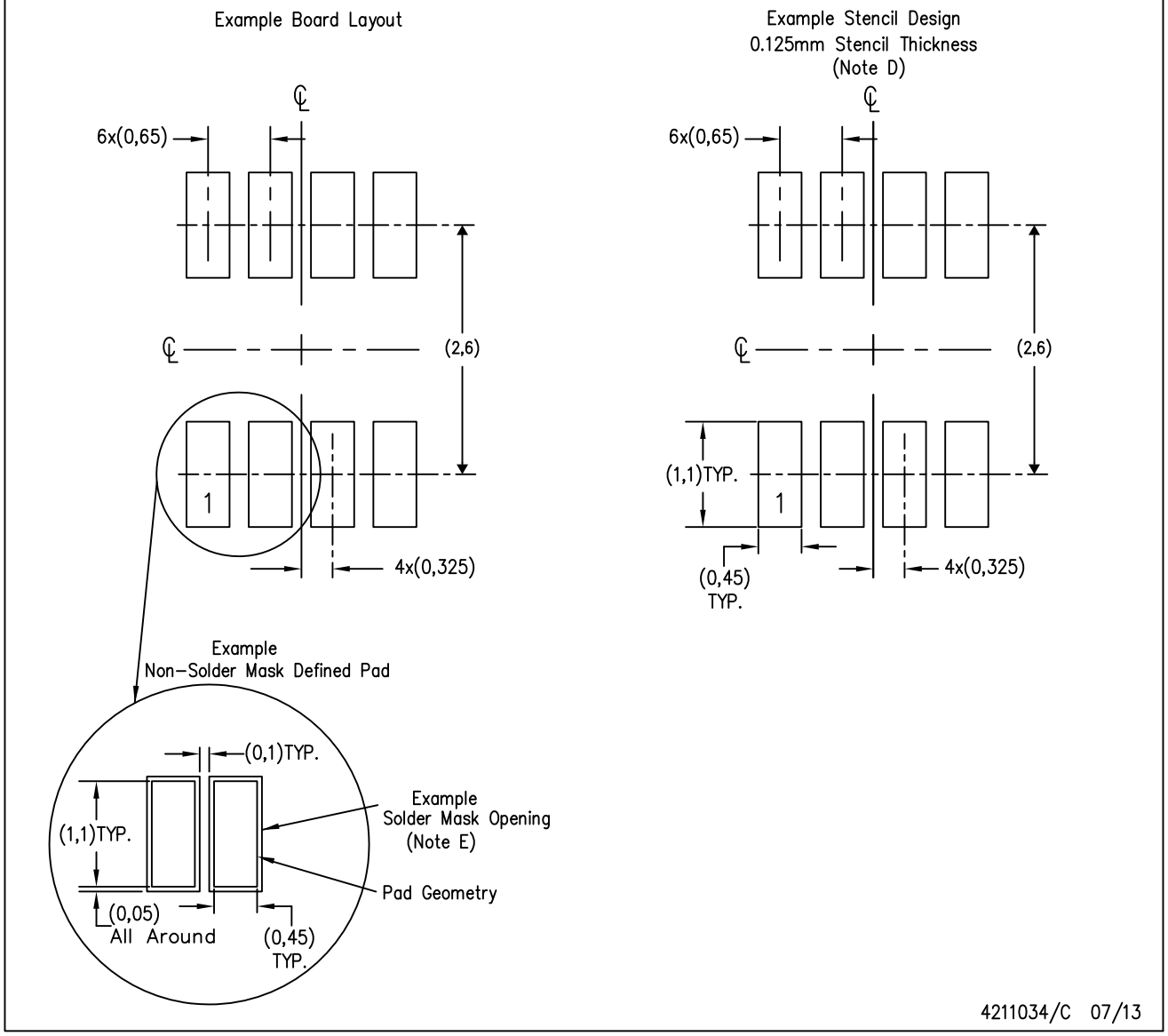
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62120DCNR	SOT-23	DCN	8	3000	202.0	201.0	28.0
TPS62120DCNR	SOT-23	DCN	8	3000	203.0	203.0	35.0
TPS62120DCNT	SOT-23	DCN	8	250	202.0	201.0	28.0
TPS62120DCNT	SOT-23	DCN	8	250	203.0	203.0	35.0
TPS62122DRVR	SON	DRV	6	3000	210.0	185.0	35.0
TPS62122DRVR	SON	DRV	6	3000	203.0	203.0	35.0
TPS62122DRVT	SON	DRV	6	250	210.0	185.0	35.0
TPS62122DRVT	SON	DRV	6	250	203.0	203.0	35.0

DCN (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



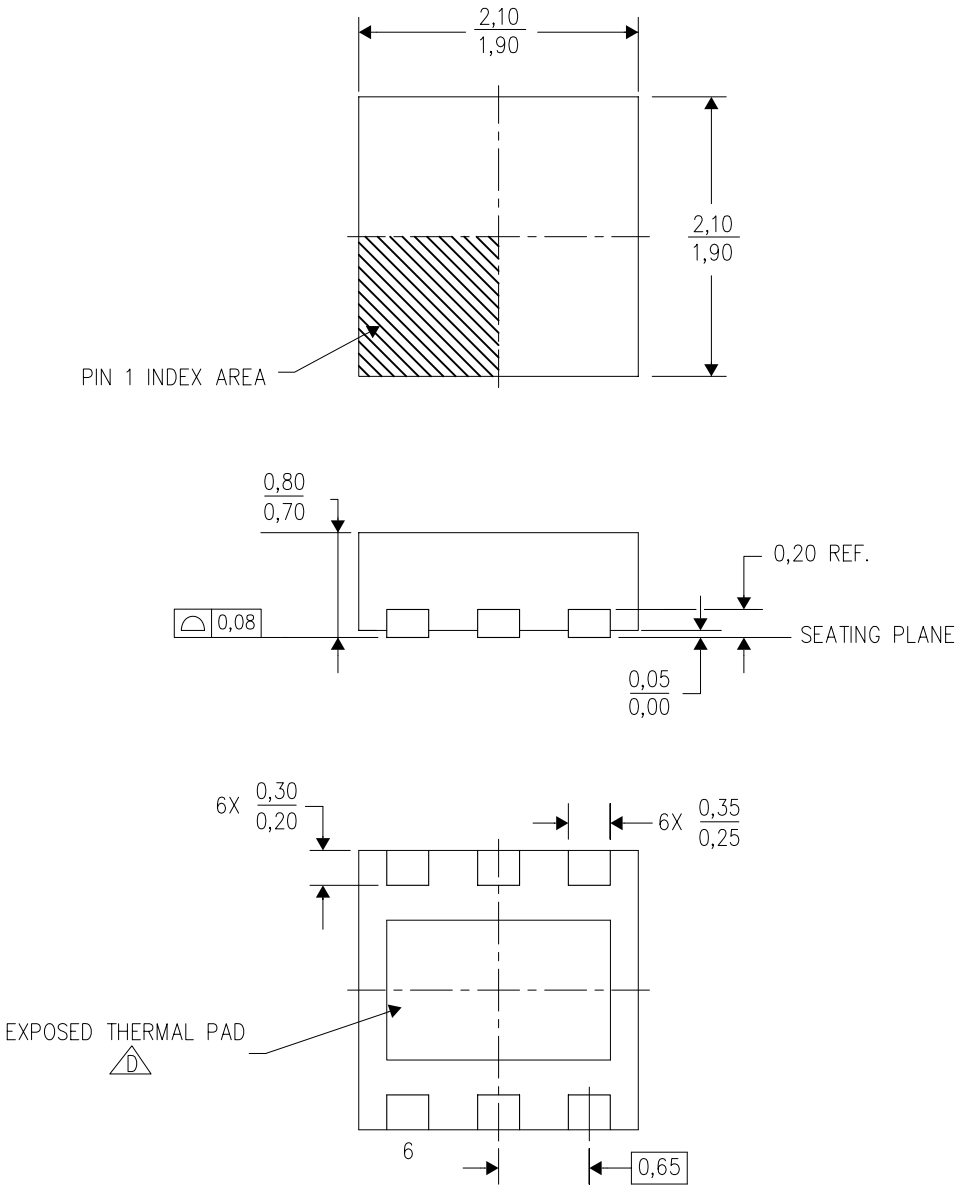
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Package outline exclusive of metal burr & dambar protrusion/intrusion.
D. Package outline inclusive of solder plating.
E. A visual index feature must be located within the Pin 1 index area.
F. Falls within JEDEC MO–178 Variation BA.
G. Body dimensions do not include flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

DCN (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



4206925/E 10/10

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

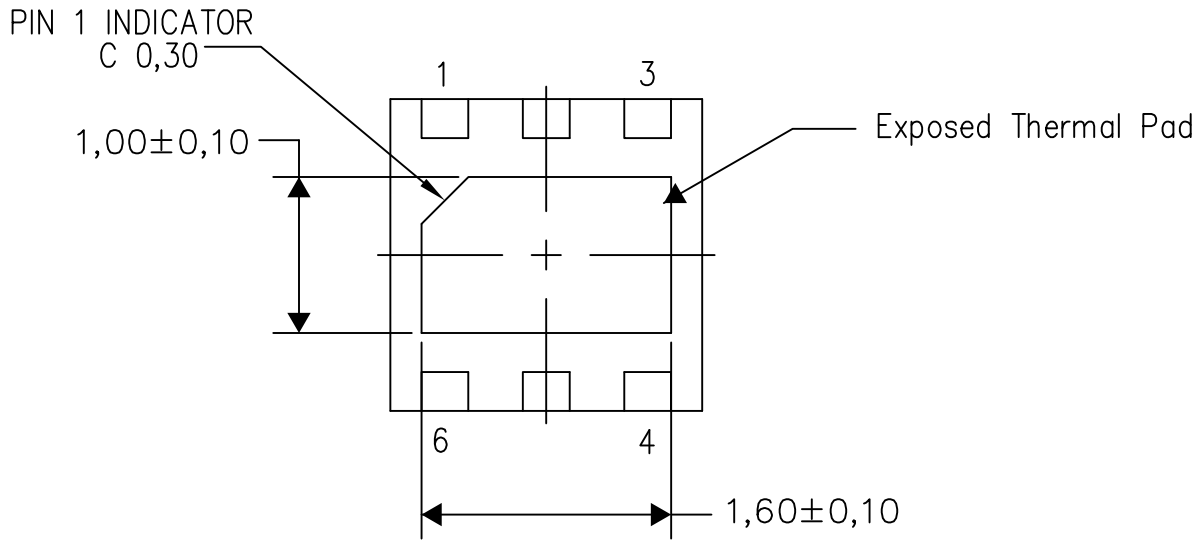
DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



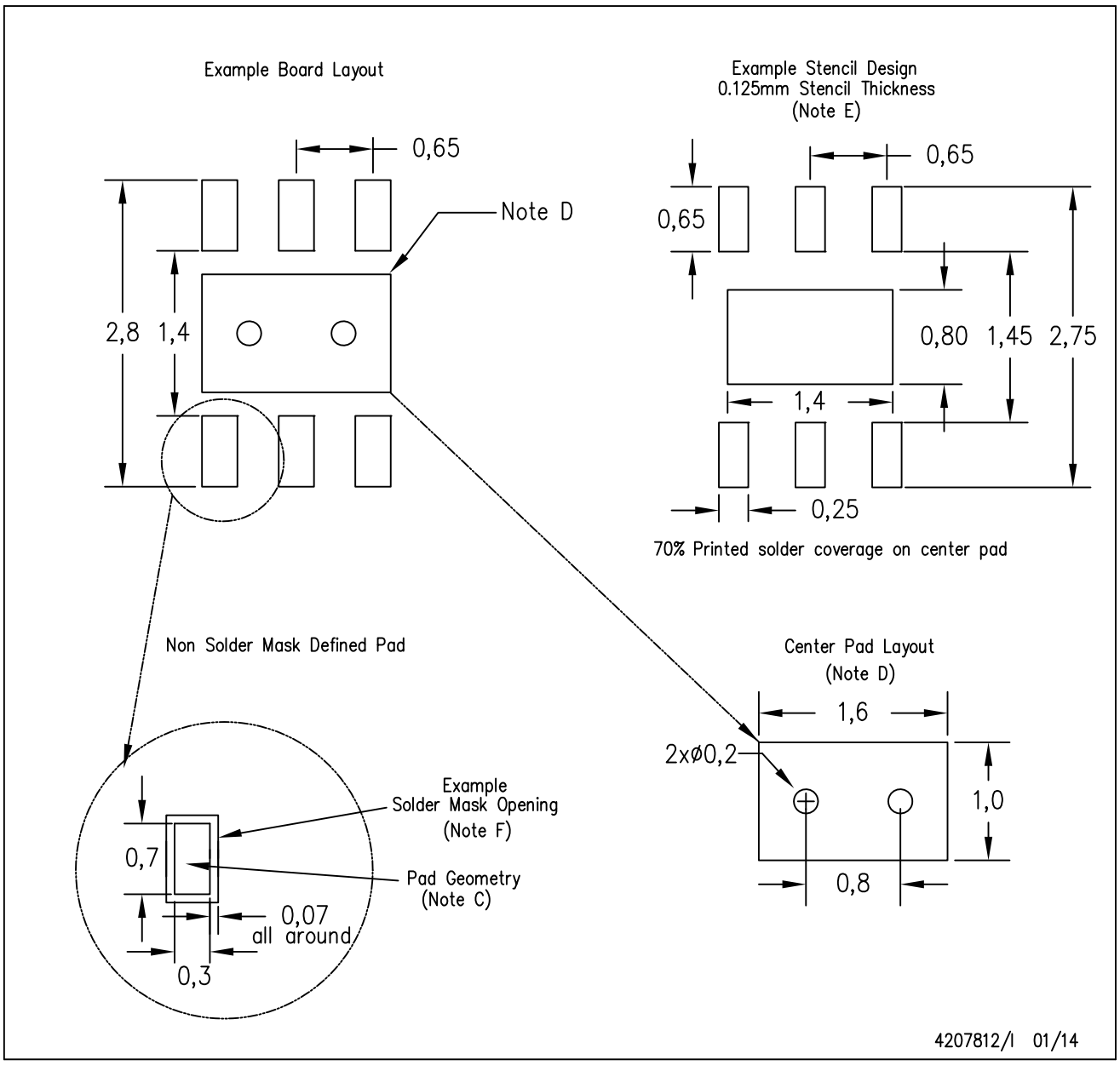
Bottom View

Exposed Thermal Pad Dimensions

4206926/0 01/14

NOTE: All linear dimensions are in millimeters

DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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