LMV712-N, LMV712-N-Q1 Low Power, Low Noise, High Output, RRIO Dual Operational Amplifier With Independent Shutdown

1 Features

- Available In Automotive AEC-Q100 Grade 1 Version (LMV712-N Only)
- 5-MHz GBP
- Slew Rate: 5 V/µs
- Low Noise: 20 nV/√Hz
- Supply Current: 1.22 mA/Channel
- V_{OS}< 3 mV Maximum
- Ensured 2.7-V and 5-V Specifications
- Temperature Range: –40°C to 125°C
- Rail-to-Rail Inputs and Outputs
- Unity Gain Stable
- Small Package: 10-Pin DSBGA, 10-Pin WSON, and 10-Pin VSSOP
- 1.5-µA Shutdown I_{CC}
- 2.2-µs Turnon

2 Applications

- Power Amplifier Control Loops
- Cellular Phones
- Portable Equipment
- Wireless LAN
- Radio Systems
- Cordless Phones

3 Description

The LMV712-N devices are high-performance BiCMOS operational amplifiers intended for applications requiring rail-to-rail inputs combined with speed and low noise. They offer a bandwidth of 5 MHz and a slew rate of 5 V/µs, and can handle capacitive loads of up to 200 pF without oscillation.

The LMV712-N is ensured to operate from 2.7 V to 5.5 V and offers two independent shutdown pins. This feature allows disabling of each device separately and reduces the supply current to less than 1 µA typical. The output voltage rapidly ramps up smoothly with no glitch as the amplifier comes out of the shutdown mode.

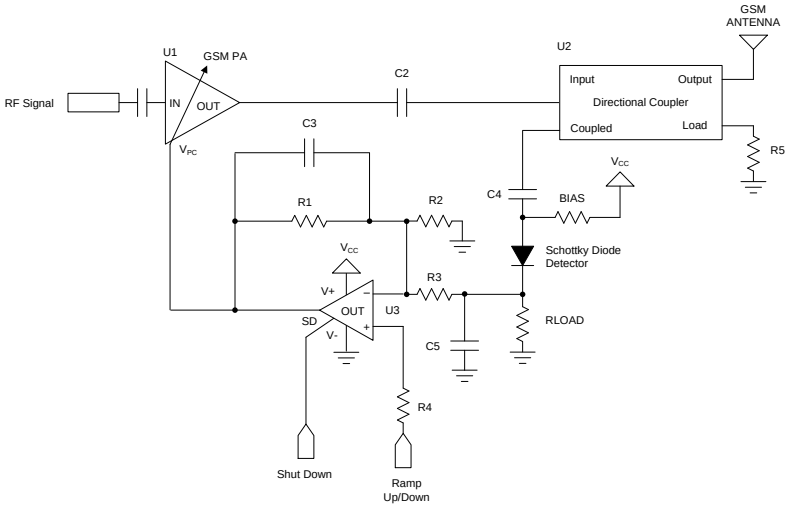
The LMV712-N with the shutdown feature is offered in space-saving 10-pin DSBGA and 10-pin WSON packages. It is also offered in 10-pin VSSOP package. These packages are designed to meet the demands of small size, low power, and low cost required by cellular phones and similar battery-operated portable electronics.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMV712-N	DSBGA (10)	1.75 mm × 2.25 mm
	WSON (10)	3.00 mm × 3.00 mm
LMV712-N, LMV712-N-Q1	VSSOP (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Power Amplifier Control Loop



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision I (January 2014) to Revision J — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted Soldering specification from *Absolute Maximum Ratings* table ... 6
- Changed Thermal Resistance values in *Thermal Information* table From: 196 To: 84.1 (DSBGA), From: 53.4 To: 70 (WSON), and From: 235 To: 176.8 (VSSOP) ... 6

Changes from Revision H (February 2013) to Revision I — **Page**

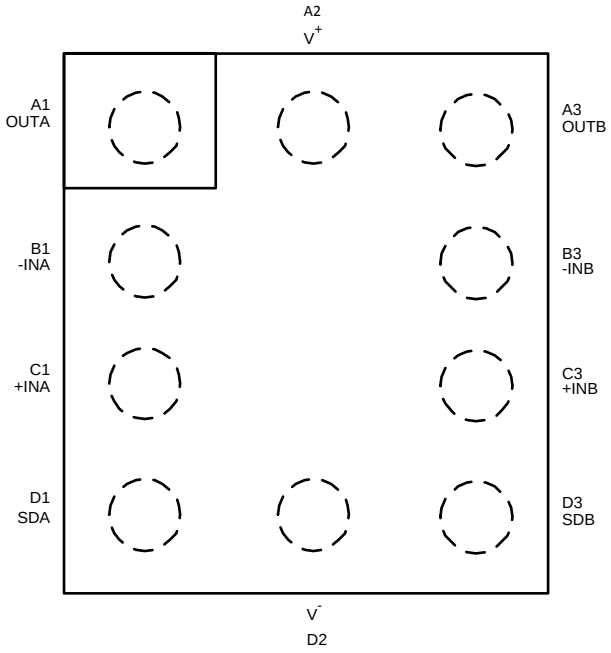
- Added -Q1 part ... 1

Changes from Revision G (February 2013) to Revision H — **Page**

- Changed layout of National Semiconductor Data Sheet to TI format ... 1

5 Pin Configuration and Functions

YPA Package
10-Pin DSBGA
Top View

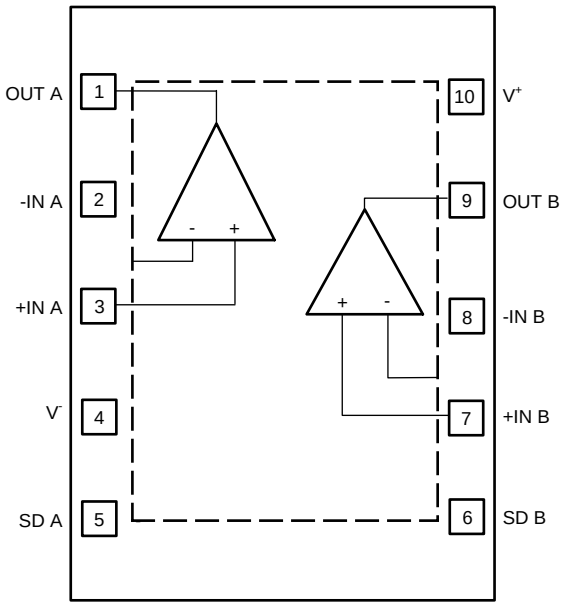


Pin Functions: DSBGA Package

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
A1	OUTA	O	Channel A output
A2	V+	P	Positive supply input
A3	OUTB	O	Channel B output
B1	–INA	I	Channel A inverting input
B3	–INB	I	Channel B inverting input
C1	+INA	I	Channel A noninverting input
C3	+INB	I	Channel A noninverting input
D1	SDA	I	Channel A shutdown
D2	V–	P	Negative supply input
D3	SDB	I	Channel B shutdown

(1) I = Input, O = Output, P = Power

NGY Package
10-Pin WSON
Top View

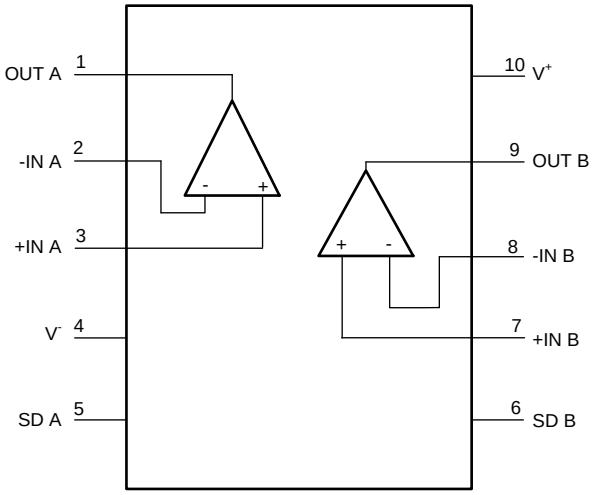


Pin Functions: WSON Package

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	OUT A	O	Channel A output
2	–IN A	I	Channel A inverting input
3	+IN A	I	Channel A noninverting input
4	V^-	P	Positive supply input
5	SD A	I	Channel A shutdown
6	SD B	I	Channel B shutdown
7	+IN B	I	Channel B noninverting input
8	–IN A	I	Channel B inverting input
9	OUT B	O	Channel B output
10	V^+	P	Positive supply input
11	Thermal Pad	G	Connect thermal pad to V^- or leave floating

(1) G = Ground, I = Input, O = Output, P = Power

DGS Package
10-Pin VSSOP
Top View



Pin Functions: VSSOP Package

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	OUT A	O	Channel A output
2	–IN A	I	Channel A inverting input
3	+IN A	I	Channel A noninverting input
4	V^-	P	Negative supply input
5	SD A	I	Channel A shutdown
6	SD B	I	Channel B shutdown
7	+IN B	I	Channel B noninverting input
8	–IN A	I	Channel B inverting input
9	OUT B	O	Channel B output
10	V^+	P	Positive supply input

(1) I = Input, O = Output, P = Power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
	Differential input voltage	±Supply voltage		
	Voltage at input or output pin	(V^+) + 0.4	(V^-) – 0.4	V
	Supply voltage $(V^+ – V^-)$		6	V
V^+, V^-	Output short circuit		See(3)	
	Current at input pin		±10	mA
	Current at output pin		±50	mA
T_{JMAX}	Junction temperature(4)		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the *Electrical Characteristics*.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office / Distributors for availability and specifications.
(3) Shorting circuit output to either V^+ or V^- adversely affects reliability.
(4) The maximum power dissipation is a function of $T_{J(MAX)}$ and $R_{\theta JA}$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±150	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage		2.7	5.5	V
Operating temperature	LMV712	–40	85	°C
	LMV712-Q1	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LMV712-N, LMV712-N-Q1			UNIT
		YPA (DSBGA)	NGY (WSON)	DGS (VSSOP)	
		10 PINS	10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	84.1	70	176.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.6	74.7	67.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	21.4	43.7	97.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.2	2	9.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	21.3	43.7	95.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	11.8	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics – 2.7 V

All limits ensured for V^+ = 2.7 V, V^- = 0 V, V_{CM} = 1.35 V, T_A = 25°C, and R_L > 1 mΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN(1)	TYP(2)	MAX(1)	UNIT
V_{OS}	Input offset voltage (WSON and VSSOP)	V_{CM} = 0.85 V and V_{CM} = 1.85 V	T_A = 25°C		0.4	3	mV
			−40°C ≤ T_J ≤ 85°C (LMV712) or −40°C ≤ T_J ≤ 125°C (LMV712-Q1)			3.2	
	Input offset voltage (DSBGA only)	V_{CM} = 0.85 V and V_{CM} = 1.85 V	T_A = 25°C		3	7	
			−40°C ≤ T_J ≤ 85°C (LMV712) or −40°C ≤ T_J ≤ 125°C (LMV712-Q1)			9	
I_B	Input bias current	LMV712	T_A = 25°C		5.5	115	pA
			−40°C ≤ T_J ≤ 85°C			130	
		LMV712-Q1	T_A = 25°C		5.5		
			−40°C ≤ T_J ≤ 125°C			3740	
CMRR	Common mode rejection ratio	0 V ≤ V_{CM} ≤ 2.7 V	T_A = 25°C	50	75		dB
			−40°C ≤ T_J ≤ 85°C (LMV712) or −40°C ≤ T_J ≤ 125°C (LMV712-Q1)	45			
PSRR	Power supply rejection ratio	2.7 V ≤ V^+ ≤ 5 V, V_{CM} = 0.85 V	T_A = 25°C	70	90		dB
			−40°C ≤ T_J ≤ 85°C (LMV712) or −40°C ≤ T_J ≤ 125°C (LMV712-Q1)	68			
		2.7 V ≤ V^+ ≤ 5 V, V_{CM} = 1.85 V	T_A = 25°C	70	90		
			−40°C ≤ T_J ≤ 85°C (LMV712) or −40°C ≤ T_J ≤ 125°C (LMV712-Q1)	68			
CMVR	Common mode voltage	For CMRR ≥ 50 dB	V-	−0.2	−0.3		V
			V+		3	2.9	
I_{SC}	Output short circuit current	Sourcing V_O = 0 V	T_A = 25°C	15	25		mA
			−40°C ≤ T_J ≤ 85°C (LMV712) or −40°C ≤ T_J ≤ 125°C (LMV712-Q1)	12			
		Sinking V_O = 2.7 V	T_A = 25°C	25	50		
			−40°C ≤ T_J ≤ 85°C (LMV712) or −40°C ≤ T_J ≤ 125°C (LMV712-Q1)	22			
V_O	Output swing	R_L = 10 kΩ to 1.35 V	T_A = 25°C	2.62	2.68		V
			−40°C ≤ T_J ≤ 85°C (LMV712) or −40°C ≤ T_J ≤ 125°C (LMV712-Q1)	2.6			
		T_A = 25°C			0.01	0.12	
		−40°C ≤ T_J ≤ 85°C (LMV712) or −40°C ≤ T_J ≤ 125°C (LMV712-Q1)				0.15	
		R_L = 600 Ω to 1.35 V	T_A = 25°C	2.52	2.55		
			−40°C ≤ T_J ≤ 85°C (LMV712) or −40°C ≤ T_J ≤ 125°C (LMV712-Q1)	2.5			
		T_A = 25°C			0.05	0.23	
		−40°C ≤ T_J ≤ 85°C (LMV712) or −40°C ≤ T_J ≤ 125°C (LMV712-Q1)				0.3	
V_O(SD)	Output voltage in shutdown				10	200	mV
I_S	Supply current per channel	On mode	T_A = 25°C		1.22	1.7	mA
			−40°C ≤ T_J ≤ 85°C (LMV712) or −40°C ≤ T_J ≤ 125°C (LMV712-Q1)			1.9	
		Shutdown mode	T_A = 25°C		0.12	1.5	µA
			−40°C ≤ T_J ≤ 85°C (LMV712) or −40°C ≤ T_J ≤ 125°C (LMV712-Q1)			2	

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

Electrical Characteristics – 2.7 V (continued)

All limits ensured for V^+ = 2.7 V, V^- = 0 V, V_{CM} = 1.35 V, T_A = 25°C, and R_L > 1 mΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN(1)	TYP(2)	MAX(1)	UNIT
A_{VOL}	Large signal voltage gain	LMV712 Sourcing R_L = 10 kΩ V_O = 1.35 V to 2.3 V	T_A = 25°C	80	115		dB
			−40°C ≤ T_J ≤ 85°C	76			
		LMV712-Q1	T_A = 25°C		115		
			−40°C ≤ T_J ≤ 125°C	69			
		LMV712 Sinking R_L = 10 kΩ V_O = 0.4 V to 1.35 V	T_A = 25°C	80	113		
			−40°C ≤ T_J ≤ 85°C	76			
		LMV712-Q1	T_A = 25°C		113		
			−40°C ≤ T_J ≤ 125°C	69			
		LMV712 Sourcing R_L = 600 Ω V_O = 1.35 V to 2.2 V	T_A = 25°C	80	97		
			−40°C ≤ T_J ≤ 85°C	76			
		LMV712-Q1	T_A = 25°C		97		
			−40°C ≤ T_J ≤ 125°C	64			
		LMV712 Sinking R_L = 600 Ω V_O = 0.5 V to 1.35 V	T_A = 25°C	80	100		
			−40°C ≤ T_J ≤ 85°C	76			
		LMV712-Q1	T_A = 25°C		100		
			−40°C ≤ T_J ≤ 125°C	62			
V_{SD}	Shutdown pin voltage	On mode		2.4	2.0		V
		Shutdown mode			1	0.8	
GBWP	Gain-bandwidth product				5		MHz
SR	Slew rate(3)				5		V/µs
φ_m	Phase margin				60		°
e_n	Input referred voltage noise	f = 1 kHz			20		nV/√Hz
T_{ON}	Turnon time from shutdown	T_A = 25°C			2.2	4	µs
		−40°C ≤ T_J ≤ 85°C (LMV712) or −40°C ≤ T_J ≤ 125°C (LMV712-Q1)				4.6	
	DSBGA turnon time from shutdown	T_A = 25°C		6			
		−40°C ≤ T_J ≤ 85°C (LMV712) or −40°C ≤ T_J ≤ 125°C (LMV712-Q1)		8			

(3) Number specified is the slower of the positive and negative slew rates.

6.6 Electrical Characteristics – 5 V

All limits ensured for V^+ = 5 V, V^- = 0 V, V_{CM} = 2.5 V, T_A = 25°C, and R_L > 1 mΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN(1)	TYP(2)	MAX(1)	UNIT
V_{OS}	Input offset voltage (WSON and VSSOP)	V_{CM} = 0.85 V and V_{CM} = 1.85 V	T_A = 25°C		0.4	3	mV
			−40°C ≤ T_J ≤ 85°C (LMV712) or −40°C ≤ T_J ≤ 125°C (LMV712-Q1)			3.2	
	Input offset voltage (DSBGA only)	V_{CM} = 0.85 V and V_{CM} = 1.85 V	T_A = 25°C		3	7	
			−40°C ≤ T_J ≤ 85°C (LMV712) or −40°C ≤ T_J ≤ 125°C (LMV712-Q1)			9	
I_B	Input bias current	LMV712	T_A = 25°C		5.5	115	pA
			−40°C ≤ T_J ≤ 85°C			130	
		LMV712-Q1	−40°C ≤ T_J ≤ 125°C			3600	
CMRR	Common mode rejection ratio	0 V ≤ V_{CM} ≤ 5 V	T_A = 25°C	50	80		dB
			−40°C ≤ T_J ≤ 85°C (LMV712) or −40°C ≤ T_J ≤ 125°C (LMV712-Q1)	45			
PSRR	Power supply rejection ratio	2.7 V ≤ V^+ ≤ 5 V, V_{CM} = 0.85 V	T_A = 25°C	70	90		dB
			−40°C ≤ T_J ≤ 85°C (LMV712) or −40°C ≤ T_J ≤ 125°C (LMV712-Q1)	68			
		2.7 V ≤ V^+ ≤ 5 V, V_{CM} = 1.85 V	T_A = 25°C	70	90		
			−40°C ≤ T_J ≤ 85°C (LMV712) or −40°C ≤ T_J ≤ 125°C (LMV712-Q1)	68			
CMVR	Common mode voltage	For CMRR ≥ 50 dB	V-	−0.2	−0.3		V
			V+		5.3	5.2	
I_{SC}	Output short circuit current	Sourcing V_O = 0 V	T_A = 25°C	20	35		mA
			−40°C ≤ T_J ≤ 85°C (LMV712) or −40°C ≤ T_J ≤ 125°C (LMV712-Q1)	18			
		Sinking V_O = 5 V	T_A = 25°C	25	50		
			−40°C ≤ T_J ≤ 85°C (LMV712) or −40°C ≤ T_J ≤ 125°C (LMV712-Q1)	21			
V_O	Output swing	R_L = 10 kΩ to 2.5 V	T_A = 25°C	4.92	4.98		V
			−40°C ≤ T_J ≤ 85°C (LMV712) or −40°C ≤ T_J ≤ 125°C (LMV712-Q1)	4.9			
		T_A = 25°C			0.01	0.12	
		−40°C ≤ T_J ≤ 85°C (LMV712) or −40°C ≤ T_J ≤ 125°C (LMV712-Q1)				0.15	
		R_L = 600 Ω to 2.5 V	T_A = 25°C	4.82	4.85		
			−40°C ≤ T_J ≤ 85°C (LMV712) or −40°C ≤ T_J ≤ 125°C (LMV712-Q1)	4.8			
		T_A = 25°C			0.05	0.23	
		−40°C ≤ T_J ≤ 85°C (LMV712) or −40°C ≤ T_J ≤ 125°C (LMV712-Q1)				0.3	
V_O(SD)	Output voltage in shutdown				10	200	mV
I_S	Supply current per channel	On mode	T_A = 25°C		1.17	1.7	mA
			−40°C ≤ T_J ≤ 85°C (LMV712) or −40°C ≤ T_J ≤ 125°C (LMV712-Q1)			1.9	
		Shutdown mode	T_A = 25°C		0.12	1.5	µA
			−40°C ≤ T_J ≤ 85°C (LMV712) or −40°C ≤ T_J ≤ 125°C (LMV712-Q1)			2	

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

Electrical Characteristics – 5 V (continued)

All limits ensured for V^+ = 5 V, V^- = 0 V, V_{CM} = 2.5 V, T_A = 25°C, and R_L > 1 mΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN(1)	TYP(2)	MAX(1)	UNIT
A_{VOL}	Large signal voltage gain	LMV712 Sourcing R_L = 10 kΩ V_O = 2.5 V to 4.6 V	T_A = 25°C	80	130		dB
			−40°C ≤ T_J ≤ 85°C	76			
		LMV712-Q1	T_A = 25°C		130		
			−40°C ≤ T_J ≤ 125°C	69			
		LMV712 Sinking R_L = 10 kΩ V_O = 0.4 V to 2.5 V	T_A = 25°C	80	130		
			−40°C ≤ T_J ≤ 85°C	76			
		LMV712-Q1	T_A = 25°C		130		
			−40°C ≤ T_J ≤ 125°C	69			
		LMV712 Sourcing R_L = 600 Ω V_O = 2.5 V to 4.6 V	T_A = 25°C	80	110		
			−40°C ≤ T_J ≤ 85°C	76			
		LMV712-Q1	T_A = 25°C		110		
			−40°C ≤ T_J ≤ 125°C	69			
		LMV712 Sinking R_L = 600 Ω V_O = 0.4 V to 2.5 V	T_A = 25°C	80	107		
			−40°C ≤ T_J ≤ 85°C	76			
		LMV712-Q1	T_A = 25°C		107		
			−40°C ≤ T_J ≤ 125°C	69			
V_{SD}	Shutdown pin voltage	On mode		4.5	3.5		V
		Shutdown mode			1.5	0.8	
GBWP	Gain-bandwidth product				5		MHz
SR	Slew rate(3)				5		V/µs
φ_m	Phase margin				60		°
e_n	Input referred voltage noise	f = 1 kHz			20		nV/√Hz
T_{ON}	Turnon time for shutdown	T_A = 25°C			1.6	4	µs
		−40°C ≤ T_J ≤ 85°C (LMV712) or −40°C ≤ T_J ≤ 125°C (LMV712-Q1)				4.6	
	DSBGA turnon time for shutdown	T_A = 25°C		6			
		−40°C ≤ T_J ≤ 85°C (LMV712) or −40°C ≤ T_J ≤ 125°C (LMV712-Q1)		8			

(3) Number specified is the slower of the positive and negative slew rates.

6.7 Typical Characteristics

T_A = 25°C, V_S = 5 V, and single supply (unless otherwise noted)

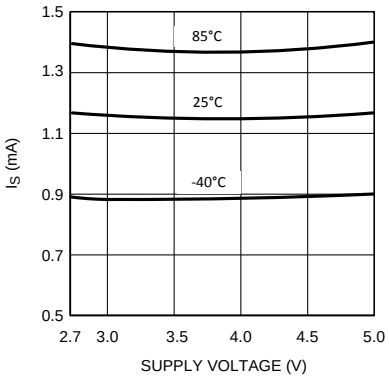


Figure 1. Supply Current Per Channel vs Supply Voltage

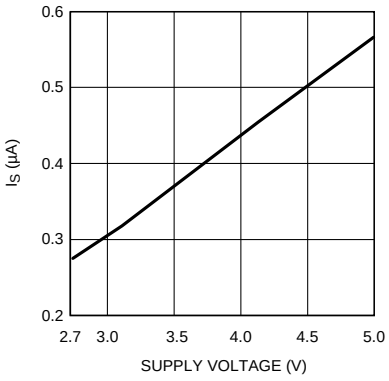


Figure 2. Supply Current vs Supply Voltage (Shutdown)

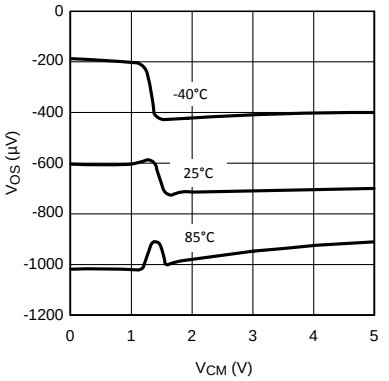


Figure 3. V_{OS} vs V_{CM}

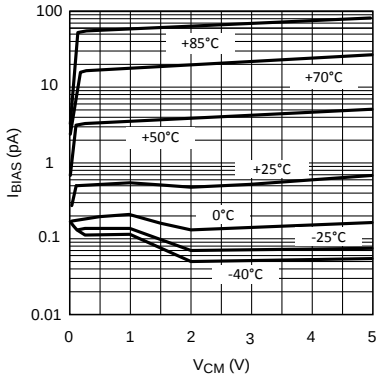
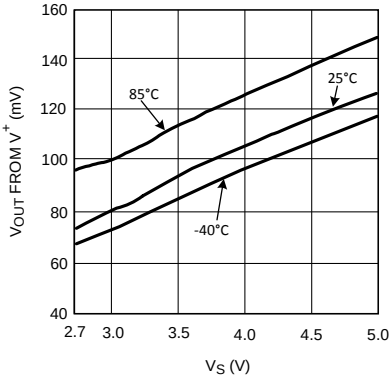
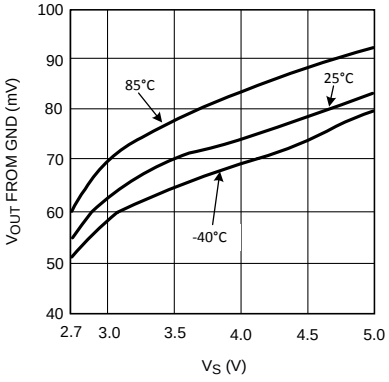


Figure 4. I_B vs V_{CM} Over Temperature



R_L = 600 Ω

Figure 5. Output Positive Swing vs Supply Voltage

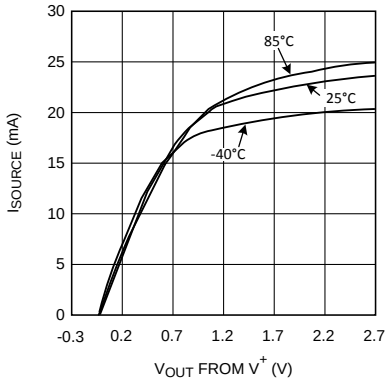


R_L = 600 Ω

Figure 6. Output Negative Swing vs Supply Voltage

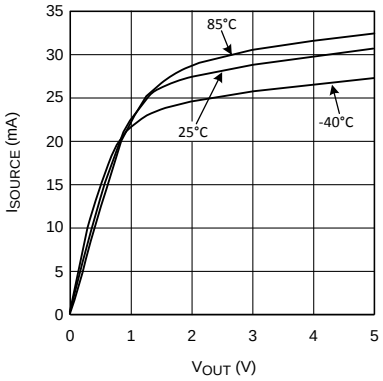
Typical Characteristics (continued)

T_A = 25°C, V_S = 5 V, and single supply (unless otherwise noted)



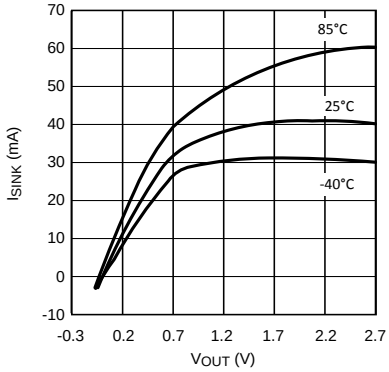
V_S = 2.7 V

Figure 7. Sourcing Current vs Output Voltage



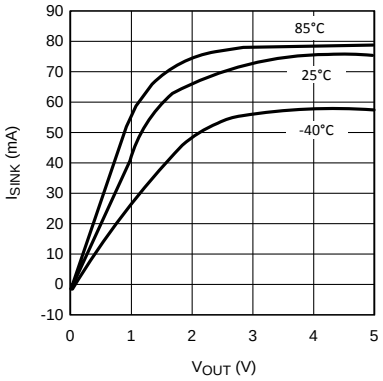
V_S = 5 V

Figure 8. Sourcing Current vs Output Voltage



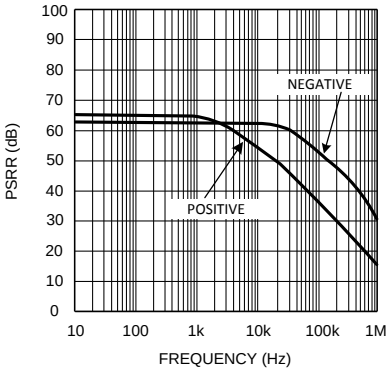
V_S = 2.7 V

Figure 9. Sinking Current vs Output Voltage



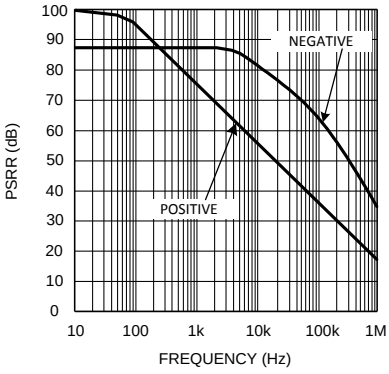
V_S = 5V

Figure 10. Sinking Current vs Output Voltage



V_S = 2.7 V

Figure 11. PSRR vs Frequency



V_S = 5 V

Figure 12. PSRR vs Frequency

Typical Characteristics (continued)

T_A = 25°C, V_S = 5 V, and single supply (unless otherwise noted)

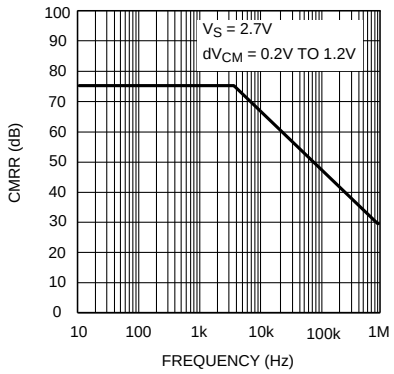


Figure 13. CMRR vs Frequency

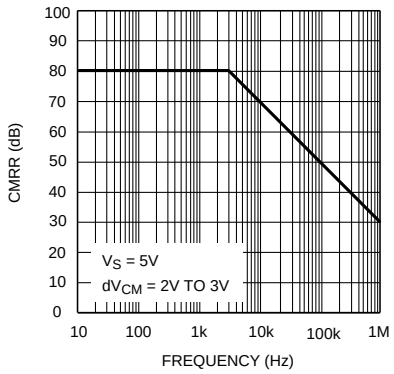


Figure 14. CMRR vs Frequency

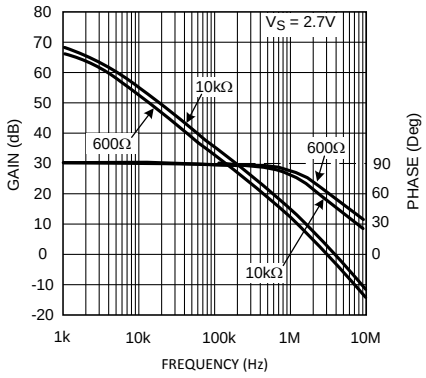


Figure 15. Open Loop Frequency Response vs R_L

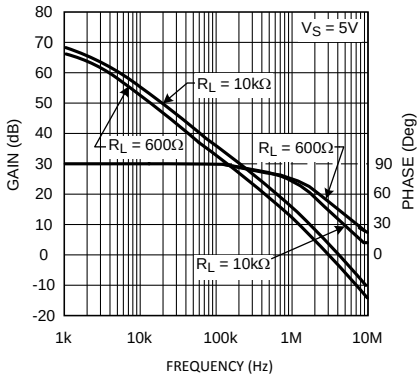


Figure 16. Open Loop Frequency Response vs R_L

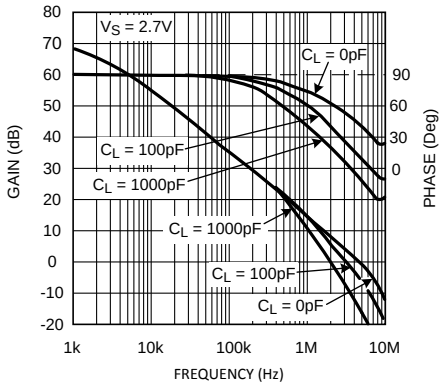


Figure 17. Open Loop Frequency Response vs C_L

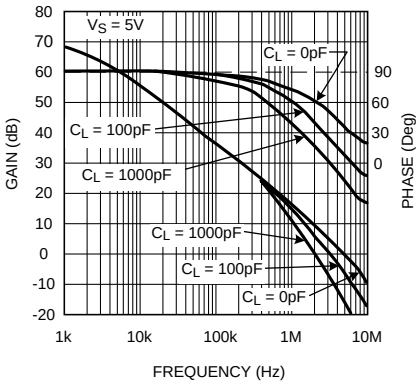


Figure 18. Open Loop Frequency Response vs C_L

Typical Characteristics (continued)

T_A = 25°C, V_S = 5 V, and single supply (unless otherwise noted)

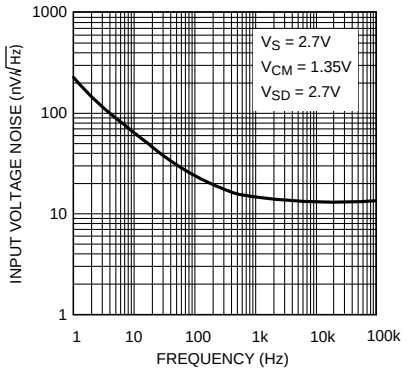


Figure 19. Voltage Noise vs Frequency

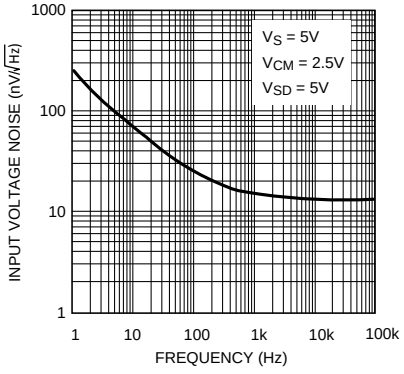
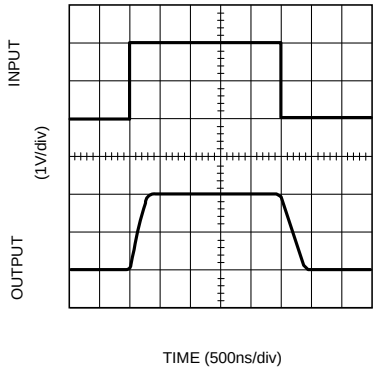
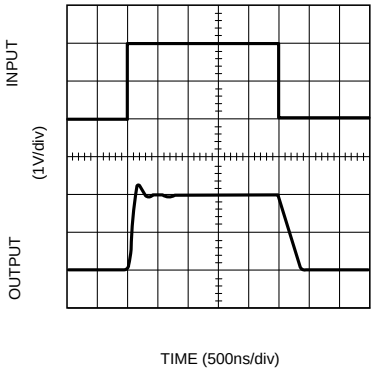


Figure 20. Voltage Noise vs Frequency



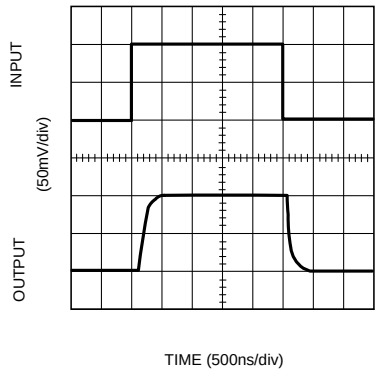
V_S = 2.7 V

Figure 21. Non-Inverting Large Signal Pulse Response



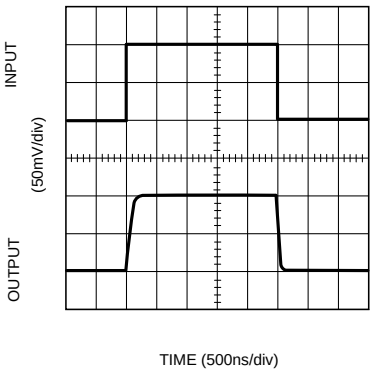
V_S = 5 V

Figure 22. Non-Inverting Large Signal Pulse Response



V_S = 2.7 V

Figure 23. Non-Inverting Small Signal Pulse Response

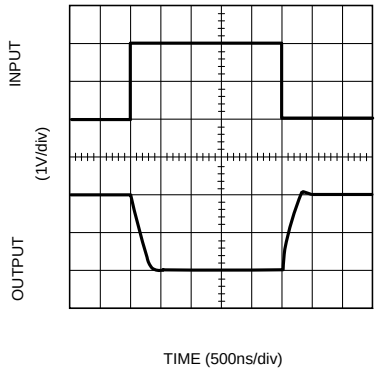


V_S = 5 V

Figure 24. Non-Inverting Small Signal Pulse Response

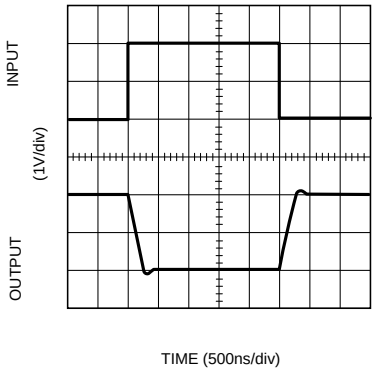
Typical Characteristics (continued)

T_A = 25°C, V_S = 5 V, and single supply (unless otherwise noted)



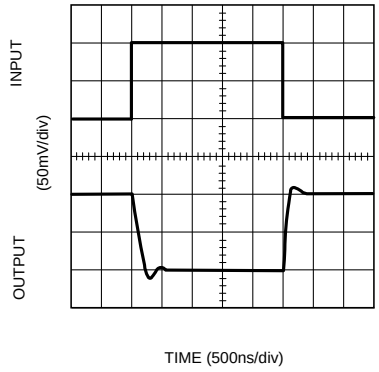
V_S = 2.7 V

Figure 25. Inverting Large Signal Pulse Response



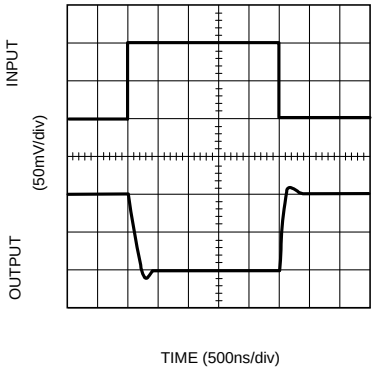
V_S = 5 V

Figure 26. Inverting Large Signal Pulse Response



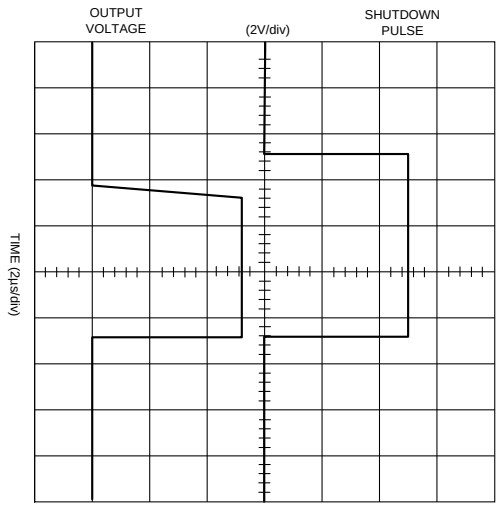
V_S = 2.7 V

Figure 27. Inverting Small Signal Pulse Response



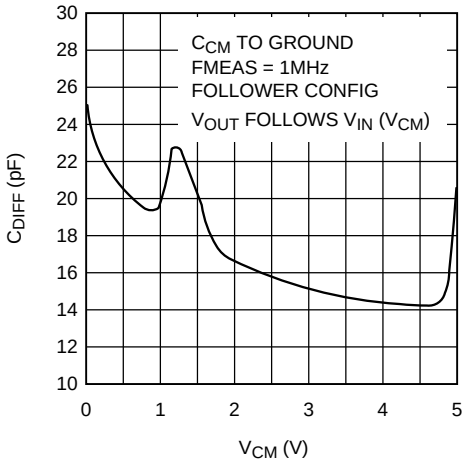
V_S = 5 V

Figure 28. Inverting Small Signal Pulse Response



V_S = 5 V

Figure 29. Turnon Time Response



V_S = 5 V

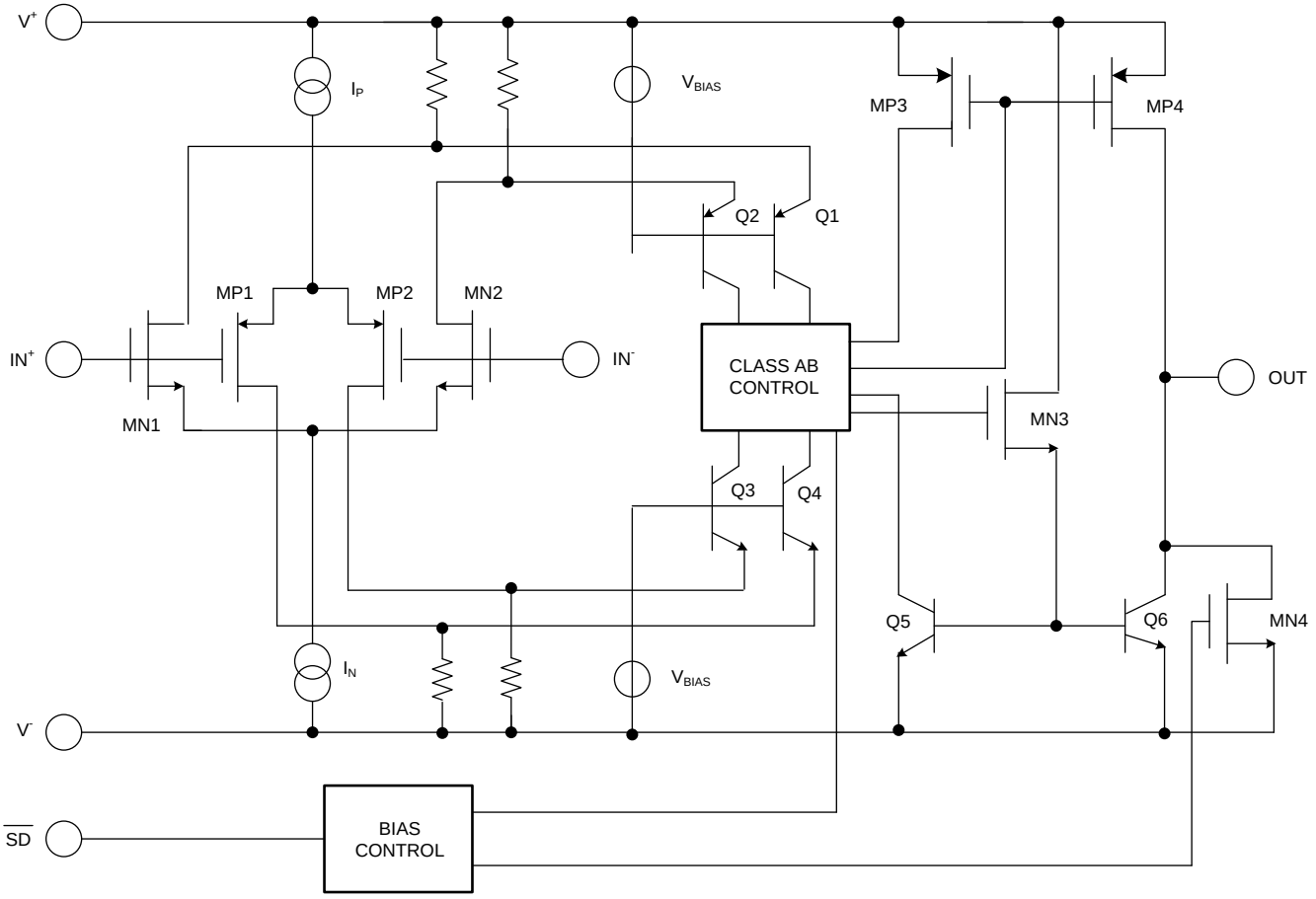
Figure 30. Input Common Mode Capacitance vs V_{CM}

7 Detailed Description

7.1 Overview

The LMV712-N features low voltage, low power, and rail-to-rail output operational amplifiers designed for low-voltage portable applications.

7.2 Functional Block Diagram



7.3 Feature Description

Rail-to-rail input is achieved by using in parallel, one NMOS differential pair (MN1 and MN2) and one PMOS differential pair (MP1 and MP2). When the common mode input voltage (V_{CM}) is near V^+, the NMOS pair is on and the PMOS pair is off. When V_{CM} is near V^-, the NMOS pair is off and the PMOS pair is on. When V_{CM} is between V^+ and V^-, internal logic decides how much current each differential pair receives. This special logic ensures stable and low distortion amplifier operation within the entire common mode voltage range.

Because both input stages have their own offset voltage (V_{OS}) characteristic, the offset voltage of the LMV712-N becomes a function of V_{CM}. V_{OS} has a crossover point at 1.4 V above V^- (see Figure 3). Caution must be taken in situations where input signal amplitude is comparable to V_{OS} value or the design requires high accuracy. In these situations, it is necessary for the input signal to avoid the crossover point.

The current coming out of the input differential pairs gets mirrored through two folded cascode stages (Q1, Q2, Q3, Q4) into the class AB control block. This circuitry generates voltage gain, defines the dominant pole of the op amp and limits the maximum current flowing at the output stage. MN3 introduces a voltage level shift and acts as a high impedance to low impedance buffer.

Feature Description (continued)

The output stage is composed of a PMOS and a NPN transistor in a common source or emitter configuration, delivering a rail-to-rail output excursion.

The MN4 transistor ensures that the LMV712-N output remains near V^- when the amplifier is in shutdown mode.

7.4 Device Functional Modes

7.4.1 Shutdown Pin

The LMV712-N offers independent shutdown pins for the dual amplifiers. When the shutdown pin is tied low, the respective amplifier shuts down and the supply current is reduced to less than 1 µA. In shutdown mode, the output level of the amplifier stays at V^-. In a 2.7-V operation, when a voltage from 1.5 V to 2.7 V is applied to the shutdown pin, the amplifier is enabled. As the amplifier is coming out of the shutdown mode, the output waveform ramps up without any glitch.

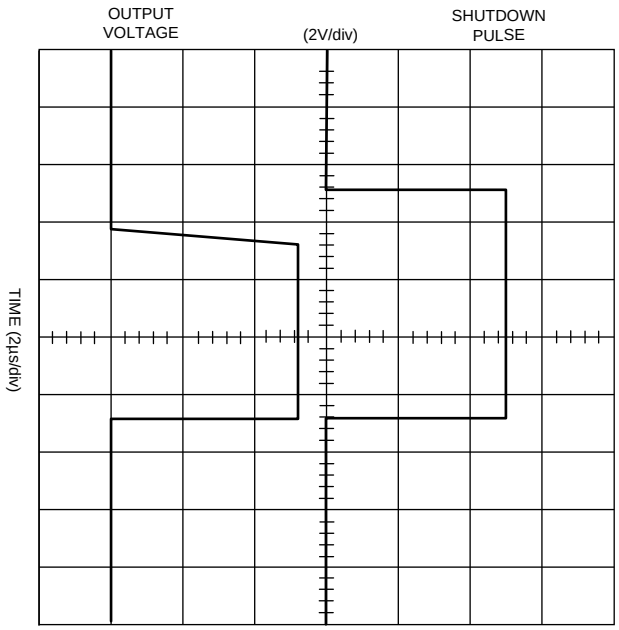


Figure 31. Output Recovery from Shutdown

A glitch-free output waveform is highly desirable in many applications, one of which is power amplifier control loops. In this application, the LMV712-N is used to drive the power amplifier's power control. If the LMV712-N did not have a smooth output ramp during turn on, it would directly cause the power amplifier to produce a glitch at its output. This adversely affects the performance of the system.

To enable the amplifier, the shutdown pin must be pulled high. It must not be left floating in the event that any leakage current may inadvertently turn off the amplifier.

7.4.2 Capacitive Load Tolerance

The LMV712-N can directly drive 200 pF in unity-gain without oscillation. The unity-gain follower is the most sensitive configuration to capacitive loading. Direct capacitive loading reduces the phase margin of amplifiers. The combination of the amplifier's output impedance and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation. To drive a heavier capacitive load, TI recommends the circuit in Figure 32.

Device Functional Modes (continued)

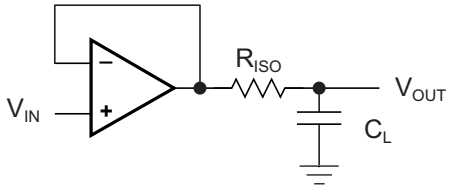


Figure 32. Driving Heavy Capacitive Loads

In Figure 32, the isolation resistor R_{ISO} and the load capacitor C_L form a pole to increase stability by adding more phase margin to the overall system. The desired performance depends on the value of R_{ISO}. The bigger the R_{ISO} resistor value, the more stable V_{OUT} is. But the DC accuracy is degraded when the R_{ISO} gets bigger. If there were a load resistor in the application, the output voltage would be divided by R_{ISO} and the load resistor.

Figure 33 is an improvement to the one in Figure 32 because it provides DC accuracy as well as AC stability. In Figure 33, R_F provides the DC accuracy by using feed-forward techniques to connect V_{IN} to R_L. C_F and R_{ISO} serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the inverting input of the amplifier, thereby preserving phase margin in the overall feedback loop. Increased capacitive drive is possible by increasing the value of C_F. This in turn slows down the pulse response.

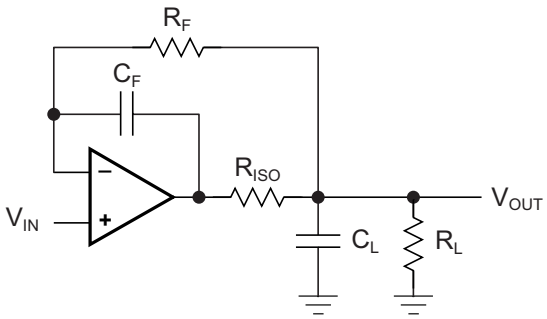


Figure 33. Enhanced DC Accuracy

7.4.3 Latchup

CMOS devices tend to be susceptible to latchup due to their internal parasitic SCR (silicon controlled rectifier) effects. The input and output pins look similar to the gate of the SCR. There is a minimum current required to trigger the SCR gate lead. The LMV712-N is designed to withstand 150-mA surge current on all the pins. Some resistive method must be used to isolate any capacitance from supplying excess current to the pins. In addition, like an SCR, there is a minimum holding current for any latchup mode. Limiting current to the supply pins also inhibits latchup susceptibility.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LMV712-N devices are dual op amps derived from the LMV711 single op amp. Figure 34 contains a simplified schematic of one channel of the LMV712-N.

8.2 Typical Applications

8.2.1 High-Side Current-Sensing

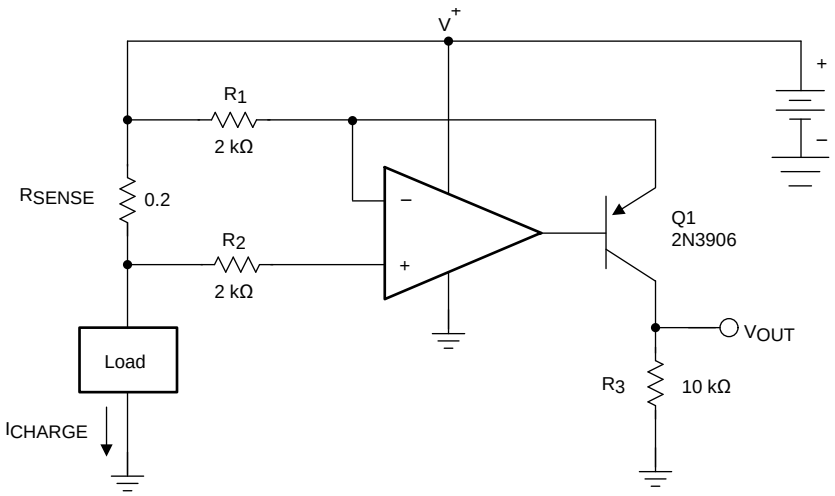


Figure 34. High-Side, Current-Sensing Schematic

8.2.1.1 Design Requirements

The high-side, current-sensing circuit (Figure 34) is commonly used in a battery charger to monitor charging current to prevent over charging. A sense resistor R_{SENSE} is connected to the battery directly. This system requires an op amp with rail-to-rail input. The LMV712-N is ideal for this application because its common-mode input range goes up to the rail.

8.2.1.2 Detailed Design Procedure

As seen in (Figure 34), the I_{CHARGE} current flowing through sense resistor R_{SENSE} develops a voltage drop equal to V_{SENSE}. The voltage at the negative sense point is now less than the positive sense point by an amount proportional to the V_{SENSE} voltage.

The low-bias currents of the LMV712-N causes little voltage drop through R_2, so the negative input of the LMV712-N amplifier is at essentially the same potential as the negative sense input.

The LMV712-N detects this voltage error between its inputs and servo the transistor base to conduct more current through Q1, increasing the voltage drop across R_1 until the LMV712-N inverting input matches the noninverting input. At this point, the voltage drop across R_1 now matches V_{SENSE}.

Typical Applications (continued)

I_G, a current proportional to I_{CHARGE}, flows according to Equation 1.

$$I_G = V_{RSENSE} / R_1 = (R_{SENSE} \times I_{CHARGE}) / R_1 \quad (1)$$

I_G also flows through the gain resistor R_3 developing a voltage drop equal to Equation 2.

$$V_3 = I_G \times R_3 = (V_{RSENSE} / R_1) \times R_3 = ((R_{SENSE} \times I_{CHARGE}) / R_2) \times R_3 \quad (2)$$

$$V_{OUT} = (R_{SENSE} \times I_{CHARGE}) \times G$$

where

- $G = R_3 / R_1$ (3)

The other channel of the LMV712-N may be used to buffer the voltage across R3 to drive the following stages.

8.2.1.3 Application Curve

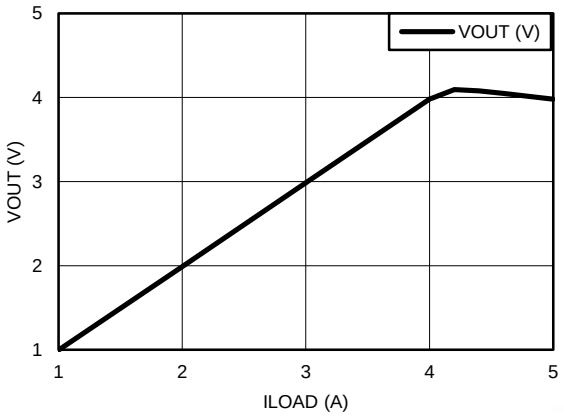


Figure 35. High-Side Current-Sensing Results

8.2.2 Peak Detector

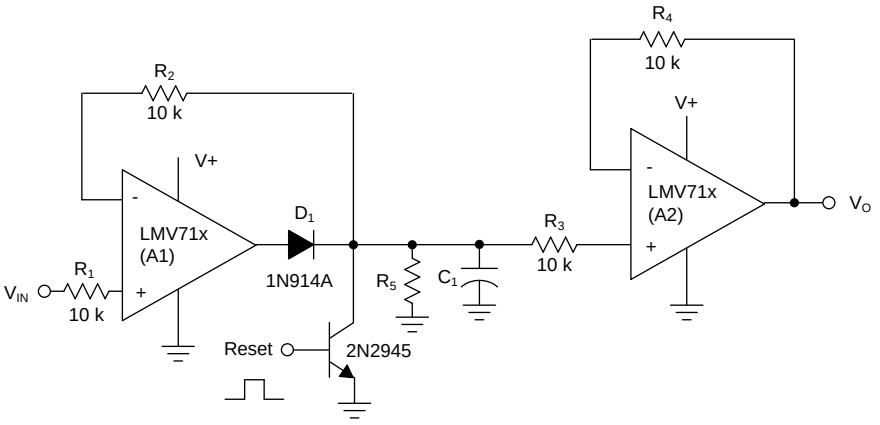


Figure 36. Peak Detector Schematic

8.2.2.1 Design Requirements

A peak detector outputs a DC voltage equal to the peak value of the applied AC signal. Peak detectors are used in many applications, such as test equipment, measurement instrumentation, ultrasonic alarm systems, and so forth. Figure 36 shows the schematic diagram of a peak detector using LMV712-N. This peak detector basically consists of a clipper, a parallel RC network, and a voltage follower.

Typical Applications (continued)

8.2.2.2 Detailed Design Procedure

An AC voltage source applied to V_{IN} charges capacitor C1 to the peak of the input. Diode D1 conducts positive *half cycles*, charging C1 to the waveform peak. Including D1 inside the feedback loop of the amplifier removes the voltage drop of D1 and allows an accurate peak detection of V_{IN} on C1. When the input waveform falls below the DC *peak* stored on C1, D1 is reverse biased. The low input bias current of A1 and the reverse biasing of D1 limits current leakage from C1. As a result, C1 retains the peak value even as the waveform drops to zero. A2 further isolates the peak value on C1 while completing the peak detector circuit by operating as a voltage follower and reporting the peak voltage of C1 at its output.

R5 and C1 are properly selected so that the capacitor is charged rapidly to V_{IN}. During the holding period, the capacitor slowly discharge through C1, through leakage of the capacitor and the reverse-biased diode, or op amp bias currents. In any cases the discharging time constant is much larger than the charge time constant. And the capacitor can hold its voltage long enough to minimize the output ripple.

Resistors R2 and R3 limit the current into the inverting input of A1 and the noninverting input of A2 when power is disconnected from the circuit. The discharging current from C1 during power off may damage the input circuitry of the op amps.

The peak detector is reset by applying a positive pulse to the reset transistor. The charge on the capacitor is dumped into ground, and the detector is ready for another cycle.

The maximum input voltage to this detector must be less than $(V^+ – V_D)$, where V_D is the forward voltage drop of the diode. Otherwise, the input voltage must be scaled down before applying to the circuit.

8.2.3 GSM Power Amplifier Control Loop

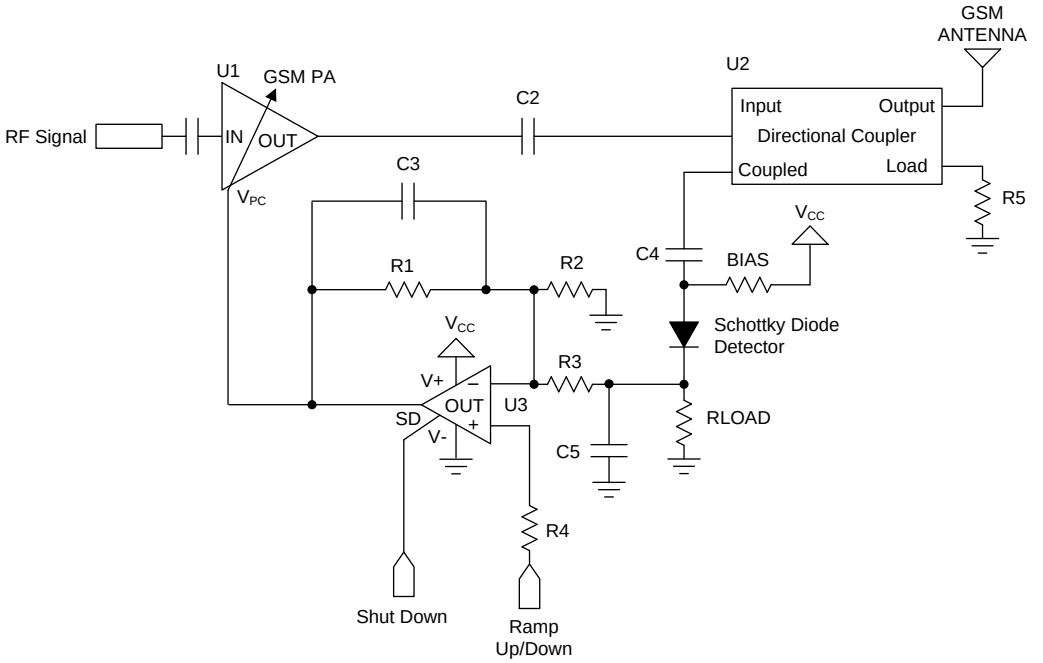


Figure 37. GSM Power Amplifier Control Loop Schematic

8.2.3.1 Design Requirements

The control loop in Figure 37 controls the output power level of a GSM mobile phones. The control loop is used to avoid intermodulation of base station receivers, to prevent intermodulation with other mobile phones, and to minimize power consumption depending on the distance between mobile and base station.

Typical Applications (continued)

8.2.3.2 Detailed Design Procedure

There are four critical sections in the GSM Power Amplifier Control Loop. The class-C R_F power amplifier provides amplification of the R_F signal. A directional coupler couples small amount of R_F energy from the output of the R_F P. A. to an envelope detector diode. The detector diode senses the signal level and rectifies it to a DC level to indicate the signal strength at the antenna. An op amp is used as an error amplifier to process the diode voltage and ramping voltage. This loop control the power amplifier gain through the op amp and forces the detector diode voltage and ramping voltage to be equal. Power control is accomplished by changing the ramping voltage.

The LMV712-N is well suited as an error amplifier in this application. The LMV712-N has an extra shutdown pin to switch the op amp to shutdown mode. In shutdown mode, the LMV712-N consumes very low current. Therefore, the power amplifier can be turned off to save battery life. The LMV712-N output is tri-stated when in shutdown.

9 Power Supply Recommendations

For proper operation, the power supplies must be properly decoupled. For decoupling the supply lines, TI recommends that 10-nF capacitors be placed as close as possible to the power supply pins of the operational amplifier. For single supply, place a capacitor between V^+ and V^- supply leads. For dual supplies, place one capacitor between V^+ and ground, and one capacitor between V^- and ground.

10 Layout

10.1 Layout Guidelines

To properly bypass the power supply, several locations on a printed circuit board must be considered. A 6.8 µF or greater tantalum capacitor must be placed at the point where the power supply for the amplifier is introduced onto the board. Another 0.1-µF ceramic capacitor must be placed as close as possible to the power supply pin of the amplifier. If the amplifier is operated in a single power supply, only the V^+ pin requires bypassing with a 0.1-µF capacitor. If the amplifier is operated in a dual power supply, both V^+ and V^- pins must be bypassed.

It is good practice to use a ground plane on a printed circuit board to provide all components with a low inductive ground connection.

Surface mount components in 0805 size or smaller are recommended in the LMV712-N application circuits. Designers can take advantage of the DSBGA, WSON, and VSSOP miniature sizes to condense board layout to save space and reduce stray capacitance.

10.2 Layout Example

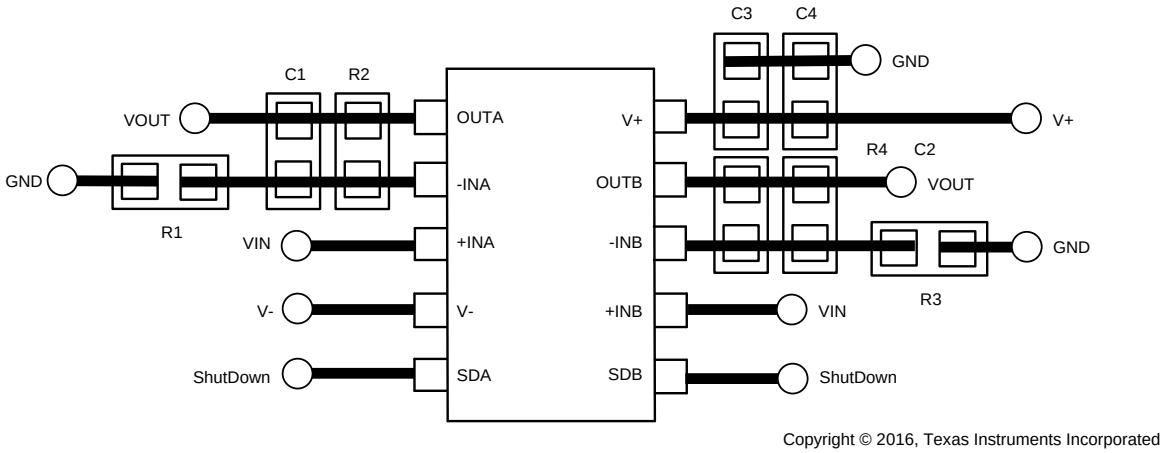


Figure 38. Sample Layout of VSSOP

11 Device and Documentation Support

11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LMV712-N	Click here	Click here	Click here	Click here	Click here
LMV712-N-Q1	Click here	Click here	Click here	Click here	Click here

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV712LD/NOPB	ACTIVE	WSON	NGY	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	A62	Samples
LMV712LDX/NOPB	ACTIVE	WSON	NGY	10	4500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	A62	Samples
LMV712MM	NRND	VSSOP	DGS	10	1000	TBD	Call TI	Call TI	-40 to 85	A61	
LMV712MM/NOPB	ACTIVE	VSSOP	DGS	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A61	Samples
LMV712MMX/NOPB	ACTIVE	VSSOP	DGS	10	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A61	Samples
LMV712Q1MM/NOPB	ACTIVE	VSSOP	DGS	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AUA	Samples
LMV712Q1MMX/NOPB	ACTIVE	VSSOP	DGS	10	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AUA	Samples
LMV712TL/NOPB	ACTIVE	DSBGA	YPA	10	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	AU2A	Samples
LMV712TLX/NOPB	ACTIVE	DSBGA	YPA	10	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	AU2A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF LMV712-N, LMV712-N-Q1 :

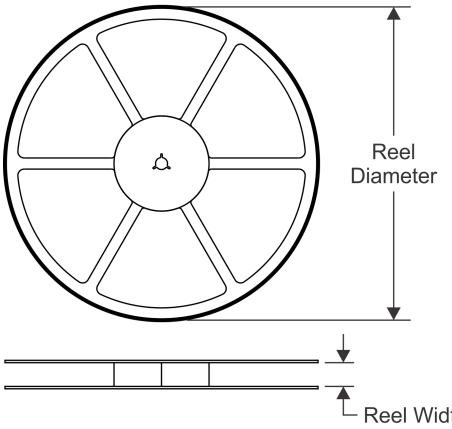
- Catalog: LMV712-N
- Automotive: LMV712-N-Q1

NOTE: Qualified Version Definitions:

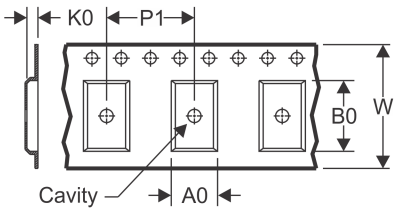
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

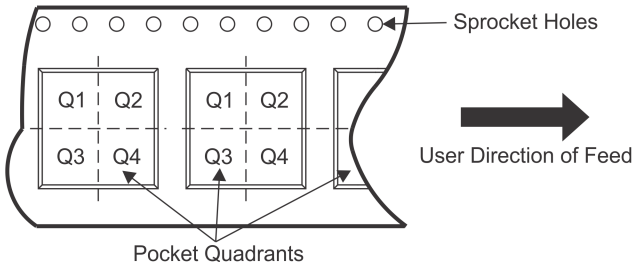


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

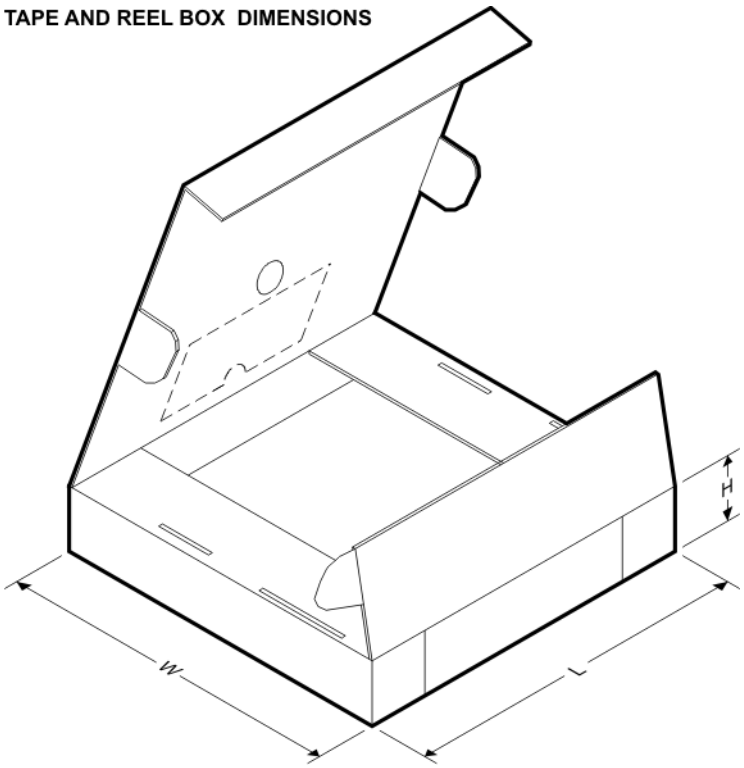
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV712LD/NOPB	WSON	NGY	10	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LMV712LDX/NOPB	WSON	NGY	10	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LMV712MM	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV712MM/NOPB	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV712MMX/NOPB	VSSOP	DGS	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV712Q1MM/NOPB	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV712Q1MMX/NOPB	VSSOP	DGS	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV712TL/NOPB	DSBGA	YPA	10	250	178.0	8.4	1.68	2.13	0.76	4.0	8.0	Q1
LMV712TLX/NOPB	DSBGA	YPA	10	3000	178.0	8.4	1.68	2.13	0.76	4.0	8.0	Q1

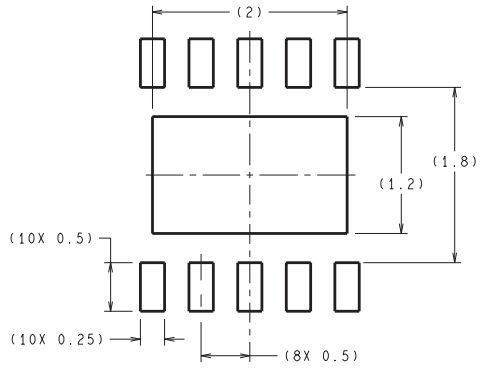
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

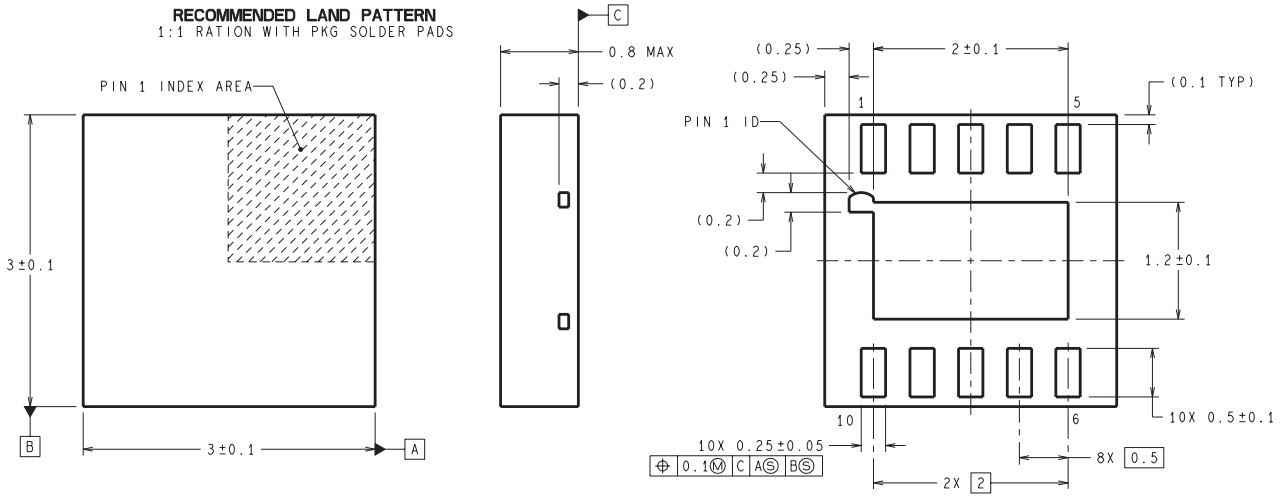
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV712LD/NOPB	WSON	NGY	10	1000	210.0	185.0	35.0
LMV712LDX/NOPB	WSON	NGY	10	4500	367.0	367.0	35.0
LMV712MM	VSSOP	DGS	10	1000	210.0	185.0	35.0
LMV712MM/NOPB	VSSOP	DGS	10	1000	210.0	185.0	35.0
LMV712MMX/NOPB	VSSOP	DGS	10	3500	367.0	367.0	35.0
LMV712Q1MM/NOPB	VSSOP	DGS	10	1000	210.0	185.0	35.0
LMV712Q1MMX/NOPB	VSSOP	DGS	10	3500	367.0	367.0	35.0
LMV712TL/NOPB	DSBGA	YPA	10	250	210.0	185.0	35.0
LMV712TLX/NOPB	DSBGA	YPA	10	3000	210.0	185.0	35.0

NGY0010A



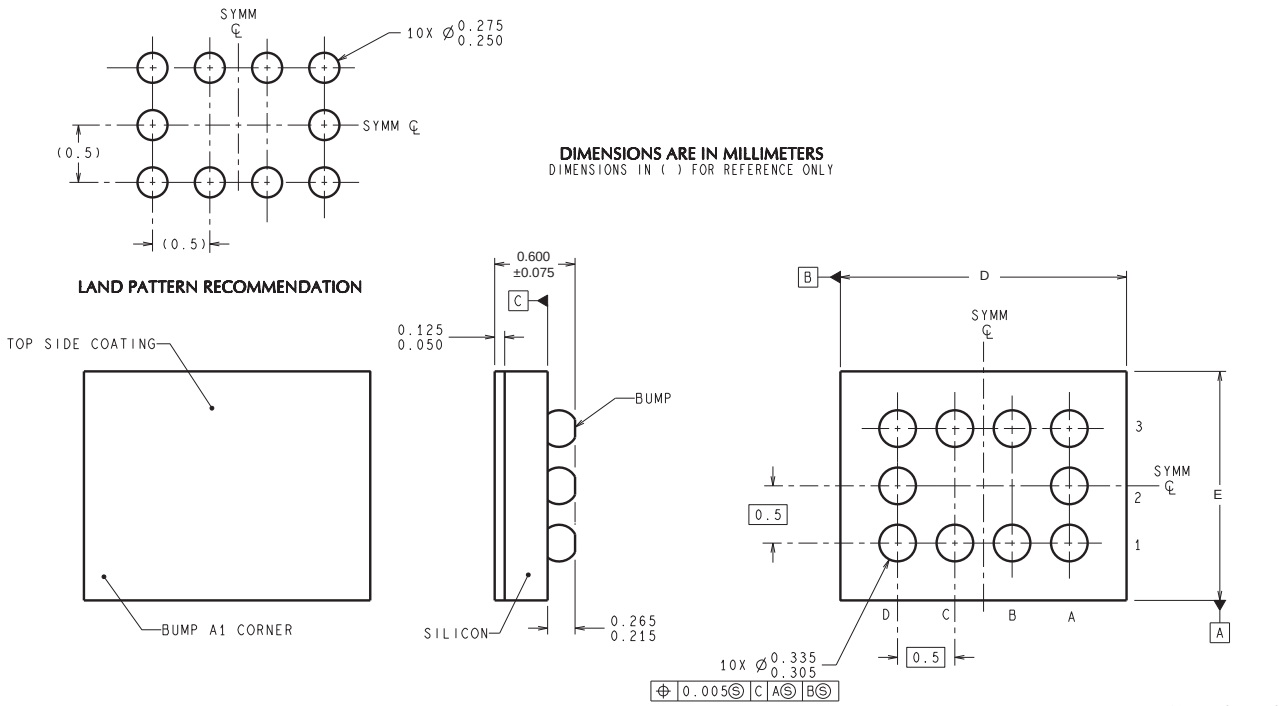
RECOMMENDED LAND PATTERN
1:1 RATION WITH PKG SOLDER PADS

DIMENSIONS ARE IN MILLIMETERS



LDA10A (Rev B)

YPA0010



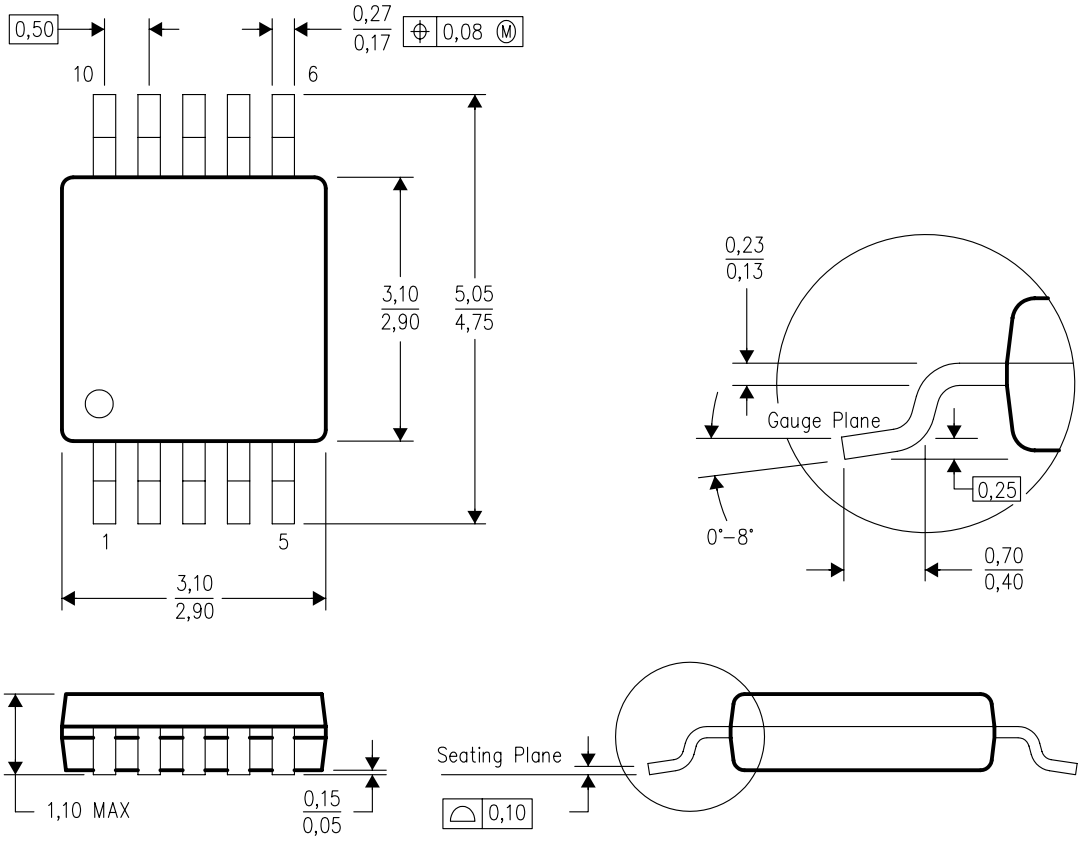
D: Max = 2.048 mm, Min =1.987 mm

E: Max = 1.565 mm, Min =1.504 mm

4215069/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

DGS (S–PDSO–G10) PLASTIC SMALL–OUTLINE PACKAGE



4073272/C 02/04

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation BA.

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