OPAx363、OPAx364 1.8V 7MHz 90dB CMRR 单电源轨至轨 I/O 运算放大器

1 特性

- 1.8V 运行电压
- 微型 封装
- 带宽： 7MHz
- CMRR：90dB（典型）
- 压摆率：5V/μs
- 低失调电压：500μV（最大值）
- 静态电流：每个通道750μA（最大值）
- 关断模式：每个通道小于 1μA

2 应用

- 信号调节
- 数据采集
- 过程控制
- 有源滤波器
- 测试设备

3 说明

OPA363 和 OPA364 系列是两款高性能 CMOS 运算放大器，针对超低电压单电源运行进行优化。这些微型低成本放大器设计用于在介于 1.8V (±0.9 V) 到 5.5V (±2.75V) 之间的单电源上运行。应用 包括在电池供电系统中的传感器放大和信号调节。

OPAx363 和 OPA364 系列提供出色的 CMRR，而不存在与传统互补输入级关联的交叉。此特性可在驱动模数 (A/D) 转换器方面实现优异的性能，而不会降低微分线性和 THD。输入共模范围同时包括正负电源。电源轨的输出电压摆幅在 10mV 以内。

OPA363 系列包括关断模式。在逻辑控制下，这些放大器可从正常运行状态切换到待机电流小于 1μA 的状态。

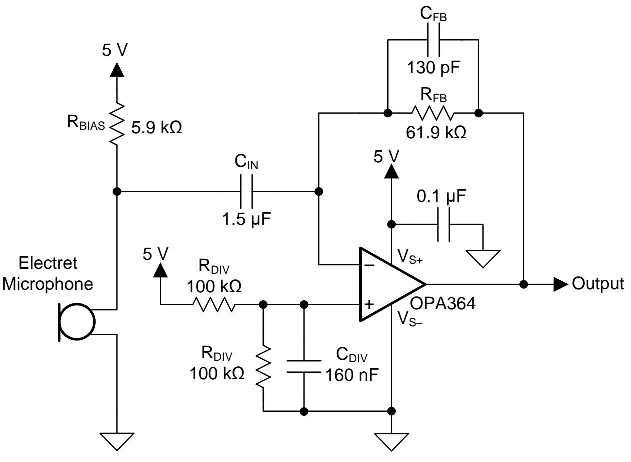
单通道版本采用微型 5 引脚 SOT-23（6 引脚 SOT-23 用于关断模式）和 8 引脚 SOIC。双通道版本采用 8 引脚 VSSOP、10 引脚 VSSOP、16 引脚 UQFN 和 8 引脚 SOIC 封装。这四种封装都可应用 14 引脚 TSSOP 和 14 引脚 SOIC 封装。所有器件版本的额定工作温度范围均为 –40°C 至 +125°C。

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA363	SOT-23 (5)	2.60mm × 1.60mm
OPA364	SOT-23 (6)	2.60mm × 1.60mm
	SOIC (8)	4.90mm x 3.91mm
OPA2363、OPA2364	SOIC (8)	4.90mm x 3.91mm
	VSSOP (8)	3.00mm × 3.00mm
	VSSOP (10)	3.00mm × 3.00mm
	UQFN (16)	2.60mm x 1.80mm
OPA4364	SOIC (14)	8.65mm x 3.91mm
	TSSOP封装(14)	5.00 mm × 4.40 mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

单电源麦克风前置放大器



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision D (September 2016) to Revision E	Page
• 已更改 将*器件信息*表中的 OPA36x 和 OPA236x 部件编号更改为 OPA364 和 OPA2363	1
• 已添加 在*器件信息*表中增加了 OPA2364 器件	1
• Corrected formatting of pinout drawings in *Pin Configuration and Functions* section	4
• Corrected formatting of pinout tables in *Pin Configuration and Functions* section	4
• Added a minimum value of 0 V to supply voltage parameter in *Absolute Maximum Ratings* table	8
• Added "([V+] – [V–])" to supply voltage parameter in *Absolute Maximum Ratings* table	8
• Deleted operating temperature range from *Absolute Maximum Ratings* table	8
• Added the word "temperature" to junction and storage temperature ranges in *Absolute Maximum Ratings* table	8
• Added "([V+] – [V–])" to supply voltage parameter in *Recommended Operating Conditions* table	8
• Changed output voltage swing parameter units from V to mV	11
• Deleted temperature range section of *Electrical Characteristics* table	11
• Changed PSRR test condition from V_{CM} = 0 to V_{CM} = (V–) in *Electrical Characteristics* table	11
• Deleted *Buffered Reference Voltage* subsection in *Application Information* section	20
• Changed Figure 33	26
• Added Figure 34	27
• 已更改 在整个产品说明书中将“IC”更改为“器件”	28

Changes from Revision C (May 2013) to Revision D	Page
• 已添加 *增加了 ESD 额定值表、特性 说明 部分、器件功能模式、应用和实施部分、电源建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分*	1
• 已删除 *删除了封装和订购信息部分。请参阅产品说明书末尾的 POA。*	1

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Changes from Revision B (February 2003) to Revision C **Page**

- 将产品说明书转换为当前格式 1
- 已添加 在产品说明书中增加了 RSV 封装 (UQFN-16) 1
- Added text to last bullet of *Layout Guidelines* section........ 26

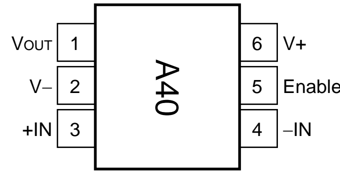
5 Device Comparison Table

5.1 Device Comparison Table

	OPA363	OPA364	OPA2363	OPA2364	OPA4364
SOT-23-5		X			
SOT-23-6 (shutdown)	X				
MSOP-8				X	
MSOP-10			X		
SO-8	X	X		X	
TSSOP-14					X
SO-14					X
UQFN-16			X		

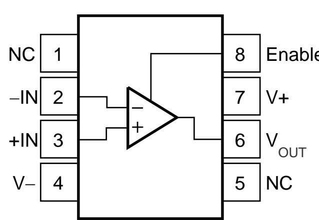
6 Pin Configuration and Functions

OPA363: DBV Package
6-Pin SOT-23
Top View



(1) Orient according to marking.

OPA363: D Package
8-Pin SOIC
Top View



NC- no internal connection

Pin Functions: OPA363

PIN			I/O	DESCRIPTION
NAME	SOIC	SOT-23		
Enable	8	5	I	Enable
–IN	2	4	I	Negative (inverting) input
+IN	3	3	I	Positive (noninverting) input
NC	1, 5	—	—	No internal connection (can be left floating)
V_{OUT}	6	1	O	Output
V–	4	2	—	Negative (lowest) power supply
V+	7	6	—	Positive (highest) power supply

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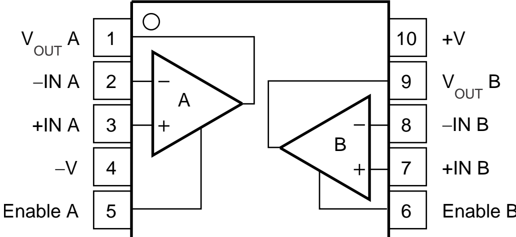
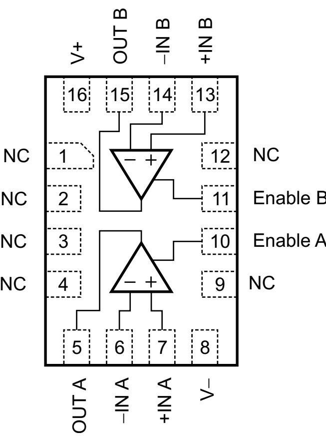
OPA2363: DGS Package
10-Pin MSOP
Top View



OPA2363: RSV Package
16-Pin UQFN
Top View

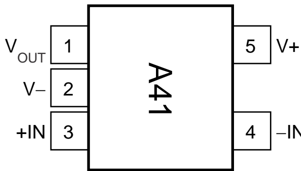


NC- no internal connection

Pin Functions: OPA2363

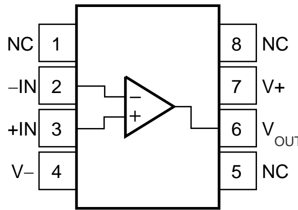
PIN			I/O	DESCRIPTION
NAME	MSOP	UQFN		
Enable A	5	10	I	Enable A amplifier
Enable B	6	11	I	Enable B amplifier
–IN A	2	6	I	Inverting input, channel A
+IN A	3	7	I	Noninverting input, channel A
–IN B	8	14	I	Inverting input, channel B
+IN B	7	13	I	Noninverting input, channel B
NC	—	1, 2, 3, 4, 9, 12	—	No internal connection (can be left floating)
OUT A	—	5	O	Output, channel A
OUT B	—	15	O	Output, channel B
V_{OUT} A	1	—	O	Output, channel A
V_{OUT} B	9	—	O	Output, channel B
–V, V–	4	8	—	Negative (lowest) power supply
+V, V+	10	16	—	Positive (highest) power supply

OPA364: DBV Package
5-Pin SOT-23
Top View



(1) Orient according to marking.

OPA364: D Package
8-Pin SOIC
Top View

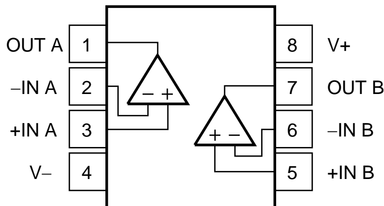


NC - no internal connection

Pin Functions: OPA364

PIN			I/O	DESCRIPTION
NAME	SOIC	SOT-23		
–IN	2	4	I	Negative (inverting) input
+IN	3	3	I	Positive (noninverting) input
NC	1, 5, 8	—	—	No internal connection (can be left floating)
V_{OUT}	6	1	O	Output
V–	4	2	—	Negative (lowest) power supply
V+	7	5	—	Positive (highest) power supply

OPA2364: DGK and D Packages
8-Pin MSOP and SOIC
Top View



Pin Functions: OPA2364

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
–IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V–	4	—	Negative (lowest) power supply
V+	8	—	Positive (highest) power supply

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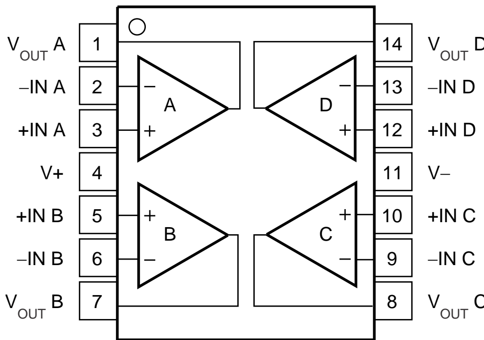
OPA4364: D and PW Packages
14-Pin SOIC and TSSOP
Top View



NC- no internal connection.

Pin Functions: OPA4364

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
–IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
–IN C	9	I	Inverting input, channel C
+IN C	10	I	Noninverting input, channel C
–IN D	13	I	Inverting input, channel D
+IN D	12	I	Noninverting input, channel D
V_{OUT} A	1	O	Output, channel A
V_{OUT} B	7	O	Output, channel B
V_{OUT} C	8	O	Output, channel C
V_{OUT} D	14	O	Output, channel D
V–	11	—	Negative (lowest) power supply
V+	4	—	Positive (highest) power supply

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7 Specifications

!~

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Supply ([V+] – [V–])	0	5.5	V
	Signal input pin(2)	−0.5	(V+) + 0.5	
Current	Signal input pin(2)	–10	10	mA
	Output short-circuit(3)	Continuous		mA
Junction!~ temperature, T_J			150	°C
Storage!~ temperature, T_{stg}		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
	Supply voltage ([V+] – [V–])	1.8		5.5	V
T_A	Operating temperature	–40		125	°C

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7.4 Thermal Information: OPA363

THERMAL METRIC(1)		OPA363 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	211.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	137	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	39.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	20.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	38.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Thermal Information: OPA364

THERMAL METRIC(1)		OPA364		UNIT
		DBV (SOT-23)	D (SOIC)	
		6 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	182.7	125.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	130.7	73.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	34.1	65.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	24.8	25.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	33.5	65.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.6 Thermal Information: OPA2363

THERMAL METRIC[(1)]		OPA2363				UNIT
		D (SOIC)	DGK (VSSOP)	DGS (VSSOP)	UQFN (RSV)	
		8 PINS	8 PINS	10 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	125.3	171.8	166.4	112.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	73.7	63.2	55.9	44	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	65.7	92.4	86.6	41.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	25.4	9.5	6.8	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	65.2	91	85.2	41.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.7 Thermal Information: OPA2364

THERMAL METRIC[(1)]		OPA2364				UNIT
		D (SOIC)	DGK (VSSOP)	DGS (VSSOP)	UQFN (RSV)	
		8 PINS	8 PINS	10 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	125.3	171.8	166.4	112.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	73.7	63.2	55.9	44	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	65.7	92.4	86.6	41.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	25.4	9.5	6.8	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	65.2	91	85.2	41.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.8 Thermal Information: OPA4364

THERMAL METRIC[(1)]		OPA4364		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	82.6	107.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	41.1	31.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.1	50.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.4	1.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	36.8	49.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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7.9 Electrical Characteristics

at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{OUT} = V_S / 2, and V_{CM} = V_S / 2, V_S = 1.8 V to 5.5 V, (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_S = 5 V (OPA363I, OPA364I)				500	µV
		OPA2363I, OPA2364I				900	µV
		OPA363AI, OPA364AI, OPA2363AI, OPA2364AI, OPA4364AI			1	2.5	mV
dV_{OS}/dT	Drift	T_A = –40°C to +125°C			3		µV/°C
PSRR	Input offset voltage vs power supply	V_S = 1.8 V to 5.5 V V_{CM} = (V–) T_A = –40°C to +125°C			80	330	µV/V
	Channel separation, DC				1		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current	T_A = 25°C			±1	±10	pA
		T_A = –40°C to +125°C		See *Typical Characteristics*			
I_{OS}	Input offset current				±1	±10	pA
NOISE							
e_n	Input voltage noise,	f = 0.1 Hz to 10 Hz			10		$µV_{PP}$
e_n	Input voltage noise density	f = 10 kHz			17		nV/√Hz
i_n	Input current noise density	f = 10 kHz			0.6		fA/√Hz
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range			(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	(V–) – 0.1 V < V_{CM} < (V+) + 0.1 V T_A = –40°C to +125°C		74	90		dB
INPUT CAPACITANCE							
	Differential				2		pF
	Common-mode				3		pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	R_L = 10 kΩ 100 mV < V_O < (V+) – 100 mV	T_A = 25°C	94	100		dB
			T_A = 25°C (OPA4364)	90			dB
		R_L = 10 kΩ 100 mV < V_O < (V+) – 100 mV	V_S = 1.8 V to 5.5 V T_A = –40°C to +125°C	86			dB
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product	C_L = 100 pF			7		MHz
SR	Slew rate	C_L = 100 pF, G = 1			5		V/µs
t_S	Settling time	0.1%, C_L = 100 pF, V_S = 5 V, 4-V step, G = 1			1		µs
		0.01%, C_L = 100 pF, V_S = 5 V, 4-V step, G = 1			1.5		µs
	Overload recovery time	C_L = 100 pF V_{IN} × Gain > V_S			0.8		µs
THD+N	Total harmonic distortion + noise	C_L = 100 pF, V_S = 5 V, G = 1, f = 20 Hz to 20 kHz			0.002%		
OUTPUT							
	Voltage output swing	R_L = 10 kΩ, T_A = 25°C			10	20	mV
		R_L = 10 kΩ T_A = –40°C to +125°C				20	mV
I_{SC}	Short-circuit current			See *Typical Characteristics*			
C_{LOAD}	Capacitive load drive			See *Typical Characteristics*			
SHUTDOWN (OPA363)							
t_{OFF}	Turnoff time				1		µs
t_{ON}	Turnon time (1)				20		µs
V_L	Logic low threshold	Shutdown				(V–) + 0.8	V
V_H	Logic high threshold	Amplifier is active		0.75 (V+)		5.5	V
$I_{Q(sd)}$	Quiescent current at shutdown (per amplifier)					0.9	µA

(1) Part is considered enabled when input offset voltage returns to specified range.

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Electrical Characteristics (continued)

at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{OUT} = V_S / 2, and V_{CM} = V_S / 2, V_S = 1.8 V to 5.5 V, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_S	Specified voltage range		1.8		5.5	V
I_Q	Quiescent current (per amplifier)	V_S = 1.8 V T_A = –40°C to +125°C		650	750	µA
		V_S = 3.6 V T_A = –40°C to +125°C		850	1000	µA
		V_S = 5.5 V T_A = –40°C to +125°C		1.1	1.4	mA

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7.10 Typical Characteristics

at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{OUT} = V_S / 2, and V_{CM} = V_S / 2, (unless otherwise noted)

Voltage Gain (dB)
Phase (°)
Frequency (Hz)

Figure 1. Open-Loop Gain and Phase vs Frequency

CMRR (dB)
Frequency (Hz)

Figure 2. Common-Mode Rejection Ratio vs Frequency

PSRR (dB)
Frequency (Hz)

Figure 3. Power-Supply Rejection Ratio vs Frequency

Per Amplifier
Quiescent Current (mA)
Supply Voltage (V)

Figure 4. Quiescent Current vs Supply Voltage

V_{OUT} = –10dBv
G = 10, R_L = 2kΩ, V_S = 5V
G = 10, R_L = 2kΩ, V_S = 1.8V
G = 10, R_L = 10kΩ, V_S = 1.8V, 5V
G = 1, R_L = 2kΩ, V_S = 1.8V
G = 1, R_L = 2kΩ, V_S = 5V
G = 1, R_L = 10kΩ, V_S = 1.8V, 5V
THD+N (%)
Frequency (Hz)

Figure 5. Total Harmonic Distortion + Noise Ratio vs Frequency

(V_S = 5V, V_{OUT} = 1Vrms)
G = 10, R_L = 2kΩ
G = 10, R_L = 10kΩ
G = 1, R_L = 2kΩ
G = 1, R_L = 10kΩ
THD+N (%)
Frequency (Hz)

Figure 6. Total Harmonic Distortion + Noise Ratio vs Frequency

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Typical Characteristics (continued)

at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{OUT} = V_S / 2, and V_{CM} = V_S / 2, (unless otherwise noted)

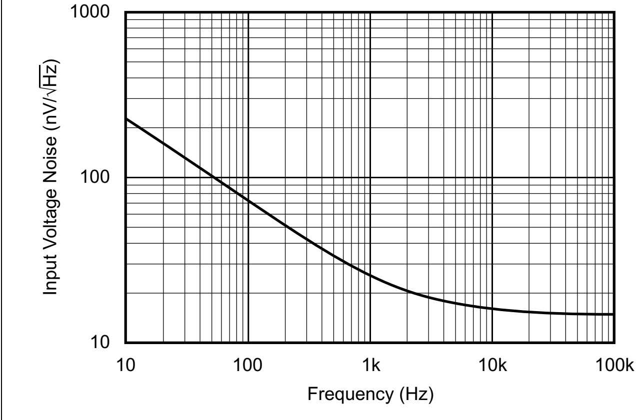

Figure 7. Input Voltage Noise Spectral Density vs Frequency

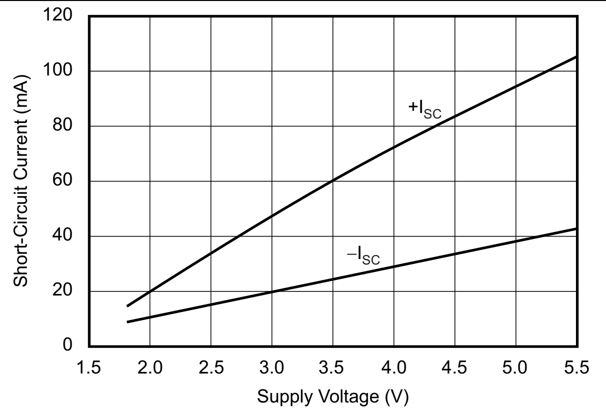

Figure 8. Short-Circuit Current vs Supply Voltage

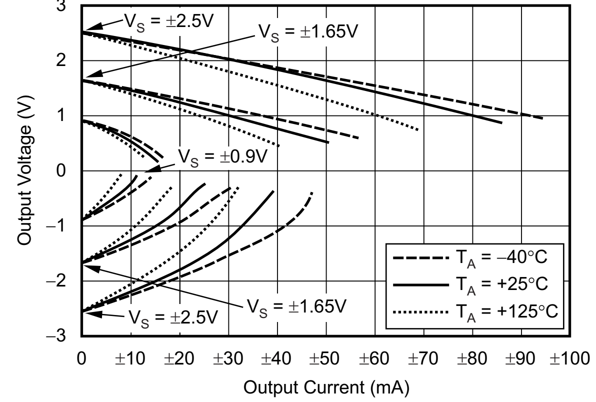

Figure 9. Output Voltage Swing vs Output Current

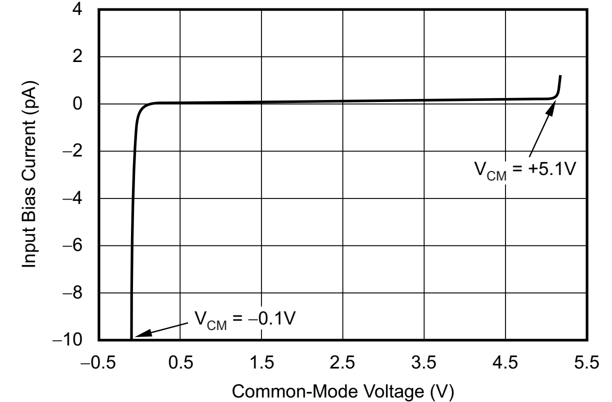

Figure 10. Input Bias Current vs Input Common-Mode Voltage

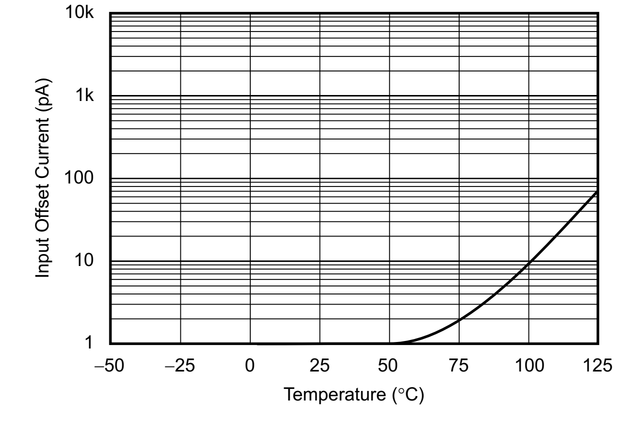

Figure 11. Input Offset Current vs Temperature

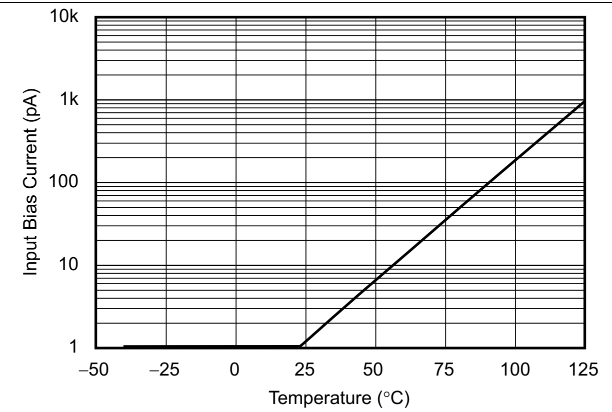

Figure 12. Input Bias Current vs Temperature

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Typical Characteristics (continued)

at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{OUT} = V_S / 2, and V_{CM} = V_S / 2, (unless otherwise noted)

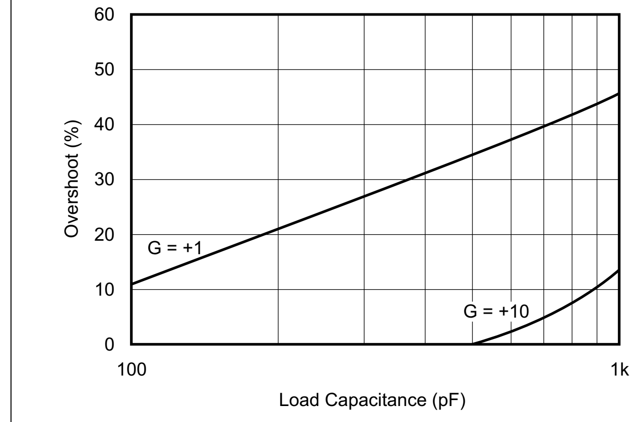


Figure 13. Small-Signal Overshoot vs Load Capacitance

Settling Time (μs)
100
10
1
0.1
0.01%
0.1%
1
10
100
Closed-Loop Gain (V/V)

Figure 14. Settling Time vs Closed-Loop Gain

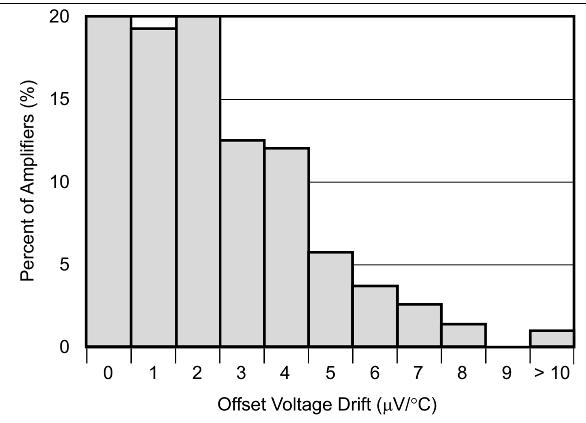


Figure 15. Offset Drift Distribution

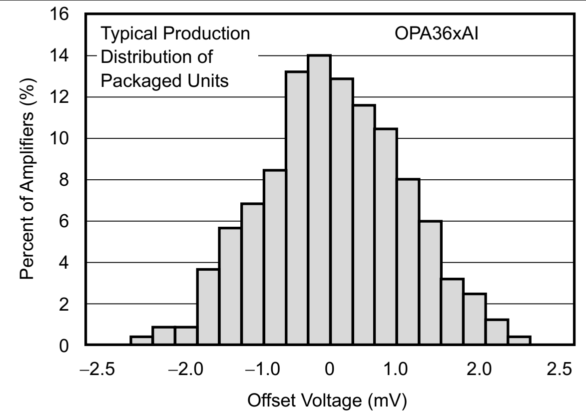


Figure 16. Offset Voltage Production Distribution

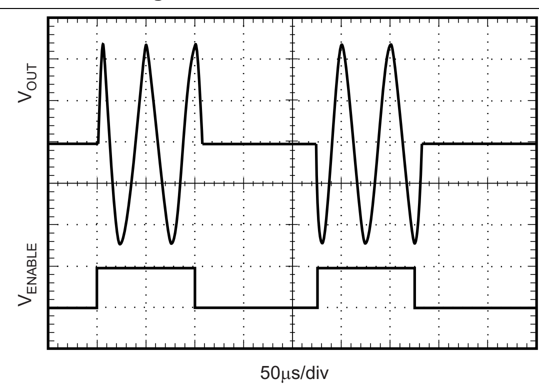


Figure 17. Output Enable Characteristic (V_S = 5 V, V_{OUT} = 20-kHz Sinusoid)

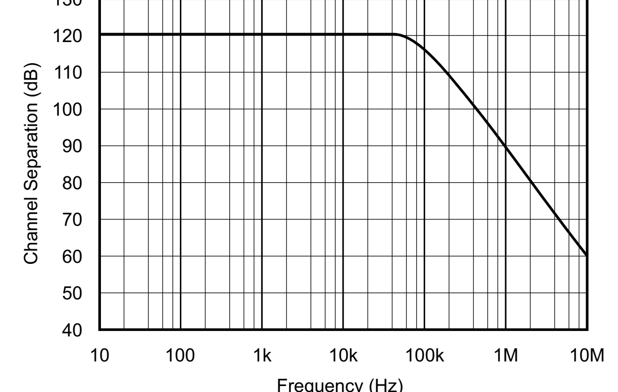
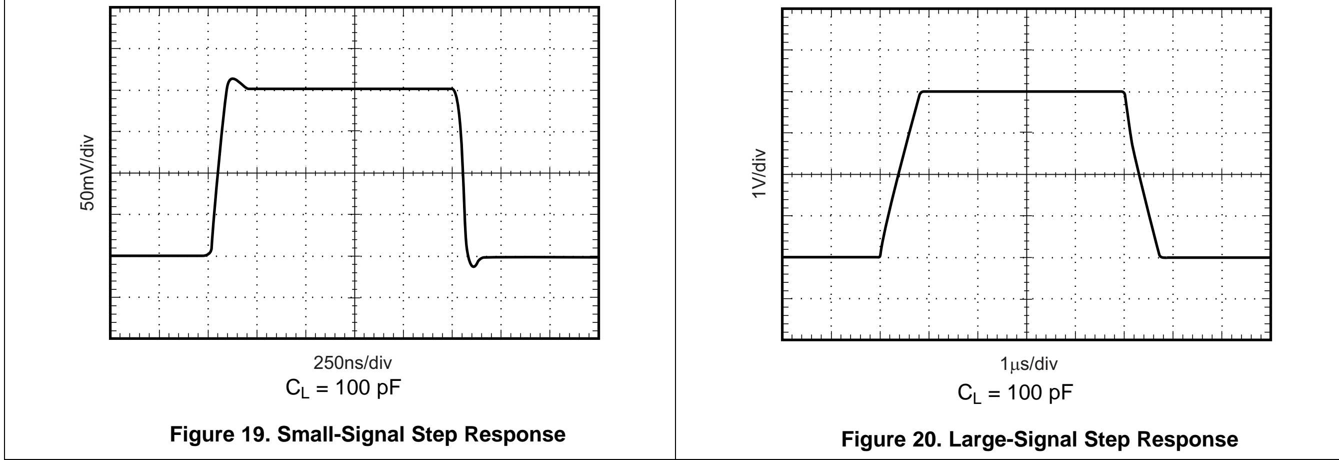


Figure 18. Channel Separation vs Frequency

Typical Characteristics (continued)

at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{OUT} = V_S / 2, and V_{CM} = V_S / 2, (unless otherwise noted)



C_L = 100 pF

Figure 19. Small-Signal Step Response

C_L = 100 pF

Figure 20. Large-Signal Step Response

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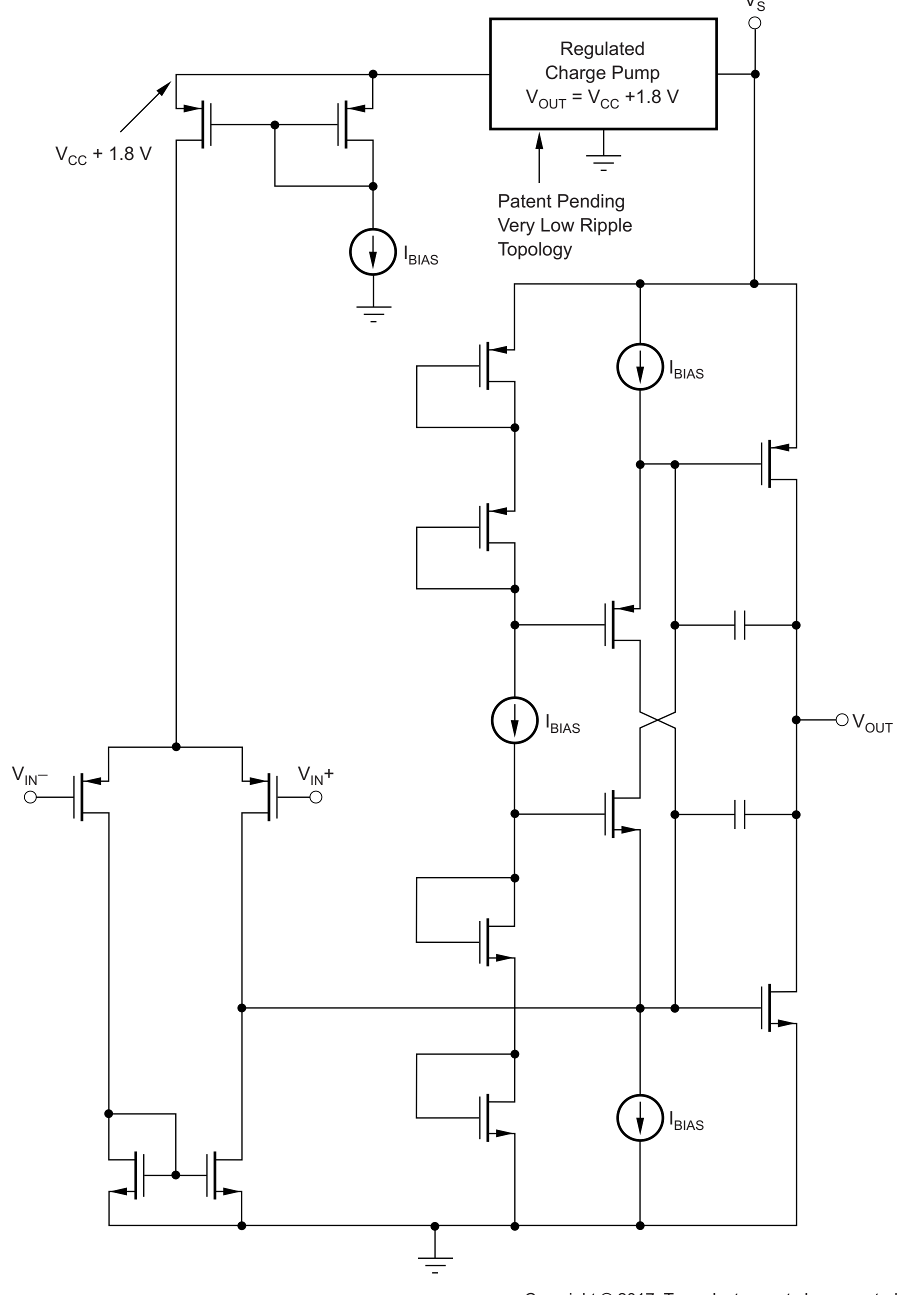
8 Detailed Description

8.1 Overview

The OPA363 and OPA364 series op amps are rail-to-rail operational amplifiers with excellent CMRR, low noise, low offset, and wide bandwidth on supply voltages as low as ±0.9 V. The OPA363 features an additional pin for a shutdown and enable function. These families do not exhibit phase reversal and are unity-gain stable. Specified over the industrial temperature range of –40°C to +125°C, the OPA363 and OPA364 families offer precision performance for a wide range of applications.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Rail-to-Rail Input

The OPA363 and OPA364 feature excellent rail-to-rail operation, with supply voltages as low as ±0.9 V. The input common-mode voltage range of the OPA363 and OPA364 family extends 100 mV beyond supply rails. The unique input topology of the OPA363 and OPA364 eliminates the input offset transition region typical of most rail-to-rail, complementary stage operational amplifiers, allowing the OPA363 and OPA364 to provide superior common-mode performance over the entire common-mode input range, as seen in Figure 21. This feature prevents degradation of the differential linearity error and THD when driving A/D converters. A simplified schematic of the OPA363 and OPA364 is shown in the *Functional Block Diagram*.

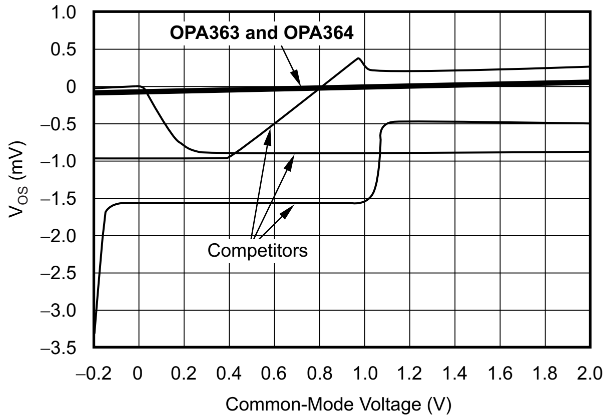

Figure 21. OPA363 and OPA364 Have Linear Offset Over Entire Common-Mode Range

8.3.2 Operating Voltage

The OPA363 and OPA364 series op amp parameters are fully specified from 1.8 V to 5.5 V. Single 0.1-µF bypass capacitors must be placed across supply pins and as close to the part as possible. Supply voltages higher than 5.5 V (absolute maximum) may cause permanent damage to the amplifier. Many specifications apply from –40°C to +125°C. Parameters that vary significantly with operating voltages or temperature are shown in the *Typical Characteristics*.

8.3.3 Capacitive Load

The OPAx363 and OPAx364 series op amps can drive a wide range of capacitive loads. However, all op amps under certain conditions may become unstable. Op amp configuration, gain, and load value are a few of the factors to consider when determining stability. An op amp in unity-gain configuration is the most susceptible to the effects of capacitive load. The capacitive load reacts with the output resistance of the op amp to create a pole in the small-signal response, which degrades the phase margin.

In unity gain, the OPAx363 and OPAx364 series op amps perform well with a pure capacitive load up to approximately 1000 pF. The equivalent series resistance (ESR) of the loading capacitor may be sufficient to allow the OPA363 and OPA364 to directly drive very large capacitive loads (greater than 1 µF). Increasing gain enhances the ability of the amplifier to drive more capacitance; see Figure 13.

One method of improving capacitive load drive in the unity-gain configuration is to insert a 10-Ω to 20-Ω resistor in series with the output, as shown in Figure 22. This resistor significantly reduces ringing with large capacitive loads. However, if there is a resistive load in parallel with the capacitive load, the load creates a voltage divider, introduces a DC error at the output, and slightly reduces output swing. This error may be insignificant. For example, with R_L = 10 kΩ and R_S = 20 Ω, there is an approximate 0.2% error at the output.

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Feature Description (continued)

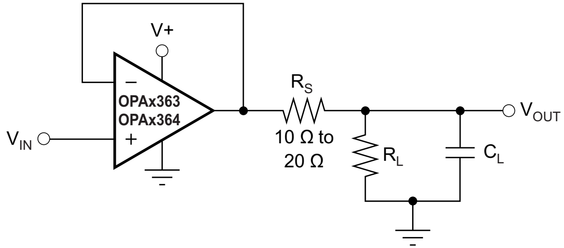

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Figure 22. Improving Capacitive Load Drive

8.3.4 Input and ESD Protection

All OPAx363 and OPAx364 pins are static-protected with internal ESD protection diodes tied to the supplies. These diodes provide overdrive protection if the current is externally limited to 10 mA, as shown in the *Absolute Maximum Ratings* and shown in Figure 23.

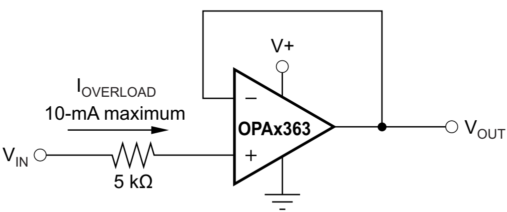

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Figure 23. Input Current Protection

8.4 Device Functional Modes

8.4.1 Enable Function

The shutdown (enable) function of the OPAx363 is referenced to the negative supply voltage of the operational amplifier. A logic level HIGH enables the op amp. A valid logic HIGH is defined as voltage greater than 75% of the positive supply applied to the enable pin. The valid logic HIGH signal can be as much as 5.5 V above the negative supply, independent of the positive supply voltage. A valid logic LOW is defined as less than 0.8 V above the negative supply pin. If dual or split power supplies are used, take care to ensure that logic input signals are properly referred to the negative supply voltage. This pin must be connected to a valid high or low voltage or driven, not left open-circuit.

The logic input is a high-impedance CMOS input. Dual op amps are provided separate logic inputs. For battery-operated applications, this feature reduces the average current and extend battery life. The enable time is 20 μs; disable time is 1 μs. When disabled, the output assumes a high-impedance state. This configuration allows the OPAx363 to operate as a *gated* amplifier, or to have the output multiplexed onto a common analog output bus.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Achieving Output Swing to the Op Amp Negative Rail

Some applications require an accurate output voltage swing from 0 V to a positive full-scale voltage. A good single-supply op amp may be able to swing within a few millivolts of single-supply ground, but as the output is driven toward 0 V, the output stage of the amplifier prevents the output from reaching the negative supply rail of the amplifier.

The output of the OPAx363 or OPAx364 can be made to swing to ground, or slightly below, on a single-supply power source. To do so requires use of another resistor and an additional, more negative power supply than the op amp negative supply. A pulldown resistor may be connected between the output and the additional negative supply to pull the output down below the value that the output would otherwise achieve, as shown in Figure 24.

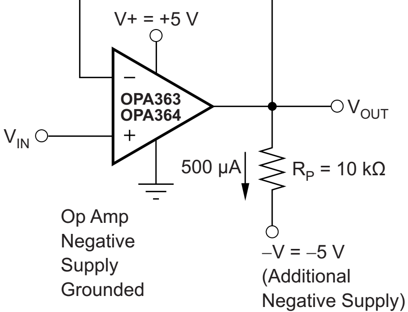

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Figure 24. OPA363 and OPA364 Swing to Ground

This technique does not work with all op amps. The output stage of the OPAx363 and OPA3x64 allows the output voltage to be pulled below that of most op amps, if approximately 500 μA is maintained through the output stage. To calculate the appropriate value load resistor and negative supply, R_L = –V / 500 μA. The OPAx363 and OPAx364 are characterized to perform well under the described conditions, maintaining excellent accuracy down to 0 V and as low as –10 mV. Limiting and nonlinearity occur below –10 mV, with linearity returning as the output is again driven above –10 mV.

9.1.2 Directly Driving the ADS8324 and the MSP430

The OPAx363 and OPAx364 series op amps are optimized for driving medium speed (up to 100-kHz) sampling A/D converters. However, they also offer excellent performance for higher speed converters. The no-crossover input stage of the OPAx363 and OPAx364 directly drive A/D converters without degradation of differential linearity and THD. They provide an effective means of buffering the A/D converter input capacitance and resulting charge injection while providing signal gain. Figure 25 and Figure 26 show the OPAx363 and OPAx364 configured to drive the ADS8324 and the 12-bit A/D converter on the MSP430.

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Application Information (continued)

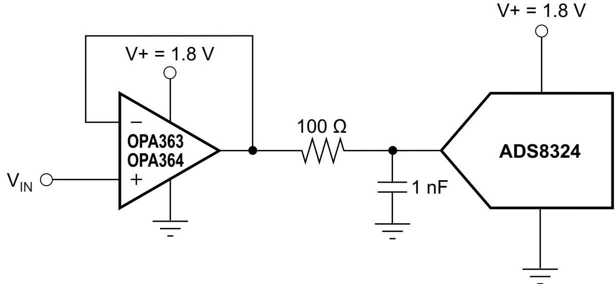

Figure 25. OPAx363 and OPAx364 Directly Drive the ADS8324

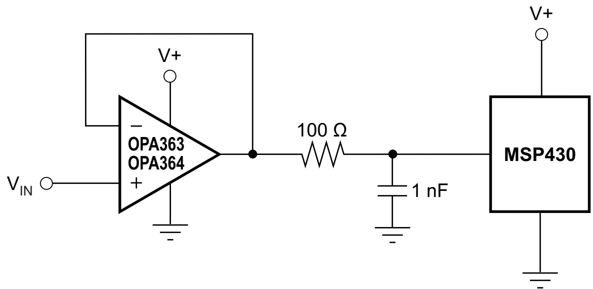

Figure 26. Driving the 12-Bit A/D Converter on the MSP430

9.1.3 Audio Applications

The OPAx363 and OPAx364 op amp family has linear offset voltage over the entire input common-mode range. Combined with low noise, this feature makes the OPAx363 and OPAx364 suitable for audio applications. Single-supply, 1.8-V operation allows the OPA2363 and OPA2364 to be optimal candidates for dual stereo-headphone drivers and microphone preamplifiers in portable stereo equipment; see Figure 27 and Figure 28.

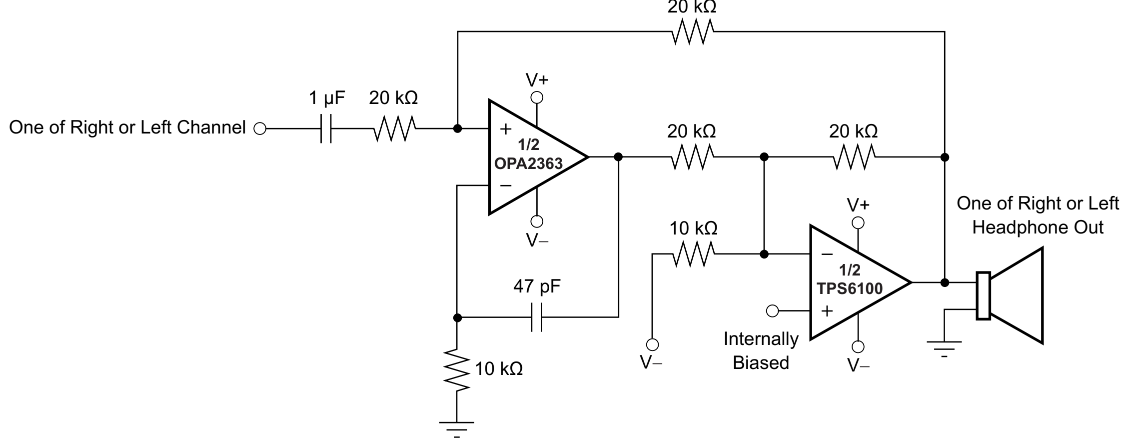

Figure 27. OPA2363 Configured as Half of a Dual Stereo-Headphone Driver

Application Information (continued)

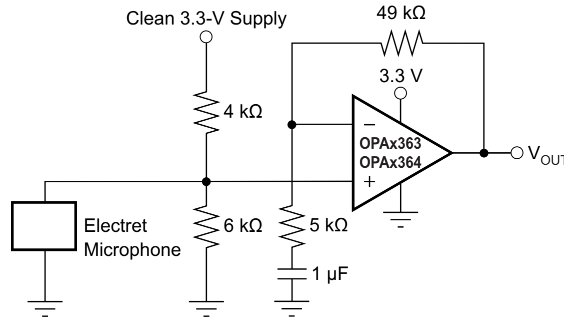

Figure 28. Microphone Preamplifier

9.1.4 Active Filtering

Low harmonic distortion and noise specifications plus high gain and slew rate make the OPAx363 and OPAx364 optimal candidates for active filtering. Figure 29 shows the OPA2363 configured as a low-distortion, third-order general immittance converter (GIC) filter. Figure 30 shows the implementation of a Sallen-Key, 3-pole, low-pass Bessel filter.

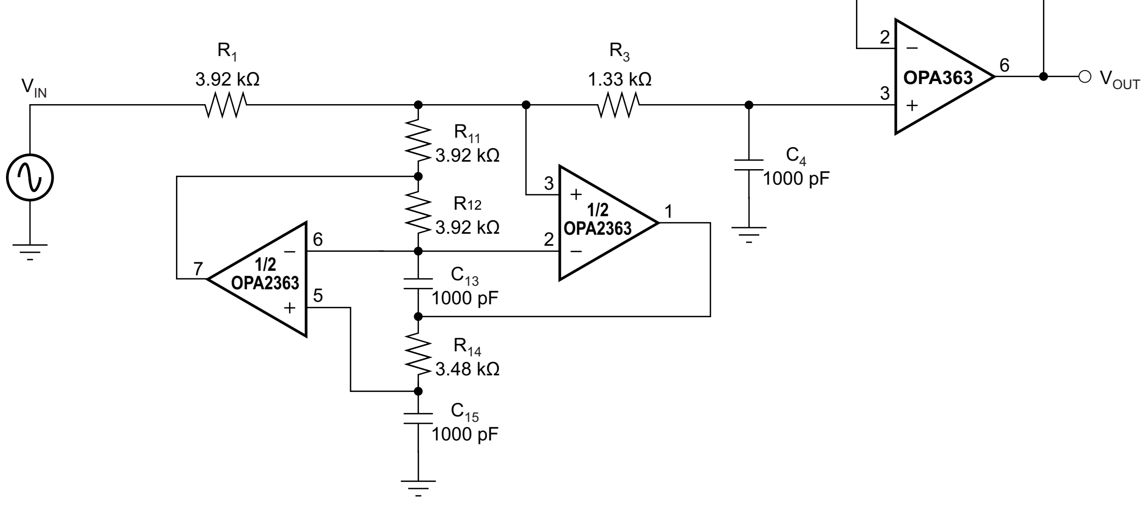

Figure 29. OPA2363 as a Third-Order, 40-kHz, Low-Pass GIC Filter

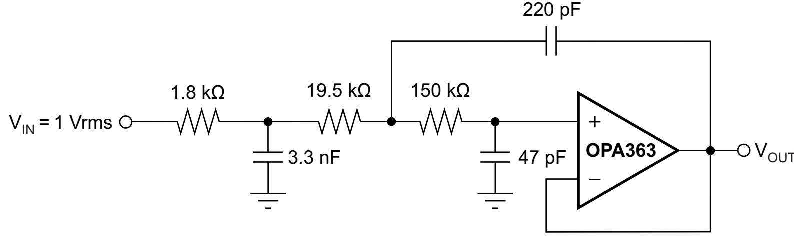

Figure 30. OPAx363 or OPAx364 Configured as a 3-Pole, 20-kHz, Sallen-Key Filter

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9.2 Typical Application

9.2.1 Single-Supply Electret Microphone Preamplifier

Electret microphones are commonly used in portable electronics because of their small size, low cost, and relatively good signal-to-noise ratio (SNR). The small package size and excellent AC performance of the OPA364 make it an excellent choice for preamplifier circuits for electret microphones. The circuit shown in Figure 31 is a single-supply preamplifier circuit for electret microphones.

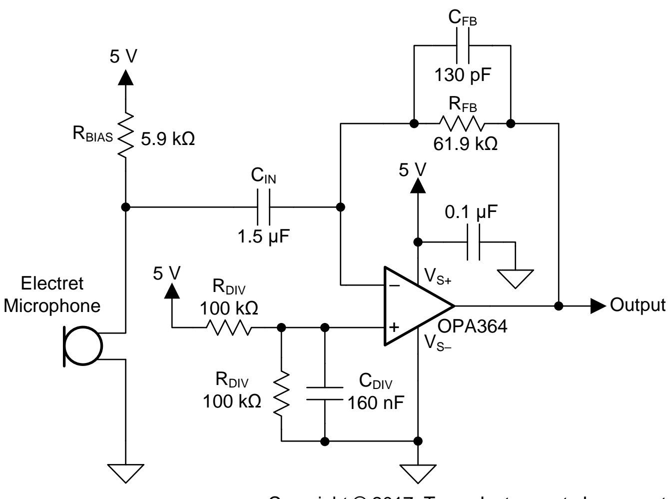

Figure 31. Preamplifier Circuit for Electret Microphones Using a Single-Supply Voltage

9.2.1.1 Design Requirements

- 5-V single supply
- 1-V_{RMS} output for 100-dB_{SPL} input
- 20-Hz to 20-kHz, –3-dB bandwidth
- Microphone sensitivity: 8 µA/Pa
- Microphone operating voltage: 2 V to 10 V
- Microphone bias current: 500 µA

9.2.1.2 Detailed Design Procedure

In this circuit, the op amp is configured as a transimpedance amplifier which converts the signal current of the microphone into an output voltage. The gain of the circuit is determined by the feedback resistor R_{FB}, which must be calculated according to the microphone sensitivity. For this design, a microphone output current of 8 µA per Pascal (Pa) of air pressure was chosen. Using this value, the output current for a sound pressure level of 100 dB_{SPL}, or 2 Pa air pressure, is calculated in Equation 1.

$$i_{mic} = \frac{8\ \mu A}{1\ Pa} \times 2\ Pa = 16\ \mu A \tag{1}$$

R_{FB} is then calculated from this current to produce 1-V_{RMS} output for a 100-dB_{SPL} input signal in Equation 2.

$$R_{FB} = \frac{V_O}{i_{mic}} = \frac{1\ V_{RMS}}{16\ \mu A} = 62500 \rightarrow 61.9\ k\Omega \tag{2}$$

The feedback capacitor (C_{FB}) is calculated to limit the bandwidth of the amplifier to 20 kHz in Equation 3.

$$C_{FB} = \frac{1}{2 \cdot \pi \cdot R_{FB} \cdot f_H} = \frac{1}{2 \cdot \pi \cdot (61.9\ k\Omega) \cdot (20\ kHz)} = 128.5 \times 10^{-12} \rightarrow 130\ pF \tag{3}$$

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Typical Application (continued)

R_{BIAS} is required to divert the microphone signal current through capacitor C_{IN} rather than flowing from the power supply, V_{CC}. Larger values of R_{BIAS} allow for a smaller capacitor to be used for C_{IN} and reduce the overall noise of the circuit. However, the maximum value for R_{BIAS} is limited by the microphone bias current and minimum operating voltage.

The value of R_{BIAS} is calculated in Equation 4.

$$R_{BIAS} = \frac{V_{CC} - V_{MIC}}{I_{BIAS}} = \frac{5\ V - 2\ V}{500\ \mu A} = 6000 \rightarrow 5.9\ k\Omega \tag{4}$$

Input capacitor C_{IN} forms a high-pass filter in combination with resistor R_{BIAS}. The filter corner frequency calculation is shown in Equation 5 to place the high-pass corner frequency at 20 Hz.

$$C_{IN} = \frac{1}{2 \cdot \pi \cdot R_{BIAS} \cdot f_L} = \frac{1}{2 \cdot \pi \cdot (5.9\ k\Omega) \cdot (20\ Hz)} = 1.349 \times 10^{-6} \rightarrow 1.5\ \mu F \tag{5}$$

The voltage divider network at the op amp noninverting input is used to bias the op amp output to the mid-supply point (V_{CC} / 2) to maximize the output voltage range of the circuit. This result is easily achieved by selecting the same value for both resistors in the divider. The absolute value of those resistors is limited by the acceptable power-supply current drawn by the voltage divider. Selecting 25 µA as an acceptable limit of supply current gives a value of 100 kΩ for the resistors in the divider, as Equation 6 shows.

$$R_{DIV} = \frac{V_{CC}}{2 \cdot I_{DIV}} = \frac{5\ V}{2 \cdot 25\ \mu A} = 100\ k\Omega \tag{6}$$

Finally, to minimize the additional noise contribution from the voltage divider, a capacitor is placed at the op amp noninverting input. This capacitor forms a low-pass filter with the parallel combination of the voltage divider resistors. Selecting a filter corner frequency of 20 Hz minimizes the noise contribution of the voltage divider inside the amplifier passband; see Equation 7.

$$C_{DIV} = \frac{1}{2 \cdot \pi \cdot \left(\frac{R_{DIV}}{2}\right) \cdot f_L} = \frac{1}{2 \cdot \pi \cdot \left(\frac{100\ k\Omega}{2}\right) \cdot (20\ Hz)} = 1.592 \times 10^{-7} \rightarrow 160\ nF \tag{7}$$

9.2.1.3 Application Curve

The transfer function of the microphone preamplifier circuit is shown in Figure 32. The nominal gain of the circuit is 95.82 dB, or 61,800 V per amp of input current. The –3-dB bandwidth limits of the circuit are 17.99 Hz and 19.23 kHz.

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Typical Application (continued)

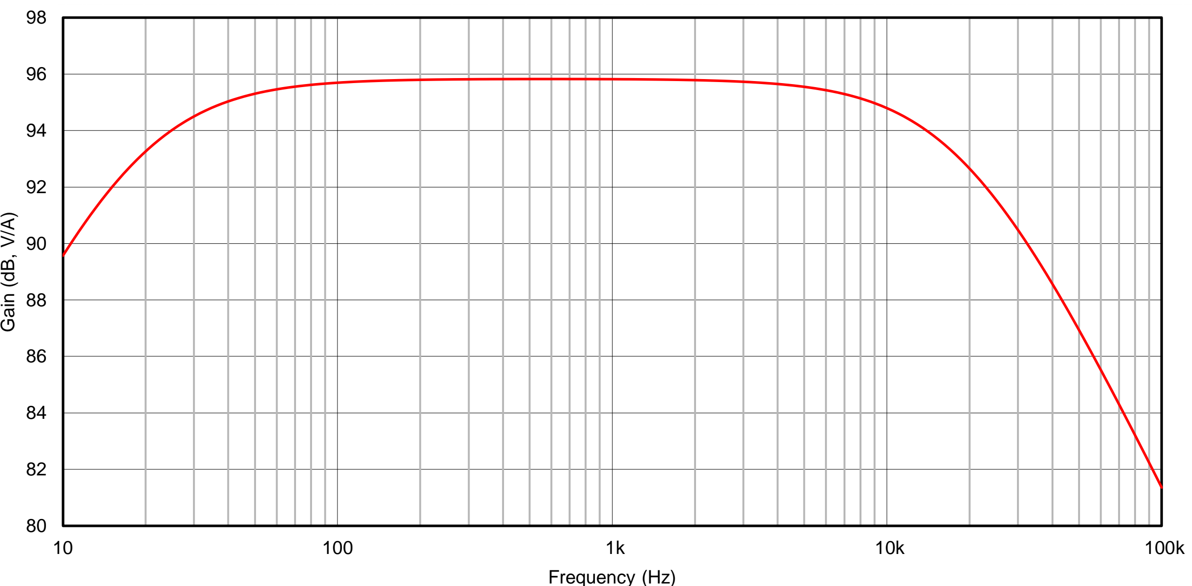

Figure 32. Microphone Preamplifier Transfer Function

10 Power Supply Recommendations

The OPAx363 and OPAx364 are specified for operation from 2.7 V to 5.5 V (±1.35 V to ±2.75 V). Parameters that can exhibit significant variance with regard to operating voltage are presented in the *Electrical Characteristics*.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good printed-circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and of op amp itself. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in Figure 33, keeping R_F and R_G close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

11.2 Layout Example

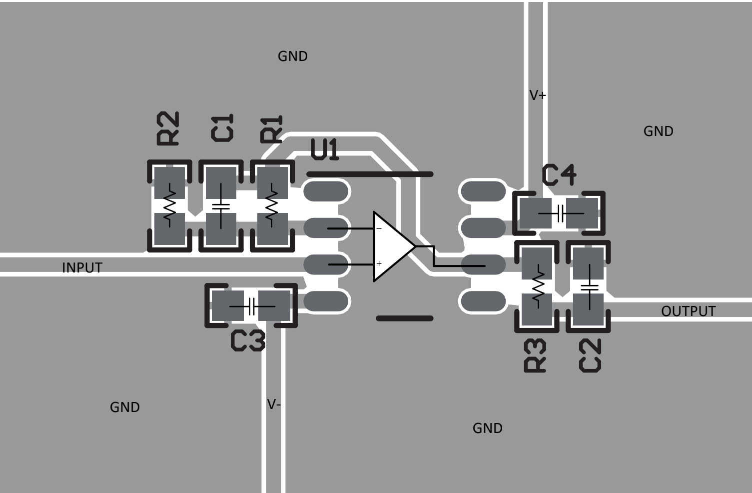

Figure 33. Operational Amplifier Board Layout for Noninverting Configuration

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Layout Example (continued)

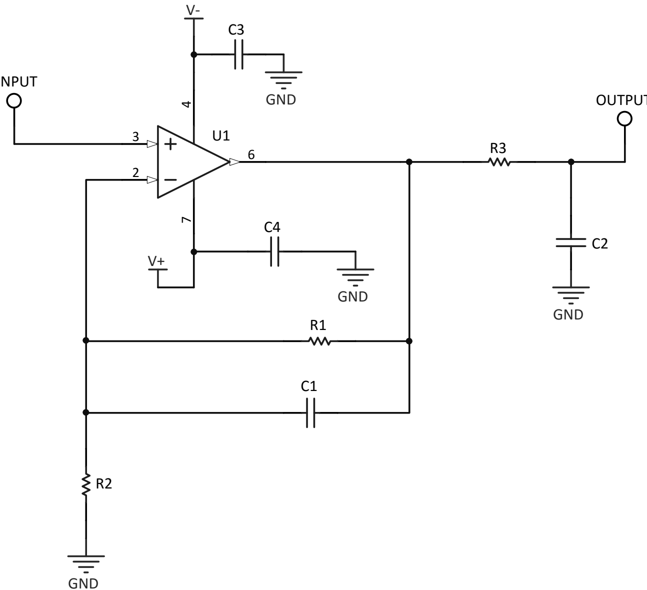

Figure 34. Layout Example Schematic

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12.1.1 开发支持

12.1.1.1 TINA-TI™（免费软件下载）

TINA™是一款简单、功能强大且易于使用的电路仿真程序，此程序基于 SPICE 引擎。 TINA-TI™ 是 TINA 软件的一款免费全功能版本，除了一系列无源和有源模型外，此版本软件还预先载入了一个宏模型库。TINA-TI 提供所有传统的 SPICE 直流、瞬态和频域分析，以及其他设计功能。

TINA-TI 可从 Analog eLab Design Center（模拟电子实验室设计中心）免费下载，它提供全面的后续处理能力，使得用户能够以多种方式形成结果。虚拟仪器提供选择输入波形和探测电路节点、电压和波形的功能，从而创建一个动态的快速入门工具。

注

这些文件需要安装 TINA 软件（由 DesignSoft™提供）或者 TINA-TI 软件。请从 TINA-TI 文件夹 中下载免费的 TINA-TI 软件。

12.1.1.2 DIP 适配器 EVM

DIP 适配器 EVM 工具提供了一种针对小型表面贴装器件进行原型设计的简易低成本方法。这些 TI 封装的评估工具：D 或 U（8 引脚 SOIC）、PW（8 引脚 TSSOP）、DGK（8 引脚 MSOP）、DBV（6 引脚 SOT-23、5 引脚 SOT-23 和 3 引脚 SOT-23）、DCK（6 引脚 SC-70 和 5 引脚 SC-70）和 DRL（6 引脚 SOT-563）。DIP 适配器 EVM 也可搭配引脚排使用或直接与现有电路相连。

12.1.1.3 通用运放 EVM

通用运放 EVM 是一系列通用空白电路板，可简化采用各种器件封装类型的电路板原型设计。借助评估模块电路板设计，可以轻松快速地构造多种不同电路。共有 5 个模型可供选用，每个模型都对应一种特定封装类型。支持 PDIP、SOIC、MSOP、TSSOP 和 SOT-23 封装。

注

这些电路板均为空白电路板，用户必须自行提供相关器件。TI 建议您在订购通用运算放大器 EVM 时申请几个运算放大器器件样品。

12.1.1.4 TI 高精度设计

TI 高精度设计的模拟设计方案是由 TI 公司高精度模拟实验室设计 应用 专家创建的模拟解决方案，提供了许多实用电路的工作原理、组件选择、仿真、完整印刷电路板 (PCB) 电路原理图和布局布线、物料清单以及性能测量结果。欲获取 TI 高精度设计，请访问 http://www.ti.com.cn/ww/analog/precision-designs/。

12.1.1.5 WEBENCH®滤波器设计器

WEBENCH® 滤波器设计器是一款简单、功能强大且便于使用的有源滤波器设计程序。借助WEBENCH 滤波设计器，用户可使用精选 TI 运算放大器和 TI 供应商合作伙伴提供的无源组件来打造最佳滤波器设计方案。

WEBENCH® 设计中心以基于网络的工具形式提供 WEBENCH® 滤波器设计器。用户通过该工具可在短时间内完成多级有源滤波器解决方案的设计、优化和仿真。

12.2 Documentation Support

12.2.1 Related Documentation

使用 OPAx363 和 OPAx364 时，建议参考下列相关文档。所有这些文档都可从 www.ti.com.cn 上下载（除非另有说明）。

- *《AB-045 运算放大器性能分析》*
- *《AB-067 运算放大器的单电源操作》*
- *《AB-105 在放大器中进行调优》*

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Documentation Support (接下页)

- *《QFN/SON PCB 连接》*
- *《四方扁平无引线逻辑器件封装》*

12.3 相关链接

下面的表格列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 **1.** 相关链接

器件	产品文件夹	立即订购	技术文档	工具和软件	支持和社区
OPA363	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
OPA2363	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
OPA364	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
OPA2364	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
OPA4364	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.4 接收文档更新通知

如需接收文档更新通知，请访问 ti.com 上的器件产品文件夹。In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.5 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI* 的工程师对工程师 *(E2E)* 社区。**此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 ***TI* 参考设计支持** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

12.6 商标

TINA-TI, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
TINA, DesignSoft are trademarks of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

12.7 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.8 Glossary

SLYZ022 — *TI Glossary*.
This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2363AIDGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	BHK	Samples
OPA2363AIDGST	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	BHK	Samples
OPA2363AIDGSTG4	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	BHK	Samples
OPA2363AIRSVR	ACTIVE	UQFN	RSV	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	SIN	Samples
OPA2363IDGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	BHK	Samples
OPA2363IDGST	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	BHK	Samples
OPA2363IDGSTG4	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	BHK	Samples
OPA2364AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 2364 A	Samples
OPA2364AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 2364 A	Samples
OPA2364AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	BHL	Samples
OPA2364AIDGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	BHL	Samples
OPA2364AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	BHL	Samples
OPA2364AIDGKTG4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	BHL	Samples
OPA2364AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 2364 A	Samples
OPA2364AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 2364 A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2364ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 2364	Samples
OPA2364IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	BHL	Samples
OPA2364IDGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	BHL	Samples
OPA2364IDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	BHL	Samples
OPA2364IDGKTG4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	BHL	Samples
OPA2364IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 2364	Samples
OPA2364IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 2364	Samples
OPA363AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 363 A	Samples
OPA363AIDBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A40	Samples
OPA363AIDBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A40	Samples
OPA363AIDBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A40	Samples
OPA363AIDBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A40	Samples
OPA363ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 363	Samples
OPA363IDBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A40	Samples
OPA363IDBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A40	Samples
OPA363IDBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A40	Samples
OPA363IDBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A40	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA363IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 363	Samples
OPA364AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 364 A	Samples
OPA364AIDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A41	Samples
OPA364AIDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A41	Samples
OPA364AIDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A41	Samples
OPA364AIDBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A41	Samples
OPA364AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 364 A	Samples
OPA364ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 364	Samples
OPA364IDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A41	Samples
OPA364IDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A41	Samples
OPA364IDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A41	Samples
OPA364IDBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A41	Samples
OPA364IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 364	Samples
OPA364IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 364	Samples
OPA364IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 364	Samples
OPA4364AID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4364A	Samples
OPA4364AIDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4364A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA4364AIDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4364A	Samples
OPA4364AIDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4364A	Samples
OPA4364AIPWR	ACTIVE	TSSOP	PW	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 4364A	Samples
OPA4364AIPWRG4	ACTIVE	TSSOP	PW	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 4364A	Samples
OPA4364AIPWT	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 4364A	Samples
OPA4364AIPWTG4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 4364A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

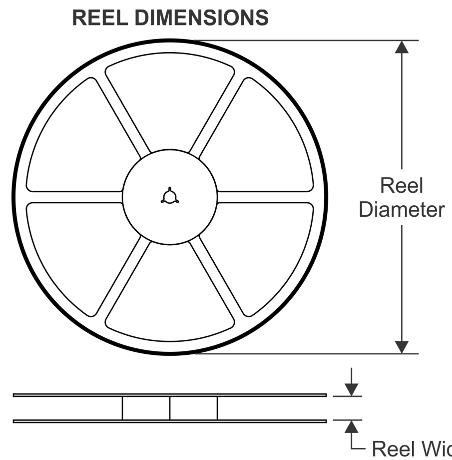
OTHER QUALIFIED VERSIONS OF OPA4364 :

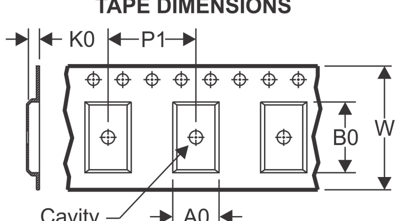
- Automotive: OPA4364-Q1

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

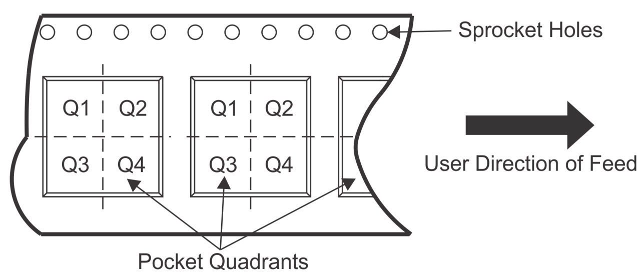
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

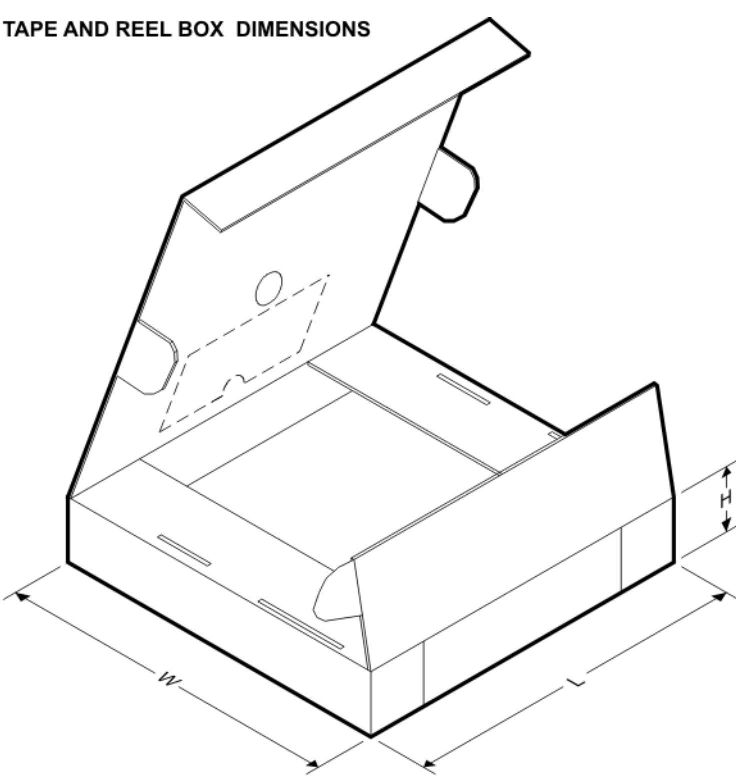


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2363AIDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2363AIDGST	VSSOP	DGS	10	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2363AIRSVR	UQFN	RSV	16	3000	177.8	12.4	2.0	2.8	0.7	4.0	12.0	Q1
OPA2363IDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2363IDGST	VSSOP	DGS	10	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2364AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2364AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2364AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2364IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2364IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2364IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA363AIDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
OPA363AIDBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
OPA363IDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
OPA363IDBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
OPA364AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA364IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4364AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA4364AIPWR	TSSOP	PW	14	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA4364AIPWT	TSSOP	PW	14	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2363AIDGSR	VSSOP	DGS	10	2500	367.0	367.0	35.0
OPA2363AIDGST	VSSOP	DGS	10	250	210.0	185.0	35.0
OPA2363AIRSVR	UQFN	RSV	16	3000	223.0	270.0	35.0
OPA2363IDGSR	VSSOP	DGS	10	2500	367.0	367.0	35.0
OPA2363IDGST	VSSOP	DGS	10	250	210.0	185.0	35.0
OPA2364AIDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
OPA2364AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
OPA2364AIDR	SOIC	D	8	2500	367.0	367.0	35.0
OPA2364IDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
OPA2364IDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
OPA2364IDR	SOIC	D	8	2500	367.0	367.0	35.0
OPA363AIDBVR	SOT-23	DBV	6	3000	565.0	140.0	75.0
OPA363AIDBVT	SOT-23	DBV	6	250	565.0	140.0	75.0
OPA363IDBVR	SOT-23	DBV	6	3000	565.0	140.0	75.0
OPA363IDBVT	SOT-23	DBV	6	250	565.0	140.0	75.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA364AIDR	SOIC	D	8	2500	367.0	367.0	35.0
OPA364IDR	SOIC	D	8	2500	367.0	367.0	35.0
OPA4364AIDR	SOIC	D	14	2500	367.0	367.0	38.0
OPA4364AIPWR	TSSOP	PW	14	2500	367.0	367.0	35.0
OPA4364AIPWT	TSSOP	PW	14	250	210.0	185.0	35.0

DBV (R-PDSO-G6) PLASTIC SMALL-OUTLINE PACKAGE

0,95
6X 0,50 / 0,25
E.
⌖ 0,20 Ⓜ
6 4
1,75 / 1,45
3,00 / 2,60
Pin 1 Index Area (See Detail)
1 3
3,05 / 2,75

6 4
Pin 1 Index Area
1 3
DETAIL: OPTIONAL ORIENTATION MARKING

0,22 / 0,08
Gage Plane
0,25
0°–8°
0,60 / 0,30

1,45 MAX
0,15 / 0,00
Seating Plane
⌓ 0,10

4073253-5/N 12/14

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO-178 Variation AB, except minimum lead width.

DBV (R-PDSO-G6) PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

1,00

0,55

2,7

2,7

0,95

0,95

0,6

Solder Mask Opening

1,05

Pad Geometry

0,07
All Around

4209593-4/C 08/11

NOTES:

A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.

D. Publication IPC-7351 is recommended for alternate designs.

E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

RSV (R-PUQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD

2,65
2,55
A
B
12 11 10 9
13 8
14 7
15 6
16 5
1,85
1,75
Pin 1 Index Area
1 2 3 4

0,55
0,45
D
0,13 Nominal
Lead Frame
Seating Plane
0,05 C
0,05
0,00
Seating Height
C

1,20
0,40
0,55
0,45
1 2 3 4
16 5
15 6
Pin 1 Identifier
0,10 X 45°
14 7
13 8
1,20
12 11 10 9
15X 0,45
0,35
16X 0,25
0,15
0,07 M C A B
0,05 M C

Bottom View

4207974/D 12/11

NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No-Lead) package configuration.
D. This package complies to JEDEC MO-288 variation UFHE, except minimum package thickness.

RSV (R–PUQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

Example Board Layout

3,00
1,70
0,40
2,20
0,40
0,90
0,75
0,65
0,20
Pin 1 ID

Example Stencil Design
0.125mm Stencil Thickness
(Note F&G)

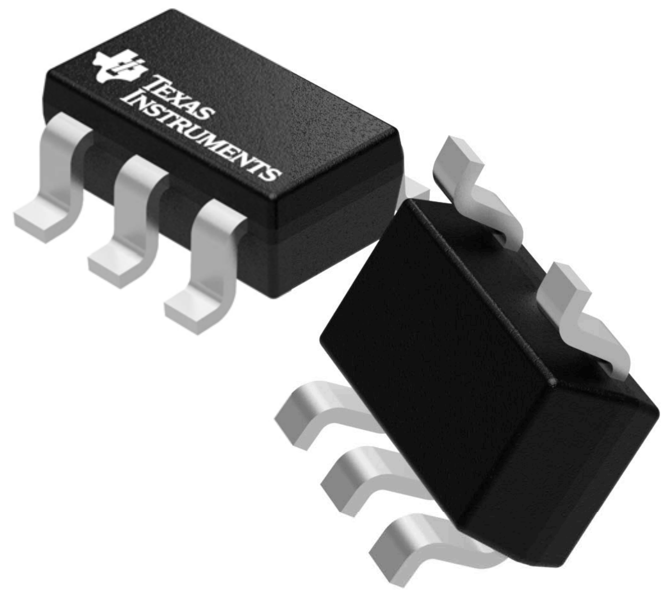
3,00
1,70
0,40
2,20
0,40
0,90
0,75
0,65
0,20
Pin 1 ID

Non Solder Mask Defined Pad

0,05
all around
Example
Solder Mask Opening
(Note D)
Example
Pad Geometry
(Note C)
0,10

4208244/C 02/13

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4214839/C 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.

PKG
5X (1.1)
5X (0.6)
1
2
3
4
5
SYMM
(1.9)
2X (0.95)
(R0.05) TYP
(2.6)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

SOLDER MASK OPENING
METAL
EXPOSED METAL
0.07 MAX ARROUND
NON SOLDER MASK DEFINED (PREFERRED)

METAL UNDER SOLDER MASK
SOLDER MASK OPENING
EXPOSED METAL
0.07 MIN ARROUND
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214839/C 04/2017

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

PKG
5X (1.1)
1
5X (0.6)
5
SYMM
2
(1.9)
2X(0.95)
3
4
(R0.05) TYP
(2.6)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE

0.344 (8,75)
0.337 (8,55)
C

14 8

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80) D

1 7

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)
0.010 (0,25) M

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

Gauge Plane

0.004 (0,10)

Seating Plane

0.010 (0,25)

0°–8°

0.050 (1,27)
0.016 (0,40)

4040047–5/M 06/11

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14) PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

12x1,27

5,40

Stencil Openings
(Note D)

14x0,55

12x1,27

14x1,50

5,40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,60

1,55

Example
Solder Mask Opening
(See Note E)

0.07
All Around

4211283-3/E 08/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE

4040064-3/G 02/11

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

12x0,65

5,60

Stencil Openings
(Note D)

14x0,30

12x0,65

14x1,55

5,60

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,35

1,60

Example
Solder Mask Opening
(See Note E)

0,07
All Around

4211284–2/G 08/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE

0.197 (5,00)
0.189 (4,80)
C
8 5
0.244 (6,20)
0.228 (5,80)
0.157 (4,00)
0.150 (3,80)
D
Pin 1 Index Area
1 4
0.050 (1,27)
0.020 (0,51)
0.012 (0,31)
0.010 (0,25) M
0.069 (1,75) Max
0.010 (0,25)
0.004 (0,10)
0.010 (0,25)
0.005 (0,13)
Gauge Plane
0.004 (0,10)
Seating Plane
0.010 (0,25)
0°–8°
0.050 (1,27)
0.016 (0,40)

4040047-3/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

6x1,27

5,40

Stencil Openings
(Note D)

8x0,55

6x1,27

8x1,50

5,40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,60

1,55

0,07
All Around

Example
Solder Mask Opening
(See Note E)

4211283-2/E 08/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE

0,65
0,38
0,25
0,13 M
8
5
1
4
3,10
2,90
5,05
4,75
D
C
0,23
0,13
Gauge Plane
0,25
0°–8°
0,70
0,40
1,10 MAX
0,15
0,05
Seating Plane
0,10

4073329/E 05/06

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DGK (S-PDSO-G8) PLASTIC SMALL OUTLINE PACKAGE

Example Board Layout

(0,65)TYP.

8 5

PKG ℄

(4,4)

1 4

PKG ℄

Example Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).
(See Note D)

8X(0,45)

(0,65)TYP.

8X(1,45)

PKG ℄

(4,4)

PKG ℄

Example
Non Soldermask Defined Pad

(0,45)

(1,45)

(0,05)
All Around

Example
Solder Mask Opening
(See Note E)

Pad Geometry
(See Note C)

4221236/A 11/13

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DGS (S-PDSO-G10) PLASTIC SMALL-OUTLINE PACKAGE

0,50

0,27
0,17

0,08 M

10 6

1 5

3,10
2,90

5,05
4,75

3,10
2,90

0,23
0,13

Gauge Plane

0,25

0°–8°

0,70
0,40

1,10 MAX

0,15
0,05

Seating Plane

0,10

4073272/C 02/04

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. Falls within JEDEC MO-187 variation BA.

DGS (S-PDSO-G10) PLASTIC SMALL OUTLINE PACKAGE

Example Board Layout

(0,5)TYP.

10 6

PKG ℄ (4,4)

1 5

PKG ℄

Example Non Soldermask Defined Pad

(0,3)

(1,45)

(0,05) All Around

Example Solder Mask Opening (See Note E)

Pad Geometry (See Note C)

Example Stencil Openings Based on a stencil thickness of .127mm (.005inch). (See Note D)

10X(0,3) (0,5)TYP.

10X(1,45) 10 6

PKG ℄ (4,4)

1 5

PKG ℄

4215304/A 11/13

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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