

FEATURES

- New generation charge pump technology : K-Chargepump, efficiency reaches as high as 92%
- Power amplifier overall efficiency 75%, greatly prolong mobile phone usage time
- Ultra-low distortion: 0.02%
- Within Lithium battery voltage range, output power is maintained constant
- ◆ Output Power level: 0.8W、1W、1.2W
- Second generation Non-crack-noise (NCN) technology
- Super TDD-Noise suppression
- Ultra-low EMI
- One wire pulse control
- High PSRR: -65dB (217Hz)
- Small 2mm×2mm FC-16package

APPLICATIONS

• Smart phone

DESCRIPTION

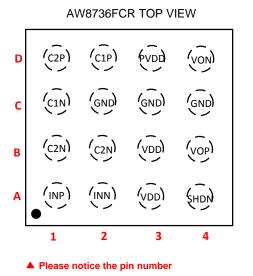
AW8736 is designed to enhance smart mobile phone sound quality, which is a new high efficiency, ultra-low distortion, constant large volume, sixth generation class K audio amplifiers. Using a new generation of charge pump technology: K -Chargepump structure, efficiency as high as 92%, power amplifier's overall efficiency reaches 75%, greatly prolong the mobile phone usage time. 0.02% ultra-low distortion and unique non-crack-noise (NCN) technology brings high quality music enjoyment.

AW8736 integrated K-Chargepump booster circuit, the output power cannot drop along with lithium battery voltage lower down. Within lithium battery voltage range(3.3 V - 4.35V), output power is constant, providing high quality music enjoyment. AW8736 has 0.8 W, 1 W and 1.2 W three output power level, recommended using rated power of 0.7W and above speakers, which greatly improve the volume, and effectively protect speakers.

The AW8736 uses awinic proprietary TDD-Noise suppression technology and EMI suppression technology, effectively restrain TDD-Noise and EMI interference.

AW8736 built-in over current protection, over-temperature protection and short circuit protection function, effectively protect the chip. The AW8736 uses small 2mmx2mm FC-16 package.

DEVICE PINOUT



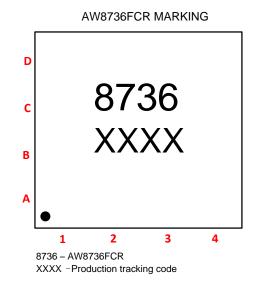


Figure 1 AW8736FCR pin diagram top view and device marking COPYRIGHT ©2012 SHANGHAI AWINIC TECHNOLOGY CO., LTD.



PIN DESCRIPTION

Number	Symbol	Description
A1	INP	Positive audio input terminal
A2	INN	Negative audio input terminal
A3, B3	VDD	Power supply
A4	SHDN	Chip power down pin, active low; one wire pulse control;
B1	C2N	Negative side of the external charge pump flying capacitor C2
B2		
B4	VOP	Positive audio output terminal
C1	C1N	Negative side of the external charge pump flying capacitor C1
C2		
C3	GND	Ground
C4		
D1	C2P	Positive side of the external charge pump flying capacitor C2
D2	C1P	Positive side of the external charge pump flying capacitor C1
D3	PVDD	Boost charge pump output voltage
D4	VON	Negative audio output terminal

APPLICATION DIAGRAM

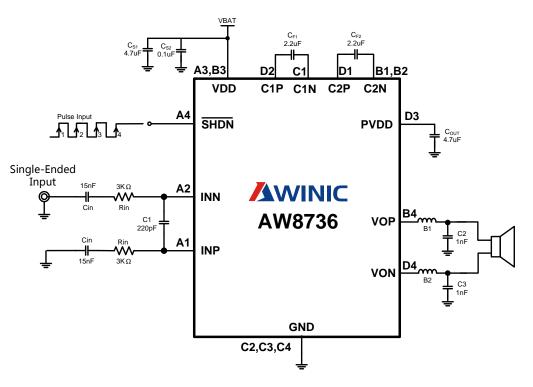


Figure 2 AW8736 single-ended input application diagram (Note 1)

Note1: when single-ended input, input audio signal can arbitrarily connect to one of INN, INP input terminal, the other terminal connects to ground through input capacitor and resistance.



Filter capacitor Cs suggest using X7R/X5R ceramic capacitors, if using tantalum capacitors, one ceramic capacitor greater than 1 uF must be placed near the VDD pin to filter high frequency interference signal.

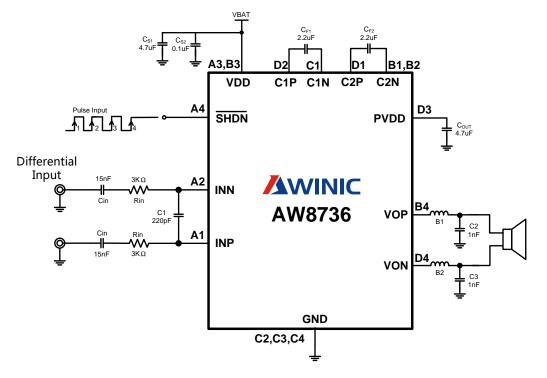
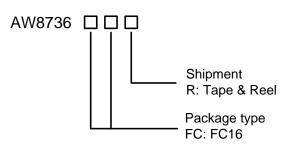


Figure 3 AW8736 differential input application diagram

ORDERING INFORMATION

Product Type	Operation temperature range	Package	Device Marking	Delivery Form
AW8736FCR	-40℃~85℃	FC-16	8736	Tape and Reel 3000 pcs





ABSOLUTE MAXIMUM RATING(Note2)

Parameter	Range				
Supply Voltage V _{DD}	-0.3V to 6V				
INP, INN Input Pin Voltage	-0.3V to V _{DD} +0.3V				
Package Thermal Resistance θ_{JA}	69°C/W				
Ambient Temperature Range	-40°C to 85°C				
Maximum Junction Temperature T _{JMAX}	125°C				
Storage Temperature Range T _{STG}	-65°C to 150°C				
Lead Temperature (Soldering 10 Seconds)	260°C				
ESD Rating (Note 3)					
HBM (human body model)	±6KV				
Latch-up					
Test Condition: JEDEC STANDARD NO.78B DECEMBER 2008	+IT: 450mA -IT: -450mA				

Note 2: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damageto the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Note 3: The human body model is a 100pF capacitor discharged through a $1.5k\Omega$ resistor into each pin. Test method: MIL-STD-883G Method 3015.7

MODE DESCRIPTION

AW8736 audio amplifier outer input capacitor is Cin, outer input resist is Rin, inner input resist is 16.5K Ω , gain Av is 320K/(Rin+16.5K). Recommended typical application is:

- 1、 Cin=15nF, Rin=3K Ω , Av=16.3V/V;
- 2, Cin=15nF, Rin=10K Ω , Av=12V/V;

Mode	Enable	Gain(V/V)		NCN Pov	NCN	
WOUE	Signal	Gain	•/•/	RL=8Ω	RL=4Ω	function
MODE1		16.3	12	1.2	2.25	\checkmark
MODE2		16.3	12	1	2	\checkmark
MODE3		16.3	12	0.8	1.6	\checkmark
MODE4		16.3	12	1.65W@THD=1%	2.15W@THD=1%	



ELECTRICAL CHARACTERISTICS

Test condition: $T_A=25^{\circ}C$ (unless otherwise noted)

Parameter		Test condition	S	Min	Тур	Max	Units
V_{DD}	Power supply voltage			3.0		5.0	V
V _{IH}	SHDN high input voltage			1.3		V _{DD}	V
VIL	SHDN low input voltage			0		0.35	V
V _{os}	Output offset voltage	Vin=0V, V_{DD} =3.0V to 5.0V		-30	0	30	mV
I_{SD}	Shutdown current	$V_{DD}=3.6V, \overline{SHDN}=0V$				1	μA
T_{TG}	Thermal AGC start temperature threshold				150		°C
T_{TGR}	Thermal AGC exit temperature threshold				130		Ĉ
T_{SD}	Over temperature protection threshold				160		ĉ
T_{SDR}	Over temperature protection recovery threshold				130		ĉ
T _{ON}	Start-up time				40		ms
K-Charg	epump						
PVDD	Output voltage	V_{DD} =3.0V to 3.8V			1.5* VDD		V
		V _{DD} >3.8V			5.8		V
Vhys	OVP hysteresis	V _{DD} >3.8V			50		mV
F_{CP}	Charge Pump frequency	V _{DD} =3.0V to 5.0V		0.8	1.06	1.33	MHz
η _{CP}	Charge pump efficiency	V _{DD} =4.2V, I _{load} =200mA			92		%
T _{ST}	Soft-start time	No load, COUT=4.7uF		1	1.2	1.4	ms
١L	Current limit when PVDD short to ground				350		mA
Class K	power amplifier (mode1-mode4	4)					
lq	Quiescent current	V _{DD} =3.6V, Vin=0, no load			9.5		mA
η	Efficiency	V_{DD} =4.2V, Po=1.2W, R _L =8 Ω			75		%
Fosc	Modulation frequency	V _{DD} =3.0V to 5.0V		600	800	1000	kHz
Av	gain	Outside input resistance=3kΩ			16.3		V/V
Rini	Inner input resistance				16.5		kΩ
		V_{DD} =4.2V, R _L =8 Ω			1.2		W
	Mode1 NCN output power	V_{DD} =4.2V, R_L =4 Ω			2.25		W
Pncn		V_{DD} =4.2V, R _L =8 Ω			1		W
	Mode2 NCN output power	V_{DD} =4.2V, RL=4 Ω			2		W
		V_{DD} =4.2V, RL=8 Ω		1	0.8		W
	Mode3 NCN output power	V_{DD} =4.2V, RL=4 Ω			1.6		W
PSRR	Power supply rejection ratio	V _{DD} =4.2V, Vp-p_sin=200mV	217Hz	-53	-65		dB



$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$			[
				1kHz	-53	-65		dB
$ \begin{array}{ c c c c c c c } \hline V_{00}=4.2V, \ \mbox{Po}=1.65W, \ \mbox{R}_{L}=8\Omega & 87.5 & dB \\ \hline Vn & Output noise voltage & VDD=4.2V, \ \mbox{Po}=202V, \ \mbox{f}=20Hz to 20kHz, \ \mbox{input ac grounded}} & A-weighting & 155 & uVrms \\ \hline THD+N & distortion+noise & V_{00}=4.2V, \ \mbox{Po}=4.2V, \ \mbox{Po}=4.2V, \ \mbox{R}_{L}=8\Omega, \ \mbox{f}=1kHz, \ \mbox{Mode}4 & 0.02 & \% \\ \hline V_{00}=4.2V, \ \mbox{Po}=1.2W, \ \mbox{R}_{L}=8\Omega, \ \mbox{Mode}4 & 0.02 & \% \\ \hline V_{00}=4.2V, \ \mbox{Po}=1.2W, \ \mbox{R}_{L}=8\Omega, \ \ \mbox{Mode}4 & 0.02 & \% \\ \hline V_{00}=4.2V, \ \mbox{Po}=1.2W, \ \mbox{R}_{L}=8\Omega, \ \ \mbox{Mode}4 & 0.02 & \% \\ \hline \ \ \mbox{Mode}4 \ \ \mbox{Mod}4 & 0.02 & \% \\ \hline \ \ \ \mbox{THD}+N=10\%, \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \$	SNR	Signal to poice ratio	$V_{\text{DD}}\text{=}4.2V, \text{ Po}\text{=}0.8W, \text{ R}_{\text{L}}\text{=}8\Omega$			84.5		dB
Vn Output noise voitage input ac grounded A-weighting 155 uVms THD+N Total harmonic distortion+noise V_{00} =4.2V, Po=1W, RL=80, f=1kHz, Mode1 0.02 % V_{00} =4.2V, Po=1.2W, RL=80, f=1kHz, Mode4 0.02 % V_{00} =4.2V, Po=1.2W, RL=80, V ₀₀ =4.2V 2.0 W THD+N=10%. f=1kHz. RL=80, V ₀₀ =4.2V 1.65 W THD+N=10%. f=1kHz. RL=80, V ₀₀ =4.2V 1.65 W THD+N=10%. f=1kHz. RL=80, V ₀₀ =3.6V 1.5 W THD+N=10%. f=1kHz. RL=80, V ₀₀ =3.6V 1.23 W THD+N=10%. f=1kHz. RL=80, V ₀₀ =4.2V 2.58 W THD+N=10%. f=1kHz. RL=40, V ₀₀ =4.2V 2.58 W THD+N=10%. f=1kHz. RL=40, V ₀₀ =3.6V 1.55 W TL SHDN high level duration time V ₀₀ =3.0V to 5.0V	SNIC	Signal-to-hoise ratio	$V_{\text{DD}}\text{=}4.2\text{V}, \text{ Po}\text{=}1.65\text{W}, \text{ R}_{\text{L}}\text{=}8\Omega$			87.5		dB
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Vn	Output noise voltage		A-weighting		155		uVrms
$ \begin{array}{ c c c c c c } \hline distortion+noise & V_{DD}=4.2V, Po=1.2W, R_L=8\Omega, f=1kHz, Mode4 & 0.02 & \% \\ \hline \\$		Total harmonic	V_{DD} =4.2V,Po=1W,R _L =8 Ω ,f=1kHz	,Mode1		0.02		%
$ P_{O} \begin{array}{cccccccccccccccccccccccccccccccccccc$		distortion+noise	V _{DD} =4.2V,Po=1.2W,R _L =8Ω,f=1kH	Hz,Mode4		0.02		%
$ P_{O} \begin{tabular}{ c c c c c c c c c c c c c c c c c c c$			THD+N=10%, f=1kHz, $R_L=8\Omega$,	V _{DD} =4.2V		2.0		W
$ P_{O} \ Mode4 \ output \ power \ Mode4 \ power \ mod4 \ power \ mod4 \ power \ mod4 \ power \ mod4 \ power \ power \ mod4 \ power \ po$			THD+N=1%, f=1kHz, $R_L=8\Omega$,	V _{DD} =4.2V		1.65		W
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$		Mode4 output power	THD+N=10%, f=1kHz, $R_L=8\Omega$, $V_{DD}=3.6V$			1.5		W
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	D		THD+N=1%, f=1kHz, $R_L=8\Omega$, $V_{DD}=3.6V$			1.23		W
$\begin{array}{ c c c c c c c c c c c c c c c c c c c$	Po		THD+N=10%, f=1kHz, R _L =4 Ω , V _{DD} =4.2V			2.58		W
$\begin{array}{ c c c c c c c c c c c c c c c c c c c$			THD+N=1%, f=1kHz, R_L =4 Ω , V_{DD} =4.2V			2.15		W
One wire pulse control T_H \overline{SHDN} high level duration time $V_{DD}=3.0V$ to $5.0V$ 0.75 2 10 us T_L \overline{SHDN} low level duration time $V_{DD}=3.0V$ to $5.0V$ 0.75 2 10 us T_{LATCH} \overline{SHDN} turn on delay time $V_{DD}=3.0V$ to $5.0V$ 150 500 us T_{OFF} \overline{SHDN} turn off delay time $V_{DD}=3.0V$ to $5.0V$ 150 500 us NCN (note 4) T_{AT} Attack time(-13.5dB) 40 ms T_{RL} Release time (13.5dB) 1.2 s			THD+N=10%, f=1kHz, R_L =4 Ω , V_{DD} =3.6V			1.85		W
T_H \overline{SHDN} high level duration time $V_{DD}=3.0V$ to $5.0V$ 0.75 2 10 us T_L \overline{SHDN} low level duration time $V_{DD}=3.0V$ to $5.0V$ 0.75 2 10 us T_{LATCH} \overline{SHDN} turn on delay time $V_{DD}=3.0V$ to $5.0V$ 150 500 us T_{OFF} \overline{SHDN} turn off delay time $V_{DD}=3.0V$ to $5.0V$ 150 500 us NCN (note 4) T_{AT} Attack time(-13.5dB) 40 ms T_{RL} Release time (13.5dB) 1.2 s			THD+N=1%, f=1kHz, $R_L=4\Omega$,	V _{DD} =3.6V		1.55		W
TL SHDN low level duration time V_{DD} =3.0V to 5.0V 0.75 2 10 us T_LATCH SHDN turn on delay time V_{DD} =3.0V to 5.0V 150 500 us T_OFF SHDN turn off delay time V_{DD} =3.0V to 5.0V 150 500 us NCN (note 4) TAT Attack time(-13.5dB) Image: Comparison of the state of the sta	One wire	e pulse control			•		•	
TLATCH SHDN turn on delay time V_{DD} =3.0V to 5.0V 150 500 us T_OFF SHDN turn off delay time V_{DD} =3.0V to 5.0V 150 500 us NCN (note 4) TAT Attack time(-13.5dB) 40 ms T_RL Release time (13.5dB) 1.2 s	Т _н	SHDN high level duration time	V _{DD} =3.0V to 5.0V		0.75	2	10	us
TOPE SHDN turn off delay time VDD=3.0V to 5.0V 150 500 us NCN (note 4) TAT Attack time(-13.5dB) 40 ms T_{RL} Release time (13.5dB) 1.2 s	T∟	SHDN low level duration time	V _{DD} =3.0V to 5.0V		0.75	2	10	us
NCN (note 4) 40 ms T _{AT} Attack time(-13.5dB) 1.2 s T _{RL} Release time (13.5dB) 1.2 s	TLATCH	SHDN turn on delay time	V _{DD} =3.0V to 5.0V		150		500	us
T _{AT} Attack time(-13.5dB) 40 ms T _{RL} Release time (13.5dB) 1.2 s	T_{OFF}	SHDN turn off delay time	V _{DD} =3.0V to 5.0V		150		500	us
T _{RL} Release time (13.5dB) 1.2 s	NCN (note 4)							
	T _{AT}	Attack time(-13.5dB)				40		ms
A _{MAX} Maximum attenuation -13.5 dB	T_{RL}	Release time (13.5dB)				1.2		S
	A _{MAX}	Maximum attenuation				-13.5		dB

Note 4: Attack time points to 13.5dB gain attenuation time; Release time points to 13.5dB gain recovery time.

MEASUREMENT SYSTEM

AW8736 features switching digital output, as shown in Figure 4. Need to connect a low pass filter to VOP/VON output respectively to filter out switch modulation frequency, then measure the differential output of filter to obtain analog output signal.

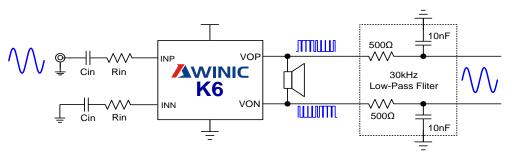


Figure 4 AW8736 test setup

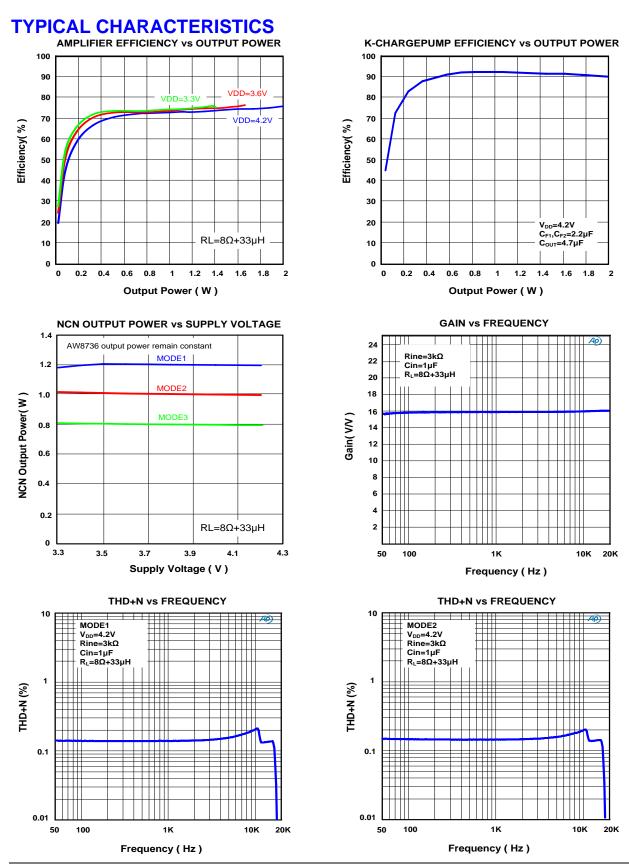


Low pass filter uses resistance and capacitor values listed in Table 2.

R _{filter}	C _{filter}	Low-pass cutoff frequency
500Ω	10nF	32kHz
1kΩ	4.7nF	34kHz

Table 2 AW8736 recommended values for low pass filter

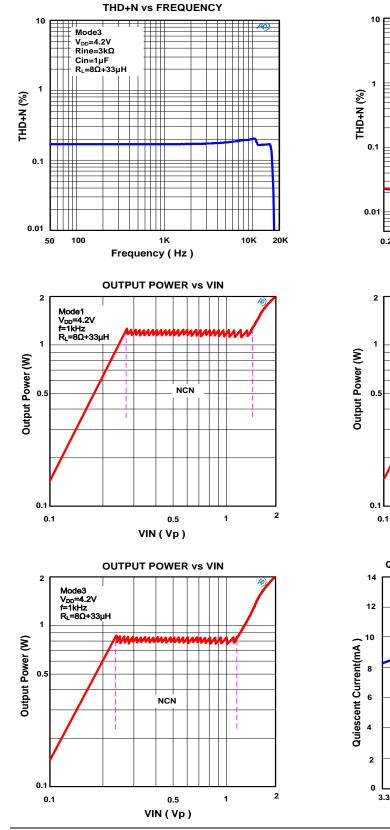


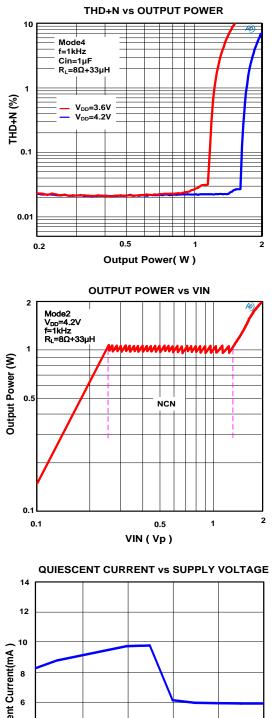


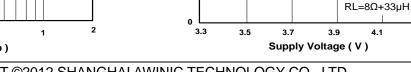


4.3

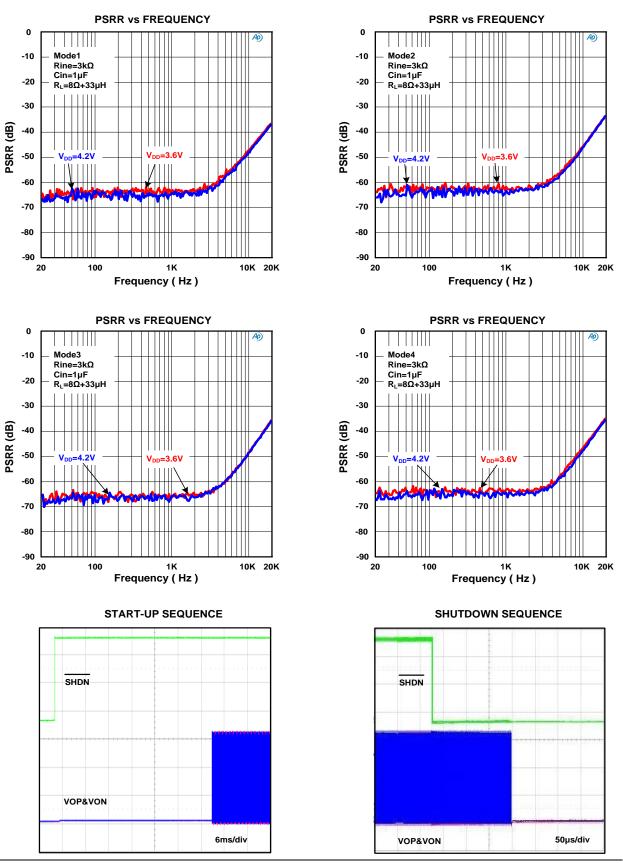
High efficiency、Ultralow distortion、Constant large volume、Sixth generation Class K Audio Amplifier



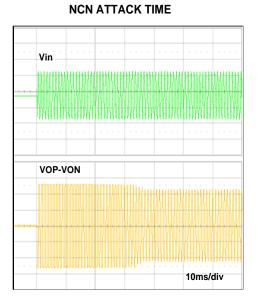




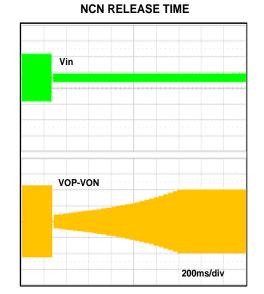


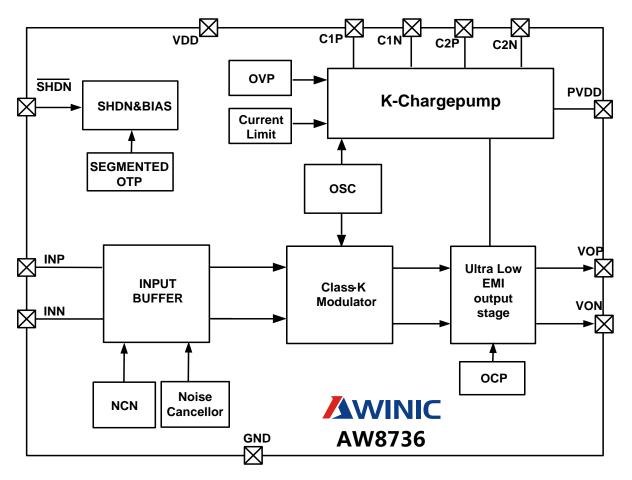






FUNCTIONAL DIAGRAM









OPERATION

AW8736 is designed to enhance smart mobile phone sound quality, which is a new high efficiency, ultra-low distortion, constant large volume, sixth generation class K audio amplifiers. Using a new generation of charge pump technology: K -Chargepump structure, built in current limiting control loop and over-voltage-protection(OVP) loop, efficiency as high as 92%, power amplifier's overall efficiency reaches 75%, greatly prolong the mobile phone usage time. 0.02% of the ultra-low distortion and unique non-crack-noise (NCN) technology brings high quality music enjoyment.

AW8736 integrated K-Chargepump booster circuit, the output power cannot drop along with lithium battery voltage lower down. Within lithium battery voltage range(3.3 V - 4.35V), output power is constant, providing high quality music enjoyment. AW8736 has 0.8 W, 1 W and 1.2 W three output power level, recommended using rated power of 0.7W and above speakers, which greatly improve the volume, and effectively protect speakers.

The AW8736 uses awinic proprietary TDD-Noise suppression technology and EMI suppression technology, effectively restrain TDD-Noise and EMI interference.

AW8736 built-in over current protection, over-temperature protection and short circuit protection function, effectively protect the chip. The AW8736 uses small 2mmx2mm FC-16 package. The AW8736 is specified over the industrial temperature range of -40 $^{\circ}$ C to 85 $^{\circ}$ C.

CONSTANT OUTPUT POWER

In the mobile phone audio applications, the NCN function to promote music volume and quality is very attractive, but as the lithium battery voltage drops, general power amplifier output power will reduce gradually, leads to smaller and smaller music volume. So, it is hard to provide high quality music within the battery voltage range. The AW8736 uses unique second generation NCN technology, within lithium battery voltage range(3.3 V - 4.35V), output power is constant, the output power cannot drop along with lithium battery voltage lower down. Even if the battery voltage drops, AW8736 can still provide high quality large volume music enjoyment. There are four AW8736 operation modes, first three modes have NCN function, the output power level is 1.2W,1W,0.8W,respectively.

Second Generation NCN technology

In audio application, output signal will be undesirable distortion caused by too large input and power supply voltage down with battery, and clipped output signal may cause permanent damage to the speaker. The traditional NCN function adjusts system gain automatically to generate desired output by detecting the "Crack" distortion of output signal, makes the output audio signal maintain smooth, not only can effectively avoid overloading output power to the damage of speaker, at the same time bring the constant shock of high quality music enjoyment. The traditional NCN function is shown below in figure 6.



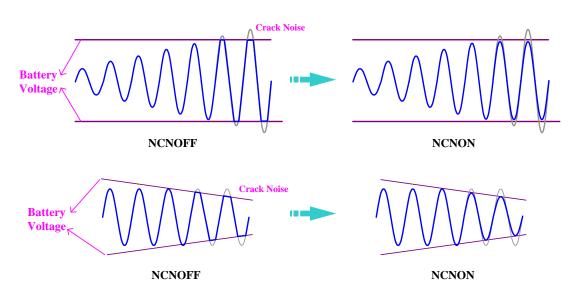


Figure 6 Traditional NCN Operation Principle

AW8736 adopts Awinic unique second generation NCN technology, the output signal is free from limitation of power rail. When battery voltage drops, NCN output signal will not distort, output amplitude remains unchanged, keeping constant output power, as shown in figure 7. Even if the battery voltage drops, AW8736 can still provide high quality large volume music enjoyment.

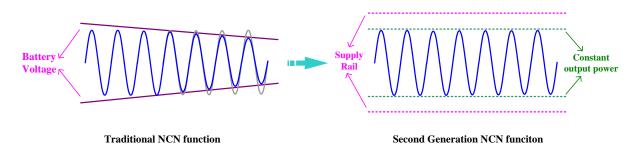


Figure 7 Second generation NCN Operation Principle

Attack time

Attack time is the time it takes for the gain to be attenuated -13.5dB once the audio signal exceeds the NCN threshold. Fast attack times allow the NCN to react quickly and prevent transients such as symbol crashes from being distorted. However, fast attack times can lead to volume pumping, where the gain reduction and release becomes noticeable, as the NCN cycles quickly. Slower attack times cause the NCN to ignore the fast transients, and instead act upon longer, louder passages. Selecting an attack time that is too slow can lead to increased distortion in the case of the No Clip function. According to mobile phone and portable equipment audio features, attack time of AW8736 is set to be 40ms, effectively keeping the music rhythm, and at the same time eliminating the crack distortion, protecting the speaker.



Release time

Release time is the time it takes for the gain to return to its normal level once the audio signal returns below the NCN threshold. A fast release time allows the NCN to react quickly to transients, preserving the original dynamics of the audio source. However, similar to a fast attack time, a fast release time contributes to volume pumping. A slow release time makes the music smooth and soft, it is better to suppress the crack distortion, but longer release time will make music sounds "boring", lack of impact. According to mobile phone and portable equipment audio features, release time of AW8736 is set to be 1.2s.

K-Chargepump

AW8736 adopts a new generation of charge pump technology: K -Chargepump structure, it has high efficiency and large driving ability, working frequency is 1.1MHz, built in soft start circuit, current limiting control loop and over-voltage-protection(OVP) loop, guaranteeing system stable and reliable operation.

High Efficiency

AW8736 uses K-chargepump structure, booster output voltage PVDD is 1.5 times of supply voltage VDD, the ideal efficiency can reach 100%. K-chargepump efficiency is the ratio of output power to input power, that is

$$\eta = \frac{P_{OUT}}{P_{IN}} * 100\%$$

For example, in an ideal M times chargepump, the input current I_{IN} is M times of output current I_{OUT} , the efficiency formula can be written as:

$$\eta = \frac{P_{OUT}}{P_{IN}} * 100\% = \frac{V_{OUT} * I_{OUT}}{V_{IN} * M * I_{OUT}} * 100\% = \frac{V_{OUT}}{M * V_{IN}} * 100\%$$

M is charge pump work mode variable (1.5 times), VOUT is charge pump output voltage, VIN is power supply voltage, IOUT is load current. For K-chargepump, the output voltage is 1.5 times of the input voltage, the ideal charge pump efficiency is 100%, due to the charge pump internal switch loss and IC static current loss, the actual efficiency will be less than ideal efficiency, up to 92%. Therefore, K-chargepump booster technology can greatly improve the power efficiency.

Charge Pump Structure

Figure 8 is charge pump basic principle diagram, the charge pump used in AW8736 has seven switches, the output voltage PVDD is 1.5 times as input voltage VDD through seven switches timing control.



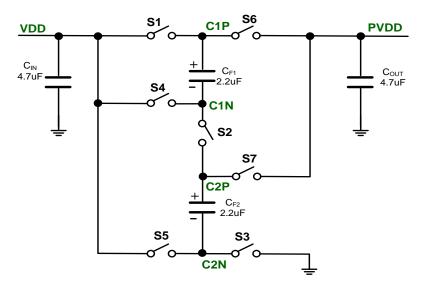


Figure 8 Charge Pump Principle Diagram

The operation of the charge pump has two phases, as shown in figure 9. In Φ 1, swtiches S1, S2 and S3 are closed, VDD charges to the flying capacitor CF1 CF2.

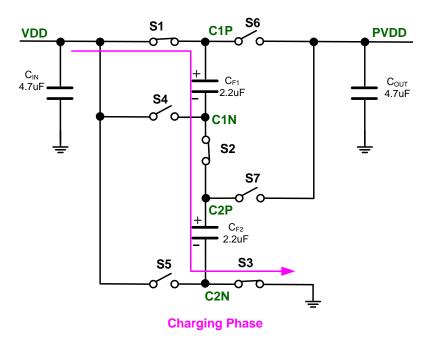


Figure 9 01: Flying Capacitor Charging

In Φ 2, as shown in figure 10: switches S1, S2 and S3 are disconnected, switches S4, S5, S6 and S7 are closed. Because the voltage across the capacitor can't mutation, so the voltage on flying capacitor CF1 CF2, is added to the VDD, which make PVDD risen to a higher voltage.



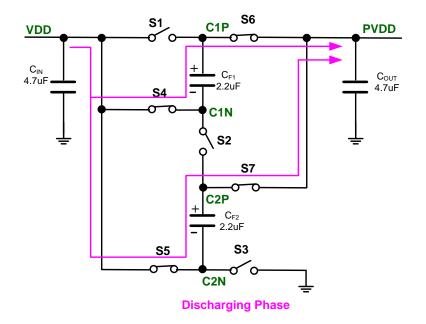


Figure 10 Φ2: Flying capacitor charge transfer to the output capacitance C_{OUT}

Soft start

K-chargepump has integrated soft start function in order to limit supply power inrush current during start-up. The supply current is limited to be 350 mA, and the soft start time is 1.2 ms.

Current Limitation Control

K-chargepump has integrated the current limitation control loop. In normal operation, when the heavy load or a situation that make charge pump flow through very large current, the current limitation control loop will control charge pump maximum output current capacity, that is 1.5 A;

Over Voltage Protection(OVP)Control

K-chargepump's output voltage PVDD is a multiple of the input voltage VDD, which provide a high voltage rail for internal power amplifier circuits, allowing the amplifiers provide greater output dynamic range in the lithium battery voltage range, so as to realize the large volume, high quality class K audio enjoyment. K-chargepump has integrated the over voltage protection control loop, when the input voltage VDD is greater than 3.8V, the output voltage PVDD is no longer a multiple of VDD, but is controlled by over voltage protection(OVP) loop and is stable in 5.8V, and the hysteresis voltage is about 50mV.

One-wire pulse control

One wire pulse control technology only needs a single GPIO port to operate the chip, complete a variety of functions, it is very popular in the area of the GPIO port shortage and portable systems.

When the control signal line is longer, because of the signal integrity or radio frequency interference problem, it will produce the narrow glitch signal. Awinic one wire pulse control technology integrated the Deglitch circuit in internal control pin, which can effectively eliminate the influence of the glitch signal, as



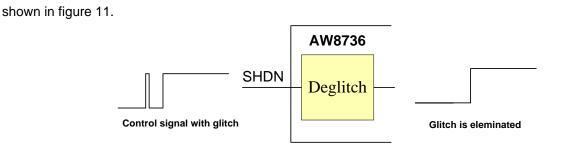


Figure 11 Awinic Deglitch function diagram

The traditional one wire pulse control technology still receives pulse signal from control port when chip is startup, so when the master control chip (such as mobile phone BB) sends wrong pulse during normal operation, the system will enter into error states. AW8736 uses one wire pulse latch technology, after the master control chip has sent pulses, the state will be latched, no longer receive the latter mis-sending pulse signals, as shown in figure 12.

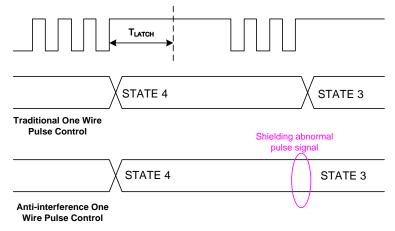


Figure 12 Anti-interference One Wire Pulse Control Function Diagram

One Wire Pulse Control

AW8736 select each mode through the detection of number of the pulse signal rising edge of SHDN pin, as shown in figure 13: When SHDN pin pull high from shutdown mode, there is only a rising edge, AW8736 enter into mode 1,NCN output power is 1.2W; When high-low-high signal set to SHDN pin, there are two rising edges, AW8736 enter into mode 2, NCN output power is 1W; When there are three rising edges, AW8736 enter into mode 3,NCN output power is 0.8W; When there are four rising edges, AW8736 enter into mode 4,NCN function is turned off; AW8736 has four operation modes, the number of the rising edges does not allow more than four.



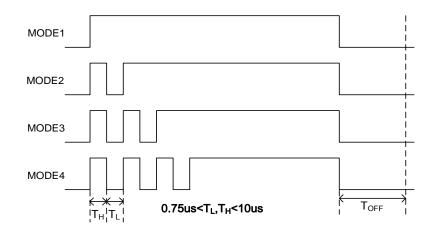


Figure 13 One Wire Pulse Control

When AW8736 needs to work in different mode, PIN SHDN should be pull low longer than T_{OFF} first(recommended 1ms) which make the AW8736 shut down, Then send series pulse make the AW8736 enter into right mode, as shown in figure 14.

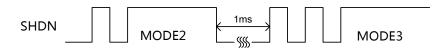


Figure 14 One Wire Pulse Control Switching Sequence

RNS(RF TDD Noise Suppression)

GSM radios transmit using time-division multiple access with 217Hz intervals. The result is an RF signal with strong amplitude modulation at 217Hz and its harmonics that is easily demodulated by audio amplifiers.

In RF applications, improvements to both layout and component selection decrease the AW8736's susceptibility to RF noise and prevent RF signals from being demodulated into audible noise. Minimizing the trace lengths prevents them from functioning as antennas and coupling RF signals into the AW8736. Additional RF immunity can also be obtained from relying on the self-resonant frequency of capacitors as it exhibits the frequency response similar to a notch filter. Depending on the manufacturer, 10pF to 20pF capacitors typically exhibit self resonance at RF frequencies. These capacitors, when placed at the input pins, can effectively shunt the RF noise at the inputs of the AW8736. For these capacitors to be effective, they must have a low-impedance, low-inductance path to the ground plane.

Some RF energy will couple onto audio traces regardless of the effort to prevent this phenomenon from occurring, form audible TDD Noise. The AW8736 features a unique RNS technology, which effectively reduces RF energy, attenuate the RF TDD-noise, an acceptable audible level to the customer.



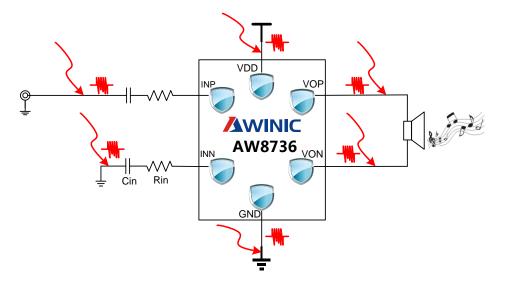


Figure 15 RF Radiation coupling schematic diagram

Filter-Free Modulation Scheme

The AW8736 features a filter-free PWM architecture that reduces the LC filter of the traditional Class-D amplifier, increasing efficiency, reducing board area consumption and system cost.

EEE

The AW8736 features a unique Enhanced Emission Elimination (EEE) technology, that controls fast transition on the output, greatly reduces EMI over the full bandwidth.

Pop-Click Suppression

The AW8736 features unique timing control circuit, that comprehensively suppresses pop-click noise, eliminates audible transients on shutdown, wakeup, and power-up/down.

Protection Function

When a short-circuit occurs between VOP/VON pin and VDD/GND or VOP and VON, the over-current circuit shutdown the device, preventing the device from being damaged. When the condition is removed, the AW8736 reactivate itself. When the junction temperature is high, the over-temperature circuit shutdown the device. The circuit switches back to normal operation when the temperature decreases to safe levels.



APPLICATION INFORMATION

External Input Resistor-Rine (Gain setting)

The AW8736 is a differential audio amplifier. The IC integrates two internal input resistors, which is R_{ini} =16.5k Ω . Take external input resistor R_{ine} =3k Ω for an example, gain setting as follows:

$$A_{V} = \frac{320k\Omega}{R_{ine} + R_{ini}} = \frac{320k\Omega}{3k\Omega + 16.5k\Omega} = 16.3V/V$$

Input Capacitor-C_{in} (input high-pass cutoff frequency)

The input coupling capacitor blocks the DC voltage at the amplifier input terminal. The input capacitors and input resistors form a high-pass filter with the corner frequency:

$$f_{H}(-3dB) = \frac{1}{2*\pi*R_{intotal}*C_{in}}(Hz)$$

Setting the high-pass filter point high can block the 217Hz GSM noise coupled to inputs. Better matching of the input capacitors improves performance of the circuit and also helps to suppress pop-click noise.

Take typical application in Figure 2 as an example:

$$f_{\rm H}(-3{\rm dB}) = \frac{1}{2*\pi*R_{\rm intotal}*C_{\rm in}}({\rm Hz}) = \frac{1}{2*\pi*19.5{\rm k}\Omega*15{\rm nF}}({\rm Hz}) = 544{\rm Hz}$$

Supply Decoupling Capacitor (C_s)

The AW8736 is a high-performance audio amplifier that requires adequate power supply decoupling. Place a low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1µF. This choice of capacitor and placement helps with higher frequency transients, spikes, or digital hash on the line. Additionally, placing this decoupling capacitor close to the AW8736 is important, as any parasitic resistance or inductance between the device and the capacitor causes efficiency loss. In addition to the 0.1µF ceramic capacitor, place a 10µF capacitor on the VBAT supply trace. This larger capacitor acts as a charge reservoir, providing energy faster than the board supply, thus helping to prevent any droop in the supply voltage.

Flying Capacitor (C_F)

The value of the flying capacitor (C_F) affects the load regulation and output resistance of the charge pump. A C_F value that is too small degrades the device's ability to provide sufficient current drive. Increasing the value of C_F improves load regulation and reduces the charge pump output resistance to an extent. A 2.2µF@10V capacitor is recommended.



Output Capacitor (C_{OUT})

The output capacitor value and ESR directly affect the ripple at PVDD. Increasing C_{OUT} reduces output ripple. Likewise, decreasing the ESR of C_{OUT} reduces both ripple and output resistance. A 4.7 μ F@10V capacitor is recommended.

Optional Ferrite Bead Filter

The AW8736 passed FCC and CE radiated emissions with no ferrite chip beads and capacitors. Use ferrite chip beads and capacitors if device near the EMI sensitive circuits and/or there are long leads from amplifier to speaker, placed as close as possible to the output pin.

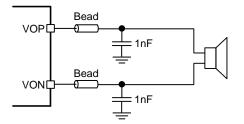
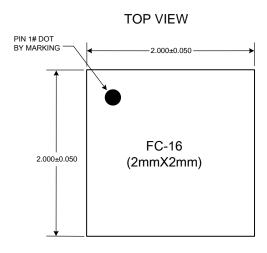


Figure 16 Ferrite Chip Bead and capacitor



PACKAGE DESCRIPTION

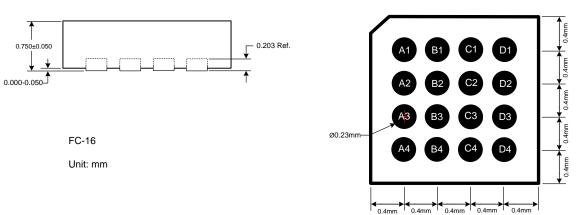


0.400 Bsc PIN 1# DENTIFICATION D.400 Bsc O D.400 Bsc O

BOTTOM VIEW

SIDE VIEW

PAD Dimention





VERSION INFORMATION

Version	Description	Owner	Date
V0.9	AW8736FCR datasheet preliminary	Zhanghaijun	2012-10-31
V1.0	AW8736FCR datasheet released	Zhanghaijun	2012-11-30
V1.1	Add SNR characteristics	Zhanghaijun	2013-01-05
V1.2	Add 12V/V gain mode description and add PA output power under 40hm load condition	Zhanghaijun	2013-02-22
V1.3	Add footmark on Bonding pad figure	Zhanghaijun	2013-03-29
V1.4	 Change the output capacitor C_{OUT} maximum voltage to 10V; Add charge pump efficiency test condition; Add charge pump operation frequency; Change the cell phone operation voltage range as 3.3V~4.35V; Change the K-chargepump part description(Page14); 	Zhanghaijun	2013-04-19
V1.5	Highlight AW8736 pin number in Page 1	Zhanghaijun	2013-05-21

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