USB Dedicated Charging Port Controller with QC 2.0 Fast Charging Function

Description

The FP6600 is a fast charge protocol controller and follows Quick Charge 2.0 specification for smart power bank application. The protocol feature monitors USB D+/D- data line voltage, and automatically adjusts output voltage of power bank and wall adaptor to optimize charge time.

FP6600 is a high performance solution for fast-charging mechanism and it saves charging time. It supports the full output voltage range of either Class A or Class B. Optionally Class B can be inhibited for protecting the battery charger from accidental damage.

FP6600 can support not only USB BC compliant devices, but also Apple / Samsung devices and automatically detects whether a connected powered device (PD) is Quick Charge 2.0 capable before enabling output voltage adjustment. If a PD not compliant to Quick Charge 2.0 is detected the FP6600 disables output voltage adjustment to ensure safe operation with legacy 5 V only USB PDs.

The FP6600 is available in a space-saving SOP-8.

Features

- Input Voltage Range from 4V to 6V.
- Fully Supports Quick Charge 2.0 specification:
  - Class A: 5V/9V/12V Output Voltage.
  - Class B : 5V/9V/12V/20V Output Voltage.
- Supports USB DCP Shorting D+ Line to D- Line per USB Battery Charging Specification, Revision 1.2.
- Meets Chinese Telecommunication Industrial Standard YD/T 1591-2009
- Supports USB DCP applying 2.7V on D+ line and 2.7V on D- line.
- Supports USB DCP applying 1.2V on D+ and D- lines
- Automatic selection of D+/D- mode for an attached device
- Complaint with Apple® and Samsung devices
- SOP-8 Pb-Free Package

Applications

- Wall-Adapter / Power Plugs, Outlets
- Mobile / Tablet Power Bank
- Car Charger
- USB Power Output Ports

Pin Assignments

SO Package(SOP-8)

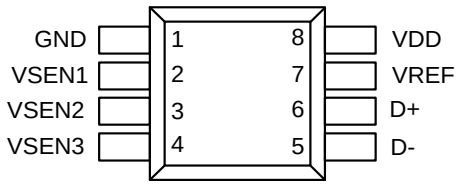
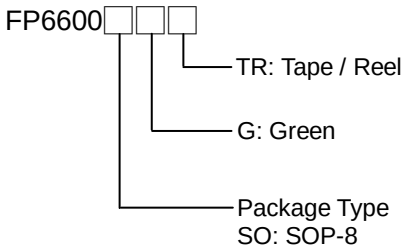


Figure 1. Pin Assignment of FP6600

Ordering Information



Typical Application Circuit

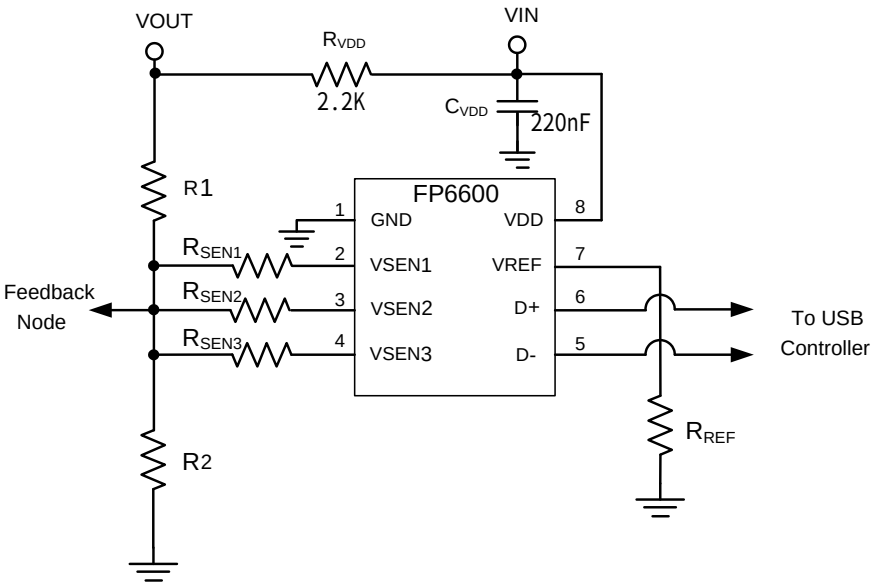


Figure 2. Typical Application Schematic

Output Voltage Lookup Table

D+	D-	Output Voltage	Internal Switch Setting		
			SW1	SW2	SW3
3.3V	3.3V	20V	0	0	0
0.6V	0.6V	12V	0	0	1
3.3V	0.6V	9V	0	1	1
0.6V	GND	5V (Default)	1	1	1

Note:1 represent the NMOS are OFF, 0 represent the NMOS are ON.

Functional Pin Description

Pin Name	Pin No. (SOP-8)	Pin Function
GND	1	Ground Pin.
VSEN1	2	Open Drain Output of output voltage adjustment switch. Active for 9V, 12V, 20V output setting.
VSEN2	3	Open Drain Output of output voltage adjustment switch. Active for 12V, 20V output setting.
VSEN3	4	Open Drain Output of output voltage adjustment switch. Active for 20V output setting.
D-	5	USB D- data line input
D+	6	USB D+ data line input
VREF	7	Internal Reference Voltage Output Pin. It must be with a resistor to GND
VDD	8	Power Supply Input Pin.

Block Diagram

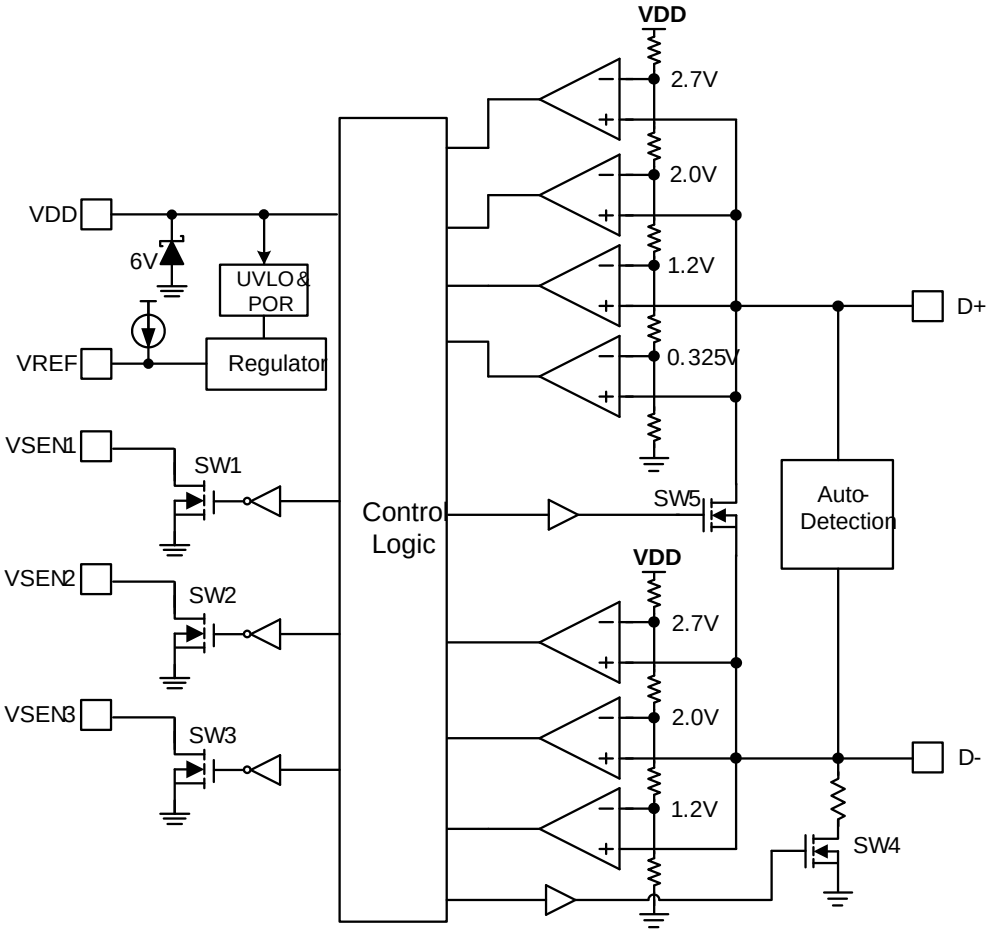


Figure 3. Block Diagram of FP6600

Absolute Maximum Ratings

- Input Supply Voltage VDD ---------- - 0.3V to + 8V
- All Other Pins Voltage ---------- - 0.3V to + 8V
- Maximum Junction Temperature (T_J)---------- + 150℃
- Storage Temperature (T_S)---------- - 65℃ to + 150℃
- Lead Temperature (Soldering, 10sec.) ---------- +260°C
- Power Dissipation @T_A=25℃, (P_D)

  SOP-8 ---------- 1.39W
- Package Thermal Resistance, (θ_{JA}):

  SOP-8---------- 90°C/W
- Package Thermal Resistance, (θ_{JC}):

  SOP-8---------- 39°C/W

Note1：Stresses beyond those listed under “Absolute Maximum Ratings" may cause permanent damage to the device.

Recommended Operating Conditions

- Input Supply Voltage (VDD)---------- 4V ~ 6V
- Operation Temperature Range (T_{OPR}) ---------- -40°C to +85°C

Note：Over operating free-air temperature range (unless otherwise noted)

Electrical Characteristics

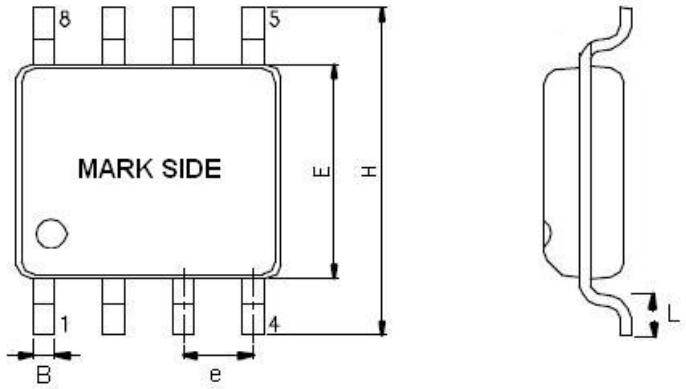
(VDD=5V, T_A=25℃ and the recommended supply voltage range, unless otherwise specified.)

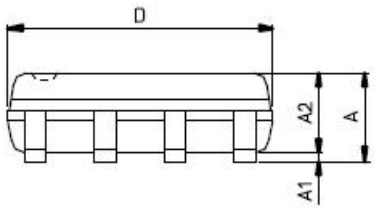
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Power						
VDD Input Voltage Range	V_{DD}		4		6	V
Input UVLO Threshold	$V_{UVLO(VTH)}$	V_{DD} Rising	2.0		3.9	V
VDD Supply Current		VDD=5V, Measure $V_{DD,}$ SW1 = SW2 = SW3 = Off		200		μA
VDD Shunt Voltage	$V_{DD(SHUNT)}$		TBD	TBD	TBD	V
Reference Voltage Output	V_R		1.18	1.23	1.28	V
High Voltage Dedicated Charging Port (HVDCP)						
20 V Output Inhibit Threshold	V_{DDH}		V_{DD}-0.6			V
Data Detect Voltage	$V_{DAT(REF)}$		0.25	0.325	0.4	V
Output voltage selection reference	V_{SEL_REF}		1.8	2.0	2.2	V
Data Lines Short-Circuit Delay	$T_{DAT(SHORT)}$	VOUT ≥ 0.8 V		10	20	ms
D+ High Glitch Filter Time	$T_{GLITCH(BC)-D+\_H}$		1000	1250	1500	ms
D- Low Glitch Filter Time	$T_{GLITCH(BC)-D-\_L}$		1			ms
Output Voltage Glitch Filter Time	$T_{GLITCH(V)CHANGE}$		20	40	60	ms
D- Pull-Down Resistance	$R_{D-(DWN)}$			20		KΩ
Switch SW1 on-resistance	$R_{DS\_ON\_N1}$	SW1 = 200μA			300	Ω
Switch SW2 on-resistance	$R_{DS\_ON\_N2}$	SW2 = 200μA			300	Ω
Switch SW3 on-resistance	$R_{DS\_ON\_N3}$	SW3 = 200μA			300	Ω
Switch SW5 on-resistance	$R_{DS\_ON\_N5}$	SW5 = 200μA			40	Ω
DCP 1.2V Charging Mode						
$D+_{\_1.2V}$/$D-_{\_1.2V}$ line output voltage			1.08	1.2	1.32	V
$D+_{\_1.2V}$/$D-_{\_1.2V}$ line output Impedance				58		KΩ
Apple 2.4A Mode						
$D+_{\_2.7V}$/$D-_{\_2.7V}$ line output voltage			2.57	2.7	2.84	V
$D+_{\_2.7V}$/$D-_{\_2.7V}$ line output Impedance				33.6		KΩ

Note ：Not production tested.

Outline Information

SOP-8 Package (Unit: mm)

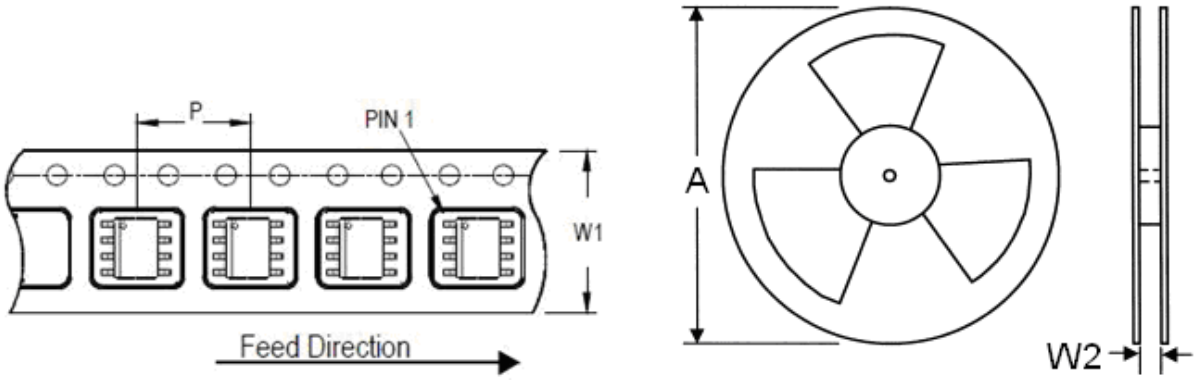




SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
A2	1.25	1.50
B	0.31	0.51
D	4.80	5.00
E	3.80	4.00
e	1.20	1.34
H	5.80	6.20
L	0.40	1.27

Note：Followed from JEDEC MO-012-E

Carrier dimensions



Tape Size (W1) mm	Pocket Pitch (P) mm	Reel Size (A)		Reel Width (W2) mm	Empty Cavity Length mm	Units per Reel
		in	mm			
12	8	13	330	12.4	400~1000	2,500

Life Support Policy

Fitipower's products are not authorized for use as critical components in life support devices or other medical systems.