

Fast Charging Physical Layer IC for USB Interfaces

Supports 10 standards: Type-C, QC3.0/QC2.0, FCP, AFC, SFCP, MTK PE+ 2.0/1.1, Apple 2.4A, BC1.2

1. Features

- Support two USB ports charging control
 - DP1,DM1 support several fast charging of: QC3.0/QC2.0, FCP, AFC, SFCP, MTK PE+ 2.0/1.1 and Apple[®] 2.4A, Samsung[®] 2.0A, BC1.2
 - DP2,DM2 support Apple[®] 2.4A, Samsung[®] 2.0A, BC1.2
- Support USB Type-C DRP controller
 - > Auto-detect USB connection condition
 - Auto-detect USB line direction and role
 - ID1/ID2 pin will enable the power rail after negotiate successfully
 - SEL2 support configure the port as DFP,UFP or DRP
- Support QC3.0&QC2.0 Class B (Compatible with Class A)
 - QC3.0 Class B: 3.6V~20V (0.2V/step) output voltage
 - QC2.0 Class B: 5 V, 9 V, 12 V or 20V
- Support MTK PE+ 2.0/1.1
- PE+ 2.0: 5V~20V (0.5V/Step)
- > PE+ 1.1: 3.6V~5V (0.2V/Step), 7V, 9V or 12V
- Support Huawei[®] FCP of 5V and 9V
- Support Samsung[®] AFC of 5V and 9V
- Support Spreadtrum[®] SFCP of 12V, 9V and 5V
- Support Apple[®] 2.4A: DP=2.7V, DM=2.7V
- Support Samsung[®] 2.0A: DP=1.2V, DM=1.2V
- Support BC1.2: Automatic shorting D+ to D- line
- SEL1 configure the maximum voltage, allowed to applied for, as 20V or 12V or 5V
- Default 5 V mode operation
- Support auto-detect and auto-switching fast charging standards
- Support NTC temperature protect function
- Support auto-detect NTC and MTK function
- FB for voltage regulation
- Support NTC temperature protect function
- Support auto-detect NTC and MTK function
- Working voltage: 3V~5.5V
- Very low power consumption I_Q = 66uA(Typ.)
- Package: DFN16

2. Typical Applications

- USB power output ports for AC adapters, Power Banka, Car chargers
- Battery chargers for smart phones, tablets, netbooks, digital cameras, and Bluetooth accessories

3. Description

IP2707 is a low-cost fast charging Physical Layer IC dedicated for USB ports, which supports 10 kinds of fast charging standards, including Type-C DFP, HVDCP QC3.0/QC2.0 (Quick Charge) Class A&B, FCP (Hisilicon® Fast Charge Protocol), AFC (Samsung® Adaptive Fast Charge), SFCP (Spreadtrum® Fast Charge Protocol), MTK PE+ 2.0/1.1 (MediaTek Pump Express Plus 2.0/1.1), Apple® 2.4A, BC1.2 and Samsung® 2.0A.

IP2707 integrated USB Type-C DRP port controller, which can be configured as DFP, UFP or DRP mode, and can co-work with Type-C UFP/DFP/DRP devices.

IP2707 support two USB ports charging control, in which DP1, DM1 support several charging standards. DP2, DM2 support Apple[©] 2.4A, Samsung[©] 2.0A and BC1.2.

IP2707 support automatically detecting the connected device's type and switching standards type to responding for fast charging requirements.

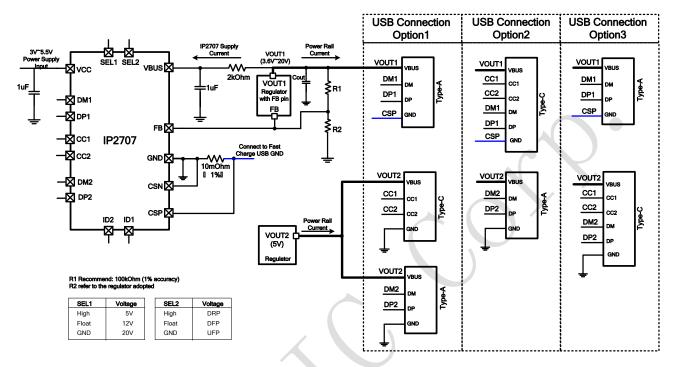
FB control line is integrated to source/sink current with precise 2uA/step in minimum, for accurate voltage regulation.

Support NTC over temperature protect function

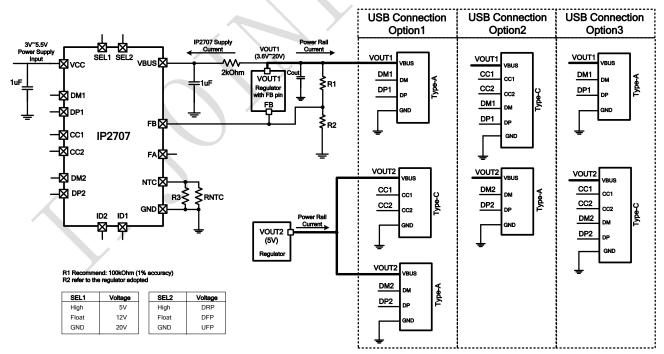


4. Typical Application Schematic

Pin 3, Pin 14 used as CSN and CSP:

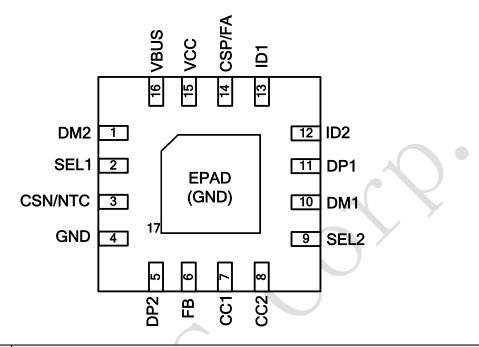


Pin 3, Pin 14 used as NTC and FA:





5. PIN Description



Pin Name	Pin No.	Pin Description
DM2	1	Connect to USB DM data line
SEL1	2	 Configure the maximum voltage allowed to apply for: V_{SELH} for 5V output Floating for 12V output GND for 20V output
CSN/NTC	3	 This pin is multiplexed as CSN and NTC two functions: 1) CSN: current detect negative pin. In MTK PE+ 2.0/1.1 mode, this pin is connected to the IC's GND pin. A resistor of 10mOhm (1%) should be applied between IC's GND pin and USB port's GND. In this condition, NTC function is disabled automatically 2) NTC: temperature sensitive resistor detect pin. In NTC mode, this pin connect to paralleled RNTC and R3 resistors to GND, MTK PE+ 2.0/1.1 function is disabled automatically. The resistor of 10mOhm (1%) between IC's GND and USB port's GND can be eliminated When neither of these two functions are needed, CSN,CSP pins left floating, IC's GND and USB port's GND are connected together
GND	4	Ground
DP2	5	Connect to USB DP data line
FB	6	Connect to the Regulator's FB line, current source/sink for voltage regulation
CC1	7	Connect to USB Type-C CC1 pin
CC2	8	Connect to USB Type-C CC2 pin
SEL2	9	Configure the Type-C Device's mode: • High: DRP



		Float: DFP
		• GND: UFP
DM1	10	Connect to USB DM data line
DP1	11	Connect to USB DP data line
ID2	12	Type-C UFP mode power rail control pin
ID1	13	Type-C DFP mode power rail control pin
CSP/FA	14	 This pin is multiplexed as CSP and FA two functions: when pin 3 is CSN function, this pin is CSP; when pin 3 is NTC, this pin is FA. 1) CSP: current detect positive pin. In MTK PE+ 2.0/1.1 mode, this pin is connected to USB port's GND. A resistor of 10mOhm (1%) should be applied between IC's GND pin and USB port's GND. In this condition, NTC function is disabled automatically 2) FA: abnormal temperature flag. In NTC mode, the resistor of 10mOhm (1%) between IC's GND and USB port's GND can be eliminated. When neither of these two functions are needed, CSN,CSP pins left floating, IC's GND and USB port's GND are connected together
VCC	15	Power supply input, apply 1uF capacitor to GND. When applying in adaptor and other DFP devices, no low power mode, VCC can be floating.
VBUS	16	Power supply input, connect with 1uF capacitor to GND, a resistor of 2kOhm should be applied between VOUT and VBUS

6. IP Series Products List

Power Bank IC

IC	Cha /Discł	-		Features						Package	
Part No.	Charge	Dis- charge	LED Num	Lighting	Keys	12C	DCP	Type-C	QC Certificate	Package	Compa tibility
IP5303	1.0A	1.2A	1,2	٧	V	-	-	-	-	eSOP8	Z
IP5305	1.0A	1.2A	1,2,3,4	٧	V	-	-	-	-	eSOP8	PIN2PIN
IP5306	2.4A	2.1A	1,2,3,4	٧	٧	-	-	-	-	eSOP8	Ы
IP5206	2A (Max)	1.5A	3,4,5	٧	v	-	-	-	-	eSOP16	PIN2PIN
IP5108E	2.0A	1.0A	3,4,5	٧	٧	-	-	-	-	eSOP16	PINZ
IP5108	2.0A	2.0A	3,4,5	٧	٧	V	-	-	-	eSOP16	_
IP5207	1.2A	1.2A	3,4,5	٧	٧	-	-	-	-	QFN24	
IP5207T	1.2A	1.2A	1,2,3,4	٧	V	V	V	-	-	QFN24	NIU
IP5109	2.1A	2.1A	3,4,5	٧	٧	٧	-	-	-	QFN24	PIN2PIN
IP5209	2.4A	2.1A	3,4,5	٧	V	v	V	-	-	QFN24	-
IP5219	2.4A	2.1A	1,2,3,4	٧	٧	٧	v	v	-	QFN24	
IP5310	3.1A	3.0A	1,2,3,4	٧	V	V	٧	v	-	QFN32	



IP2707

IP5312	15W	3.6A	2,3,4,5	٧	V	v	٧	-	-	QFN32	
IP5318Q	18W	4.0A	2,3,4,5	V	٧	٧	۷	-	V	QFN40	PIN2 PIN
IP5318	18W	4.0A	2,3,4,5	٧	V	v	٧	v	V	QFN40	II II
IP5322	18W	4.0A	1,2,3,4	٧	V	v	٧	-	V	QFN32	
IP5328	18W	4.0A	1,2,3,4	٧	V	v	٧	v	V	QFN40	

USB Charging Port Control IC

						Star	ndards S	Supported					
IC Part No.	Channel Num	BC1.2 & APPLE	QC3.0 & QC2.0	FCP	SCP	AFC	SFCP	MTK PE+ 2.0&1.1	Туре-С	NTC	QC Certi- ficate	PD3.0	Package
IP2110	1	v	-	-	-	-	-	-	-	-	-		SOT23-5
IP2111	1	v	-	-	-	-	-	-	-	1			SOT23-6
IP2112	2	v	-	-	-	-	-	- /	- (-	-	-	SOT23-6
IP2161	1	v	٧	v	-	v	V	-	-		٧	-	SOT23-6
IP2163	1	v	٧	v	-	v	V	٧	-)	٧	٧	-	SOP8
IP2701	1	v	٧	v	-	v	V	-	V	-	-	-	SOP8
IP2703	1	v	٧	v	-	v	V	٧	v	٧	-	-	DFN10
IP2705	1	v	٧	v	-	٧	V	٧	v	٧	-	-	DFN12
IP2707	2	v	٧	٧	-	V	V	v	v	٧	-	-	QFN16
IP2716	1	٧	٧	v	V	V	-	1.1	٧	-	٧	٧	QFN32

7. Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
VBUS Input Voltage Range	VBUS	-0.3 ~ 7	v
DP, DM Input Voltage Range	V _{DP} , V _{DM}	-0.3 ~ 11	v
CC1,CC2 input Voltage Range	V_{CC1}, V_{CC2}	-0.3 ~ 12	v
Other pins Voltage		-0.3~6.5	v
Junction Temperature Range	TJ	-40 ~ 150	°C
Storage Temperature Range	Tstg	-60 ~ 150	Ĉ
Lead Temperature (Soldering, 10sec.)	Ts	260	ĉ
Ambient Temperature Range	T _A	-40 ~ 150	Ĉ
Package Thermal Resistance	θ _{JA}	44.6	°C /w
Package Thermal Resistance	θ _{JC}	54.3	°C /w
Human Body Model (HBM)	ESD	4	KV

*Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to Absolute Maximum Rated conditions for extended periods may affect device reliability.

*Voltages are referenced to GND unless otherwise noted.



8. Recommended Operating Conditions

Parameter	Symbol	Min.	Тур.	Max.	Unit
Input Voltage	VBUS	3		5.5	V
Ambient Temperature	T _A	-40		85	°C

*Devices' performance cannot be guaranteed when working beyond those Recommended Operating Conditions.

9. Electrical Characteristics

Unless otherwise specified, $T_{A}\text{=}25\,^{\circ}\text{C}$, 4.5V \leq VBUS \leq 5.5V

Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Input Voltage	VBUS,VCC		3		5.5	V
Input UVLO Threshold	UVLO	VBUS,VCC Falling	2.5		2.9	V
Quiescent Current	Ι _Q	No load, VBUS=5V	50	66	100	uA
Startup Time	Ts		8	10	12	ms
SEL1, SEL2 Input High Voltage Threshold	V _{SELH}		2.5			v
SEL1, SEL2 Input Low Voltage Threshold	V _{SELL}				0.3	V
SEL1, SEL2 Default Output Voltage	V _{SELO}		1.35	1.5	1.65	V
HVDCP (QC2.0&QC3.0) Mode						
Data Detect Voltage Threshold	V _{DATA_REF}		0.25	0.325	0.4	V
Output Voltage Selection Reference	V _{SEL_REF}		1.8	2	2.2	V
DP High Glitch Filter Time	T _{GLITCH(BC)_DP_H}		1000	1250	1500	ms
DM Low Glitch Filter Time	T _{GLITCH(BC)_DM_L}			2		ms
Output Voltage Glitch Filter Time	T _{GLITCH(V)_CHANGE}		20	40	60	ms
Continuous Mode Glitch Filter Time	T _{GLITCH_CONT_CHANGE}		100		200	us
DM Pull-down Resistance	R _{DM_DOWN}	VDP=0.6V		20		kOhm
DP Pull-down Resistance	R _{DAT_LKG}	VDP=0.6V		400		kOhm
FB Current Step	I _{up} , I _{down}	40uA(9V); 70uA(12V); 150uA(20V)		2		uA
DCP Mode				1	1	1
Samsung DP/DM Output Voltage			1.08	1.2	1.32	V

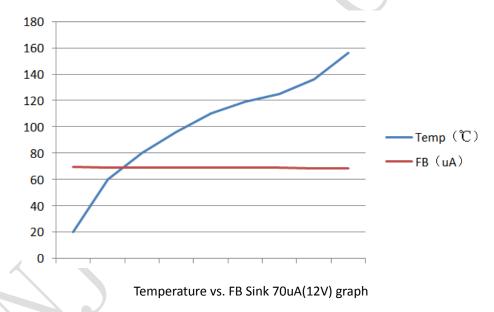




Samsung DP/DM Output Impedance			100		kOhm
Apple 2.4A DP/DM Output Voltage		2.64	2.7	2.76	V
Apple 2.4A DP/DM Output Impedance			30		kOhm
FCP/AFC Mode					
DM FCP/AFC Valid Tx High Voltage	V _{DM_TXH}	1.64		2.0	V
DM FCP/AFC Valid Tx Low Voltage	$V_{DM_{TXL}}$			0.3	V
DM FCP/AFC Valid Rx High Voltage	V _{DM_RXH}	0.9		3.6	V
DM FCP/AFC Valid Rx Low Voltage	V_{DM_RXL}			0.5	V

10.FB Temperature Character

TA=25 $^\circ\!\!\mathbb{C}$, 4.5V $\leq\!\!$ VBUS \leq 5.5V, Temp below represents the IC's temperature



11.Function Description

Charging Standards

IP2707 is a high-voltage, fast charging Physical Layer IC dedicated for charging applications where charging standards required to be negotiated between USB ports. IP2707 is needed at the host-side, when the attached portable client-side device negotiate the power allotment from the power source host-side, IP2707 can auto-detect and respond to the those charging standards and may grant or deny the request based on the available voltage/current. IP2707 will inform the power source host-side to adjust the output voltage by FB line once charging request granted.

IP2707 support dual channel USB ports charging control, and DP1,DM1 support analysis several charging



standards, including HVDCP QC3.0/QC2.0 (Quick Charge) Class A, FCP (Hisilicon[®] Fast Charge Protocol), AFC (Samsung[®] Adaptive Fast Charge), SFCP (Spreadtrum[®] Fast Charge Protocol), MTK PE+ 2.0/1.1 (MediaTek Pump Express Plus 2.0/1.1), Apple[®] 2.4A, BC1.2 and Samsung[®] 2.0A. DP2, DM2 only support Apple 2.4A, Samsung 2.0A and BC1.2.

IP2707 monitors the real-time voltage on DP line and DM line, when the attached device is not the fast charging type, IP2707 will change the voltage on the DP, DM line to fulfill the negotiation process. When fast charging client-side device connected, IP2707 auto-detect the type of charging standard and analysis the power requirements, source/sink current on FB line to grant the request voltage. When the output voltage is default 5V, FB line neither source nor sink current. IP2707 is not in control of the charging power loop, the actual charging loop and charging current is determined by the host-side power source and the client-side USB port device.

IP2707 integrated USB Type-C DRP port controller, SEL2 can configure the Type-C device as DFP, UFP or DRP mode. When worked as DFP mode, Type-C port support discharge to devices, at this moment CC1, CC2 will output 330uA current, for 3A maximum current capability broadcasting, IP2707 can work with Type-C UFP and DRP devices. When worked as UFP, Type-C port only support charging from devices, at this moment, CC1, CC2 are pulled down by 5.1kOhm resistor respectively, IP2707 can work with Type-C DFP, DRP devices. When worked as DRP mode, Type-C port recognize the inserted device's role and switch the pull-up or pull-down state on CC1 and CC2, thus IP2707 can work with DFP, UFP and DRP devices. And as DRP mode, Try.SRC function will be enabled, that is IP2707 work in DFP mode when connected with another DRP device.

SEL1

SEL1 line is used to configure the maximum voltage allotment that can be request, when SEL1 line is pull up to high-voltage of V_{SELH} , the IP2707 will not respond to any fast charging requirements and output default 5V; When SEL1 line is floating, the maximum voltage allotment is 12V; When SEL1 line is pull down to GND, the maximum voltage allotment is 20V.

Voltage

5V

12V

SEL1

Float

High (V_{SELH})

SEL2	

\rightarrow	GND	20V		
s used to configure IP2	707 as different	Type-C role, whe	n SEL2 pulled	to high

SEL2 pin is used to configure IP2707 as different Type-C role, when SEL2 pulled to high V_{SELH} , IP2707 is configured as DRP device; when SEL2 floating, IP2707 is configured as DFP devices; when SEL2 pulled to GND, IP2707 is configured as UFP device.

SEL2	Voltage
High (V _{SELH})	DRP
Float	DFP



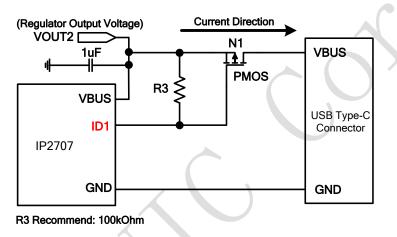
GND UFP

ID1 and ID2

ID1 and ID2 pin used to control Type-C power rail, ID1 used for Type-C DFP mode power rail control and ID2 is for Type-C UFP mode power rail control.

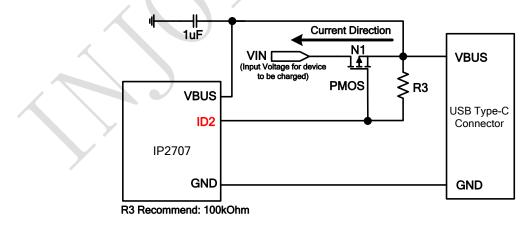
In 5V Application

In 5V application, after made successful handshake as Type-C DFP device, ID1 will output low level to open the PMOS on the Type-C power rail. The VOUT2 from regulator go through PMOS (N1) to VBUS and charge for the connected Type-C device, circuit for ID1 pin are recommended below:



Type-C DFP 5V application ID1 circuit

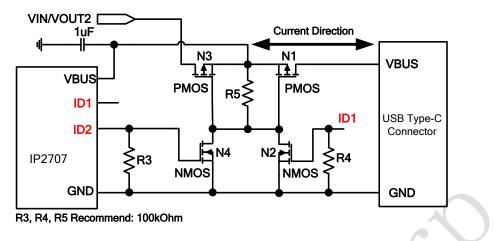
In 5V application, when Type-C work as UFP, after VBUS is detected power ok, ID2 will output low level voltage to turn on the PMOS on the Type-C power rail, VBUS output from Type-C connector go through the PMOS (N1) to VIN for the device to be charged, circuit for ID2 recommended below.

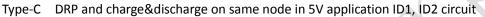


Type-C UFP 5V application ID2 circuit

In 5V application, when Type-C configured as DRP mode, and the VIN and VOUT2 are the same power node, the circuit for ID1 and ID2 are recommended below.

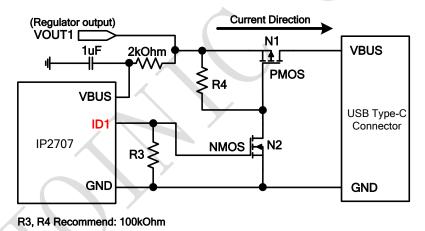






In Fast Charge Application

In fast charge application, after successful handshake as Type-C DFP role, ID1 will output high level voltage turn on the PMOS and NMOS on the Type-C power rail. VOUT1 from regulator output through PMOS (N1) to VBUS for Type-C device to be charged, circuit of ID1 in fast charge application recommended below:

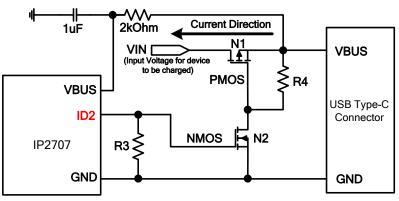


Type-C DFP in fast charge application ID1 circuit

In fast charge application, when worked as Type-C UFP, after VBUS is power ok, ID2 will output high level voltage to turn on the PMOS and NMOS on the Type-C power rail, VBUS output from Type-C device go through PMOS to VIN for the device to be charged, circuit for ID2 in fast charge application are recommended below:



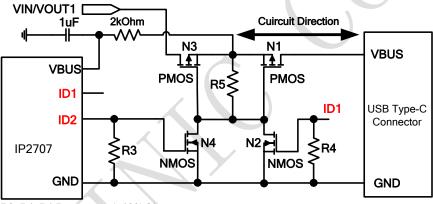




R3, R4 Recommend: 100kOhm

Type-C UFP in fast charge application ID2 circuit

In fast charge, when worked as Type-C DRP device, and VIN and VOUT1 are the same power node, the circuit for ID1 and ID2 are recommended below:



R3, R4, R4 Recommend: 100kOhm



VCC and VBUS

Both VCC and VBUS can power up IP2707, only when both VCC and VBUS are power ok, IP2707 work in normal function. Only VCC power ok, IP2707 will go into low power mode, at this moment, DP1, DM1, DP2, DM2 function disabled and these pins are in high-z state, CC1 and CC2 still in work.

When worked as DRP device applied in power bank devices, to reduce the power consumption, IP2707 enters low power mode when supplied by VCC only. Once VUBS power on or Type-C DFP mode is detected, IP2707 will be wake up automatically and work in normal function.

When worked as DFP device applied in adaptors, there's no low power mode, VCC can be floating, IP2707 can work normally by ensuring VBUS power ok.

CC1 and CC2

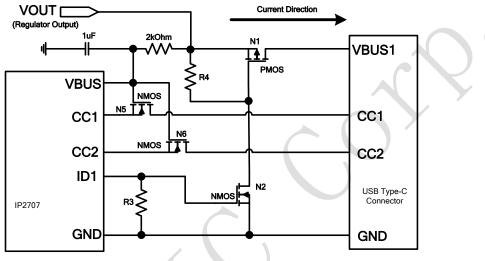
When neither VBUS or VCC is power ok, CC1 and CC2 pin pulled down by 5.1kOhm resistor respectively.

If IP2707 worked as DRP mode applied in DRP devices (such as power bank, cell phone and tablets, etc), or



worked as UFP mode only, when neither VBUS or VCC are power ok, once Type-C port accessed device, IP2707 worked as UFP mode by default.

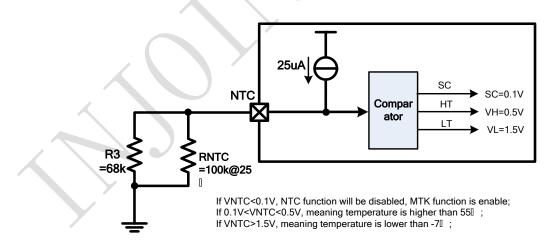
If IP2707 worked as DFP mode applied in DFP devices (such as adaptors, etc.), when neither VBUS or VCC are power ok, to avoid the current back flow from Type-C DRP device into adaptors, switch devices are needed on the CC1 and CC2 path, for isolating the pull down resistors on CC1 and CC2 of Type-C. Two NMOS switches (N5, N6) should be added, circuit recommended below:



R3, R4 Recommend: 100kOhm

Type-C DFP only application ID1 and CC1, CC2 circuit

NTC and FA



IP2707 integrated NTC temperature sensitive resistor detect function, and support abnormal temperature indication on FA pin. NTC and FA are multiplexed with CSN and CSP function on pin 3 and pin 14, only one function is enabled at the same time.

When pin 3 is connected to ground, internal comparator will detect that VNTC<0.1V, in this condition, pin 3 and pin 14 are CSN and CSP (MTK PE+ 2.0/1.1) function, a resistor of 10mOhm (1% accuracy) should be applied between the IC's GND and USB port's GND. Herein the NTC and FA function are disabled automatically.



When pin 3 is connected to the paralleled R3 and RNTC resistors to ground, in this condition, pin 3 and pin 14 are NTC and FA function, MTK PE+ 2.0/1.1 is disabled automatically. NTC pin will detect the temperature, when the temperature is abnormal, FA will output high level (equals VBUS), otherwise the FA output low level (GND).

When detected VNTC > VL (1.5V), meaning that the temperature is lower than -7° C, FA will output high level; when detected SC (0.1V) <VNTC< VH (0.5V), meaning that the temperature is higher than 55 $^{\circ}$ C, FA will output high level; when detected VH (0.5V) <VNTC< VL (1.5V), meaning that the temperature is in normal range of -7° C~55 $^{\circ}$ C, FA will output low level.

FB

IP2707 integrated FB control line used for accurate voltage regulation by source/sink current with precise 2uA/step in minimum. FB sink 40uA current for 9V output voltage; FB sink 70uA current for 12V output voltage; FB sink 150uA current for 20V output voltage; when the output voltage is default 5V, FB neither source nor sink current.

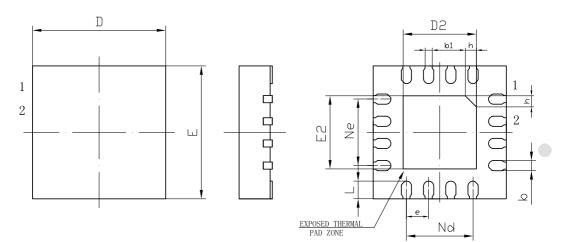
In typical applications, IP2707 FB connects to the regulator's FB line, resistor (R1) between VOUT and FB should apply 100kOhm with high precision (1%), resistor (R2) value between FB and GND should refer to the regulator adopted, resistance of R2 can be calculated by equation:

 $VFB = \frac{VOUT}{R1 + R2} * R2$



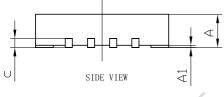


12.Package



TOP VIEW

BOTTOM VIEW



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
А	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.18	0.25	0.30
b1	0.16REF		
с	0.18	0.20	0.25
D	2.90	3.00	3.10
D 2	1.55	1.65	1.75
e	0. 50 BSC		
Ne	1.50 BSC		
Nd	1.50 BSC		
Е	2.90	3.00	3.10
E2	1.55	1.65	1.75
L	0.35	0.40	0.45
h	0.20	0.25	0.30
L/F载体尺寸 (mil)	75x75		



13.IMPORTANT NOTICE

INJOINIC TECHNOLOGY and its subsidiaries reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to INJOINIC TECHNOLOGY's terms and conditions of sale supplied at the time of order acknowledgment.

INJOINIC TECHNOLOGY assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using INJOINIC TECHNOLOGY's components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of INJOINIC TECHNOLOGY's components in its applications, notwithstanding any applications-related information or support that may be provided by INJOINIC TECHNOLOGY. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify INJOINIC TECHNOLOGY and its representatives against any damages arising out of the use of any INJOINIC TECHNOLOGY's components in safety-critical applications.

Reproduction of significant portions of INJOINIC TECHNOLOGY's information in INJOINIC TECHNOLOGY's data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. INJOINIC TECHNOLOGY is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

INJOINIC TECHNOLOGY will update this document from time to time. The actual parameters of the product may vary due to different models or other items. This document voids all express and any implied warranties.

Resale of INJOINIC TECHNOLOGY's components or services with statements different from or beyond the parameters stated by INJOINIC TECHNOLOGY for that component or service voids all express and any implied warranties for the associated INJOINIC TECHNOLOGY's component or service and is an unfair and deceptive business practice. INJOINIC TECHNOLOGY is not responsible or liable for any such statements.