



### DMT40M9LPS

# 40V N-CHANNEL ENHANCEMENT MODE MOSFET PowerDI5060-8 (Type K)

### **Product Summary**

BV <sub>DSS</sub>	R <sub>DS(ON)</sub> Max	I <sub>D</sub> T <sub>C</sub> = +25°C (Note 9)
40V	$0.9m\Omega$ @ $V_{GS} = 10V$	304A
	$1.5 \text{m}\Omega$ @ $V_{GS} = 4.5 \text{V}$	235A

# **Description and Applications**

This MOSFET has been designed to minimize the on-state resistance (R<sub>DS(ON)</sub>) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

- Engine Management Systems
- Body Control Electronics
- DC-DC Converters
- Synchronous Rectification

#### ectification

PowerDI5060-8 (Type K)







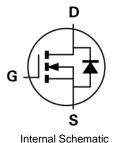
Bottom View

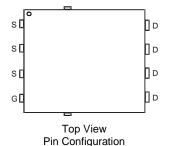
### **Features**

- 100% Unclamped Inductive Switching Ensures More Reliable and Robust End Application
- Thermally Efficient Package-Cooler Running Applications
- High Conversion Efficiency
- Low R<sub>DS(ON)</sub> Minimizes On State Losses
- <1.1mm Package Profile Ideal for Thin Applications (PowerDI<sup>®</sup>)
- Lead-Free Finish; RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free, "Green" Device (Note 3)
- Qualified to AEC-Q101 Standards for High Reliability

### **Mechanical Data**

- Case: PowerDI5060-8 (Type K)
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Finish Matte Tin Annealed over Copper Leadframe.
   Solderable per MIL-STD-202, Method 208 (3)
- Weight: 0.097 grams (Approximate)





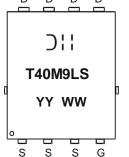
### Ordering Information (Note 4)

Part Number	Case	Packaging
DMT4001LPS-13	PowerDI5060-8 (Type K)	2,500 / Tape & Reel

Notes:

- 1. EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant. All applicable RoHS exemptions applied.
- See http://www.diodes.com/quality/lead\_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

## **Marking Information**



☐ H=Manufacturer's Marking
T40M9LS= Product Type Marking Code
YYWW = Date Code Marking
YY = Last Two Digits of Year (ex: 17 = 2017)
WW = Week Code (01 to 53)



T4001LS = Product Type Marking Code
YYWW = Date Code Marking
YY = Last Two Digits of Year (ex: 17 = 2017)
WW = Week Code (01 to 53)

PowerDI is a registered trademark of Diodes Incorporated.



# **Maximum Ratings** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit	
Drain-Source Voltage	$V_{DSS}$	40	V	
Gate-Source Voltage		$V_{GSS}$	±20	V
Continuous Drain Current, V <sub>GS</sub> = 10V (Note 6 & 9)	$T_C = +25$ °C $T_C = +70$ °C	I <sub>D</sub>	304 243	А
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)	I <sub>DM</sub>	400	Α	
Continuous Body Diode Forward Current (Note 6)	T <sub>C</sub> = +25°C	I <sub>S</sub>	100	Α
Pulsed Body Diode Forward Current (10µs Pulse, Duty Cycle = 1%)	I <sub>SM</sub>	400	Α	
Avalanche Current, L = 0.1mH	I <sub>AS</sub>	77.7	Α	
Avalanche Energy, L = 0.1mH		E <sub>AS</sub>	391	mJ

# **Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 5)	P <sub>D</sub>	2.4	W
Thermal Resistance, Junction to Ambient (Note 5)	$R_{\theta JA}$	52	°C/W
Total Power Dissipation (Note 6)	P <sub>D</sub>	125	W
Thermal Resistance, Junction to Case (Note 6)	$R_{\theta JC}$	1	°C/W
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C

# **Electrical Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition	
OFF CHARACTERISTICS (Note 7)							
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	40	_	_	V	$V_{GS} = 0V$ , $I_D = 1mA$	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>		_	1	μΑ	$V_{DS} = 32V, V_{GS} = 0V$	
Gate-Source Leakage	I <sub>GSS</sub>	-	_	±100	nA	$V_{GS} = +20V, V_{DS} = 0V$ $V_{GS} = -16V, V_{DS} = 0V$	
ON CHARACTERISTICS (Note 7)							
Gate Threshold Voltage	V <sub>GS(TH)</sub>	1	l	3	٧	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	
Static Drain-Source On-Resistance		1	0.6	0.9		$V_{GS} = 10V, I_D = 50A$	
Static Diam-Source On-Resistance	R <sub>DS(ON)</sub>		1	1.5	mΩ	$V_{GS} = 4.5V, I_D = 50A$	
Diode Forward Voltage	V <sub>SD</sub>	_	_	1.3	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = 20A	
DYNAMIC CHARACTERISTICS (Note 8)							
Input Capacitance	Ciss	1	9903	_		V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0V, f = 1MHz	
Output Capacitance	Coss	1	4518	_	pF		
Reverse Transfer Capacitance	C <sub>rss</sub>	_	410	_			
Gate Resistance	Rg	_	3.56	_	Ω	$V_{DS} = 0V$ , $V_{GS} = 0V$ , $f = 1MHz$	
Total Gate Charge (V <sub>GS</sub> = 10V)	$Q_g$	1	159	_		V <sub>DD</sub> = 20V, I <sub>D</sub> = 50A	
Total Gate Charge (V <sub>GS</sub> = 4.5V)	Qq	_	72.9	_			
Gate-Source Charge	Qgs	_	23.4	_	nC		
Gate-Drain Charge	Q <sub>qd</sub>	_	41.7	_			
Turn-On Delay Time	t <sub>D(ON)</sub>	_	7.53	_		$V_{DD} = 20V, V_{GS} = 10V,$ $I_{D} = 50A, R_{g} = 2.5\Omega$	
Turn-On Rise Time	t <sub>R</sub>	-	27.4	_			
Turn-Off Delay Time	t <sub>D(OFF)</sub>	-	135	_	ns		
Turn-Off Fall Time	t <sub>F</sub>	-	68.1	_			
Reverse Recovery Time	t <sub>RR</sub>	_	102	_	ns	L 50A di/dt 400A/v.c	
Reverse Recovery Charge	$Q_{RR}$		238	_	nC	I <sub>F</sub> = 50A, di/dt = 100A/μs	

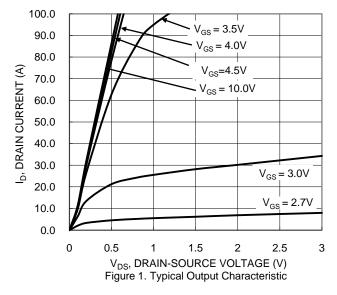
5. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate. Notes:

6. Thermal resistance from junction to soldering point (on the exposed drain pad).

<sup>7.</sup> Short duration pulse test used to minimize self-heating effect.

<sup>8.</sup> Guaranteed by design. Not subject to product testing.
9. Limited by package. Silicon chip capability is 304A at +25°C.





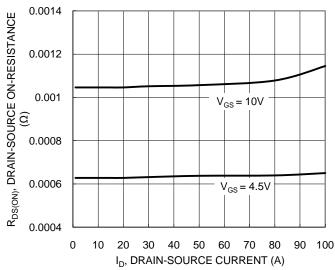
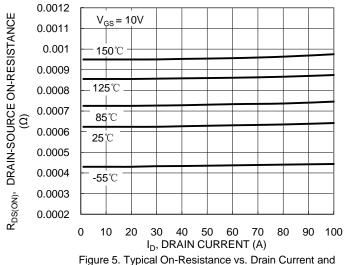
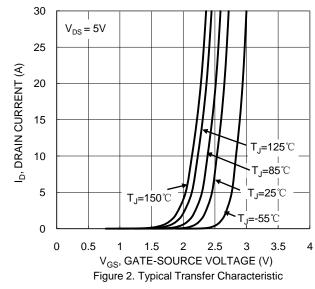
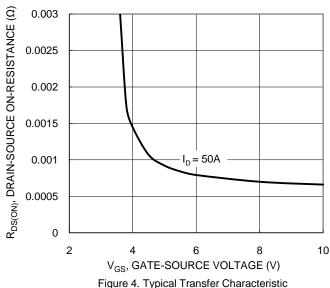


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage



Junction Temperature





1.8 R<sub>DS(ON)</sub>, DRAIN-SOURCE ON-RESISTANCE (NORMALIZED) 1.6 1.4  $V_{GS} = 10 \text{V}, I_D = 50 \text{A}$ 1.2 1  $V_{GS} = 4.5V, I_{D} = 50A$ 8.0 0.6 0.4 -50 -25 25 50 75 100 125 150 T<sub>.</sub>I, JUNCTION TEMPERATURE (°C)

Figure 6. On-Resistance Variation with Junction Temperature





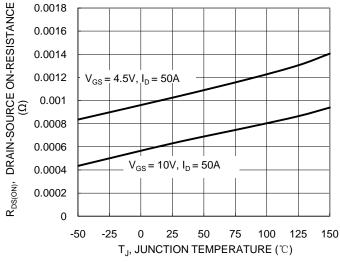


Figure 7. On-Resistance Variation with Junction Temperature

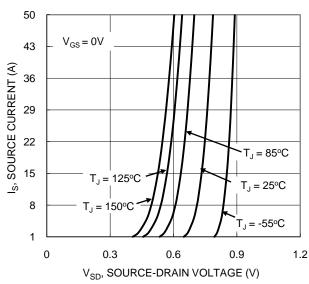


Figure 9. Diode Forward Voltage vs. Current

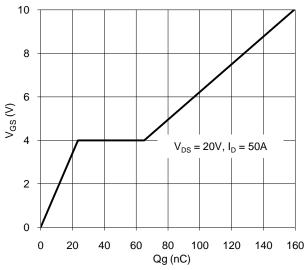


Figure 11. Gate Charge

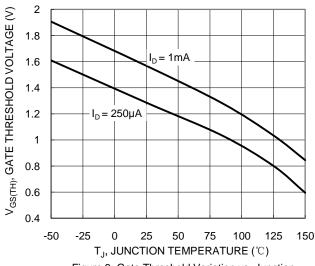


Figure 8. Gate Threshold Variation vs. Junction Temperature

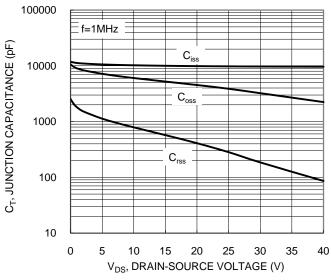
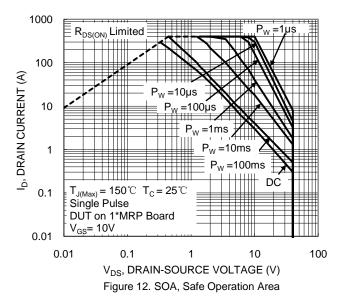


Figure 10. Typical Junction Capacitance





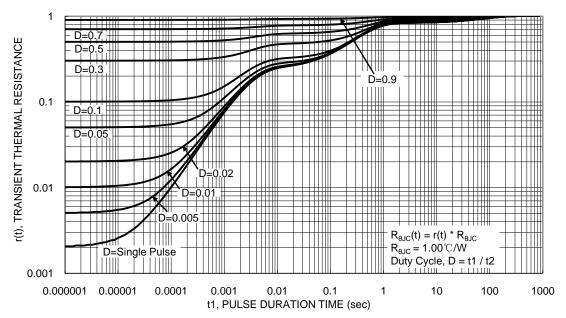


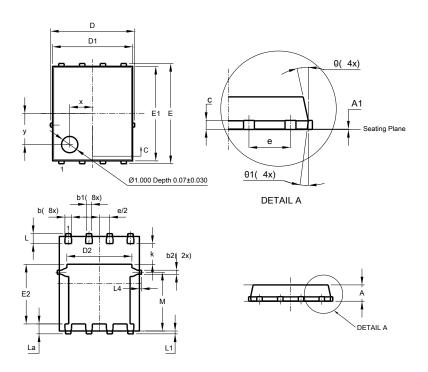
Figure 13. Transient Thermal Resistance



# **Package Outline Dimensions**

Please see http://www.diodes.com/package-outlines.html for the latest version.

### PowerDI5060-8 (Type K)

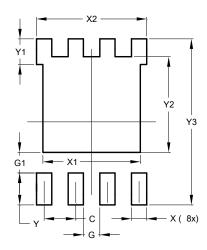


PowerDI5060-8					
(Type K)					
Dim	Min	Max	Тур		
Α	0.90	1.10	1.00		
<b>A</b> 1	0	0.05	0.02		
b	0.33	0.51	0.41		
b1	0.300	0.366	0.333		
b2	0.20	0.35	0.25		
C	0.23	0.33	0.277		
D	5	.15 BS0	3		
D1	4.85	4.95	4.90		
D2	-	-	3.98		
Е	6.15 BSC				
E1	5.75	5.85	5.80		
E2	3.56	3.76	3.66		
Е	1.27BSC				
k	-	-	1.27		
L	0.51	0.71	0.61		
La	0.51	0.71	0.61		
L1	0.05	0.20	0.175		
L4	-	-	0.125		
M	3.50	3.71	3.605		
X	-	-	1.400		
у	-	-	1.900		
θ	10°	12°	11°		
θ1	6°	8°	7°		
All Dimensions in mm					

# **Suggested Pad Layout**

Please see http://www.diodes.com/package-outlines.html for the latest version.

## PowerDI5060-8 (Type K)



Dimensions	Value			
Dillielisions	(in mm)			
С	1.270			
G	0.660			
G1	0.820			
Х	0.610			
X1	3.910			
X2	4.420			
Υ	1.270			
Y1	1.020			
Y2	3.810			
Y3	6.610			



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