

Data sheet acquired from Harris Semiconductor SCHS082C - Revised October 2003

# **CMOS 8-Bit Priority Encoder**

High-Voltage Types (20-Volt Rating)

■ CD4532B consists of combinational logic that encodes the highest priority input (D7-D0) to a 3-bit binary code. The eight inputs, D7 through D0, each have an assigned priority; D7 is the highest priority and D0 is the lowest. The priority encoder is inhibited when the chip-enable input Ei is low. When E<sub>1</sub> is high, the binary representation of the highest-priority input appears on output lines Q2-Q0, and the group select line GS is high to indicate that priority inputs are present. The enable-out (E<sub>O</sub>) is high when no priority inputs are present. If any one input is high, EO is low and all cascaded lower-order stages are disabled.

The CD4532B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

#### Features:

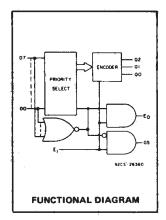
- Converts from 1 of 8 to binary
- Provides cascading feature to handle any number of inputs
- Group select indicates one or more priority inputs
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 µA at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- Noise margin (full-package-temperature range):

0.5 V at V<sub>DD</sub> = 5 V 1.5 V at V<sub>DD</sub> = 10 V 1.5 V at V<sub>DD</sub> = 15 V

- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

### Applications:

- Priority encoder
- Binary or BCD encoder (keyboard encoding)
- Floating point arithmetic



CD4532B Types

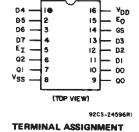
### **RECOMMENDED OPERATING CONDITIONS**

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	Min.	Max	Units
Supply Voltage Range (for T <sub>A</sub> =	3	18	V
Full Package Temp. Range)			

### MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (VDD) INPUT VOLTAGE RANGE, ALL INPUTS .....-0.5V to VDD +0.5V POWER DISSIPATION PER PACKAGE (PD): For T<sub>A</sub> = +100°C to +125°C ...... Derate Linearity at 12mW/°C to 200mW DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR TA = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)........... 100mW OPERATING-TEMPERATURE RANGE (TA) .....-55°C to +125°C STORAGE TEMPERATURE RANGE (Tstg) .....-65°C to +150°C LEAD TEMPERATURE (DURING SOLDERING): 



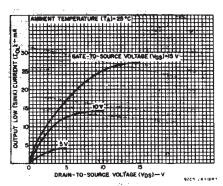


Fig. 1 — Typical output low (sink) current

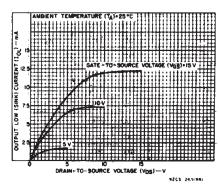


Fig. 2 — Minimum output low (sink) current characteristics.

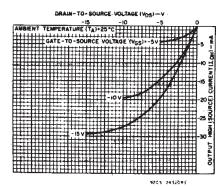


Fig. 3 — Typical output high (source) current characteristics.

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### STATIC ELECTRICAL CHARACTERISTICS

CHARACTER-	CONE	OITION	IS	LIMI	TS AT	INDICA	TED TE	MPER/	ATURES	(°C)	UNITS
ISTIC	vo	VIN	VDD						+25		0
	(V)	(V)	(V)	-55	<del>-4</del> 0	+85	+125	Min.	Тур.	Max.	
Quiescent Device		0,5	5	5	5	150	150	-	0.04	5	
Current, IDD Max.	_	0,10	10	10	10	300	300	-	0.04	10	μА
	_	0,15	15	20	20	600	600	-	0.04	20	<i>μ.</i> ,
		0,20	20	100	100	3000	3000	_	0.08	100	
Output Low	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	-	
(Sink) Current	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6		
IOL Min.	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	_	
Output High	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	_	mA
(Source) Current, IOH Min.	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2		
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	- <del>-</del>	
	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8		
Output Voltage:	_	0,5	5		0	.05		_	0	0.05	
Low-Level, VOL Max.	-	0,10	10		0	.05			0	0.05	
VUL Max.	-	0,15	15		0	.05		-	0	0.05	l v
Output Voltage:		0,5	5		4	.95		4.95	5	-	ľ
High-Level,	. –	0,10	10		9	95		9.95	10		
VOH Min.	_	0,15	15		14	1.95		14.95	15		
Input Low	0.5, 4.5	1	5			1		-		1.5	
Voltage, V <sub>IL</sub> Max.*	1, 9	-	10		2	.5		-	_	3	
VIL Max.	1.5,13.5	_	15			3		_		4	v
Input High	0.5, 4.5	_	5			4		3.5			ľ
Voltage,	1, 9		10		7	.5		7			
VIH Min.	1.5,13.5	_	15		1	2		11	_	_	
Input Current IIN Max.		0,18	18	±0.1	±0.1	±1	±1	_	±10 <sup>-5</sup>	±0.1	μА

<sup>\*</sup>One input is tested at a time; other inputs should be at  $V_{DD}$  or  $V_{SS}$ . For testing all inputs at  $V_{IL}$  and  $V_{IH}$  levels, use 20%/80%  $V_{DD}$ .

# DYNAMIC ELECTRICAL CHARACTERISTICS at T\_A=25°C; C\_L=50 pF, Input t\_r,t\_f= 20 ns, R\_L=200 K $\Omega$

CHARACTERISTIC	TEST CONDITIONS VDD	LIF	UNITS		
	VOLTS	TYP.	MAX.		
Propagation Delay Time tpHL, tpLH	5	110	220		
E <sub>I</sub> to E <sub>O</sub> , E <sub>I</sub> to GS	10	55	110	1	
	15	45	85	1	
	5	170	340	1	
Et to Qm, Dn to GS	10	85	170	ns	
	15	65	125	1	
	5	220	440		
Dn to Q <sub>M</sub>	10	110	220		
	15	85	160	[	
	5	100	200		
Transition Time tTHL, tTLH	10	50	100	ns	
	15	40	80		
Input Capacitance CIN	Any Input	5	7.5	pF	

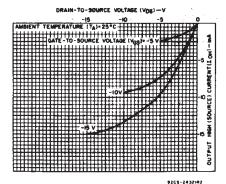


Fig. 4 — Minimum output high (source) current characteristics.

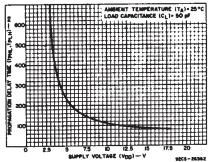


Fig. 5 — Typical propagation delay (Dn to Qm) vs. supply voltage.

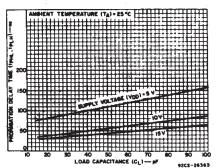


Fig. 6 — Typical propagation delay (E<sub>1</sub> to GS, E<sub>1</sub> to E<sub>O</sub>) vs. load capacitance.

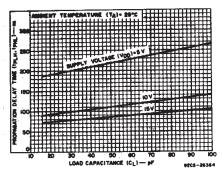


Fig. 7 — Typical propagation delay (Dn to Qm) vs. load capacitance.

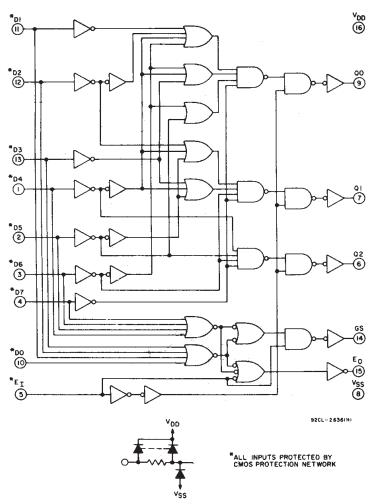


Fig. 8 — CD4532 logic diagram.

### TRUTH TABLE

			,			Dutput							
Εį	D7	D6	D5	D4	D3	D2	D1	D0	GS	Q2	Q1	Q0	Eo
0	Х	Х	Х	Х	Х	X.	Х	X	Ō	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	1
1	1	Χ.	х	Х	Х	Х	×	Х	1	1	1	1	0
1	0	1	Х	х	x	Х	×	х	1	1.	1	0	0
1	0	0	1	Х	×	Х	×	х	1	1	0	1	0
1	0	0	0	1	×	Х	x	Х	1	1	0	0	0
1	0	0	0	0	1	Х	Х	Х	1	0	1	1	0
1	0	0	0	0	0	1	×	х	1	0	1	0	0
1	0	0	0	0	0	0	1	х	1	0	0	1	0
1	0	0	0	0	0	0	0	1	1	0	0	0	0

X = Don't Care Logic 1  $\equiv$  High Logic 0  $\equiv$  Low

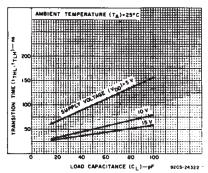


Fig.9 – Typical transition time vs. load capacitance.

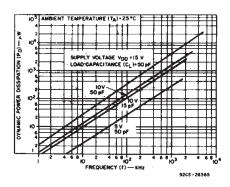


Fig. 10 — Typical dynamic power dissipation vs. fraquency.

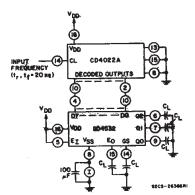


Fig.11 — Dynamic power dissipation test circuit.

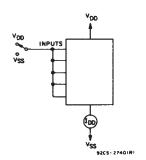


Fig. 12 - Quiescent device current test circuit.

### CD4532B Types

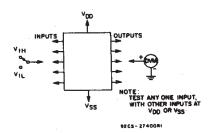


Fig. 13 - Input voltage test circuit.

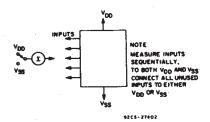
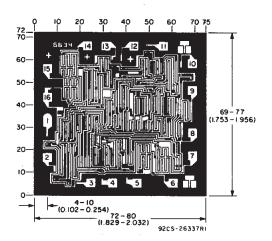


Fig. 14 - Input current test circuit.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils  $(10^{-3})$  inch).

Dimensions and pad layout for CD4532BH.

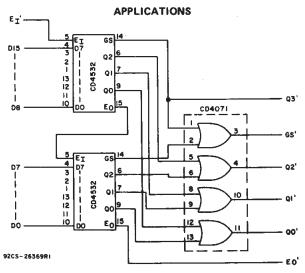
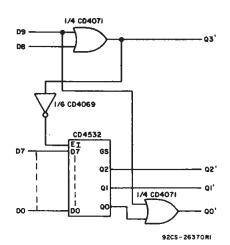


Fig. 15 - 16-level priority encoder.



TRUTH TABLE

ſ					In	out					Output					
ſ	D9	D8	D7	D6	<b>D</b> 5	D4	D3	D2	D1	DO	GS	σ3.	Q2'	01'	GO,	
ſ	1	х	х	х	х	Х	х	х	Х	х	0	1	0	0	1	
ı	0	1	x	X	Х	×	X	Х	Х	X	0	1	0	0	0	
ľ	0	0	1	х	Х	Х	Х	Х	X	X	1-	0	1	1	1	
1	0	0	0	1 -	x	х	X	X.	X	х	1	0	1	1	0	
1	0	0	0	0	1	X	X	X	Х	Х	1	0	1	0	1	
ı	0	0	0	0	0	_1_	X	X	Х	Х	1 1	0	1	0	0	
I	0	0	0	0	0	0	1	Х	Х	Х	1	0.	0	1	1	
ł	0	0	0	0	0	0	0	1	Х	х	1	- 0	0	1	0	
١	0	0	0	0	0	0	0	0	1	х	1	0	0	0	1	
ı	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	
	X =	Don	't Ca	re			Logic 1 ≡ High					Logic 0 ≅ Lov				

Fig.16 - 0-to-9 keyboard encoder.





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### **PACKAGING INFORMATION**

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Top-Side Markings	Samples
CD4532BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4532BE	Samples
CD4532BEE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4532BE	Samples
CD4532BF3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD4532BF3A	Samples
CD4532BM	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4532BM	Samples
CD4532BM96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4532BM	Samples
CD4532BM96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4532BM	Samples
CD4532BM96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4532BM	Samples
CD4532BME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4532BM	Samples
CD4532BMG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4532BM	Samples
CD4532BMT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4532BM	Samples
CD4532BMTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4532BM	Samples
CD4532BMTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4532BM	Samples
CD4532BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4532B	Samples
CD4532BNSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4532B	Samples
CD4532BNSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4532B	Samples
CD4532BPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM532B	Samples
CD4532BPWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM532B	Samples



# PACKAGE OPTION ADDENDUM

11-Apr-2013

Orderable Device	Status	Package Type	_	Pins	_	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Top-Side Markings	Samples
	(1)		Drawing		Qty	(2)		(3)		(4)	
CD4532BPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM532B	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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#### OTHER QUALIFIED VERSIONS OF CD4532B, CD4532B-MIL:

Catalog: CD4532B

Military: CD4532B-MIL





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### NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

# PACKAGE MATERIALS INFORMATION

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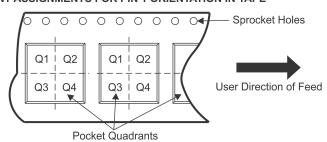
## TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



### \*All dimensions are nominal

All difficultions are florifinal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4532BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4532BNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4532BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

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### \*All dimensions are nominal

Device	Package Type Package Draw		Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4532BM96	SOIC	D	16	2500	333.2	345.9	28.6
CD4532BNSR	SO	NS	16	2000	367.0	367.0	38.0
CD4532BPWR	TSSOP	PW	16	2000	367.0	367.0	35.0

# 14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

# N (R-PDIP-T\*\*)

# PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



# D (R-PDS0-G16)

### PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



# D (R-PDSO-G16)

# PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G16)

# PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



# PW (R-PDSO-G16)

# PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



### **MECHANICAL DATA**

# NS (R-PDSO-G\*\*)

# 14-PINS SHOWN

### PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



#### IMPORTANT NOTICE

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