

# Three-wire Serial EEPROM

K93C56 / K93C66

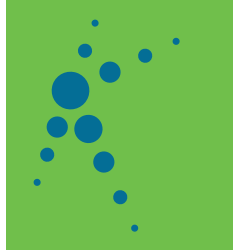


Spring 2012

# K93C56/K93C66

## Three-wire Serial EEPROM

2K bits (256 X 8 or 128 X 16) / 4K bits (512 X 8 or 256 X 16)



### Features

- ▶ Low-voltage Operation
  - 1.8V ( $V_{CC} = 1.8V$  to  $5.5V$ )
- ▶ Three-wire Serial Interface
- ▶ Sequential Read Operation
- ▶ 2 MHz Clock Rate (5V) Compatibility
- ▶ Self-timed Write Cycle (5 ms max)
- ▶ High-reliability
  - Endurance: 1 Million Write Cycles
  - Data Retention: 100 Years
- ▶ 8-lead PDIP/SOP/MSOP/TSSOP, 8-pad DFN, packages

### General Description

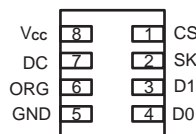
The K93C56/66 provides 2048/4096 bits of serial electrically erasable programmable read only memory (EEPROM) organized as 128/256 words of 16 bits each, when the ORG pin is connected to VCC and 256/512 words of 8 bits each when it is tied to ground. The K93C56/66 is available in space-saving 8-lead PDIP, 8-lead SOP, 8-lead TSSOP, 8-lead MSOP, and 8-pad DFN packages. The K93C56/66 is enabled through the Chip Select pin (CS), and accessed via a 3-wire serial interface consisting of Data Input (DI), Data Output (DO), and Shift Clock (SK). Upon receiving a Read instruction at DI, the address is decoded and the data is clocked out serially on the data output pin DO. The WRITE cycle is completely self-timed and no separate erase cycle is required before write. The Write cycle is only enabled when it is in the Erase/Write Enable state. When CS is brought "high" following the initiation of a write cycle, the DO pin outputs the Ready/Busy status.

### Pin Configuration

▶ Table 1: Pin Configuration

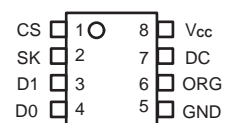
Pin Name	Functions
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V <sub>CC</sub>	Power Supply
ORG	Internal Organization
DC	Don't Connect

8-pad DFN

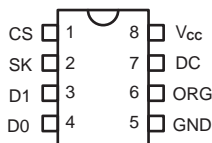


Bottom view

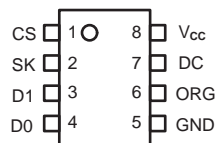
8-lead MSOP



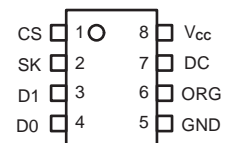
8-lead PDIP



8-lead SOP



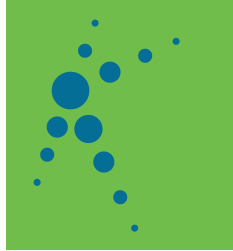
8-lead TSSOP



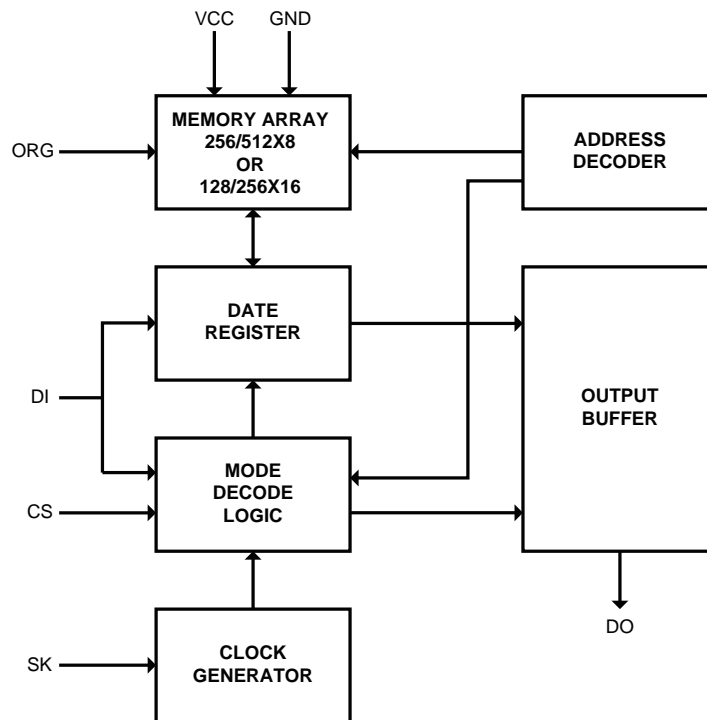
# K93C56/K93C66

## Three-wire Serial EEPROM

2K bits (256 X 8 or 128 X 16) / 4K bits (512 X 8 or 256 X 16)



### Block Diagram

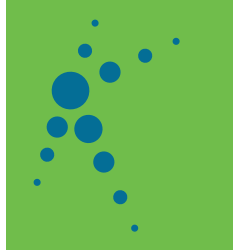


Notes: When the ORG pin is connected to VCC, the “x 16” organization is selected. When it is connected to ground, the “x 8” organization is selected. If the ORG pin is left unconnected and the application does not load the input beyond the capability of the internal 1 Meg ohm pullup, then the “x 16” organization is selected.

# K93C56/K93C66

## Three-wire Serial EEPROM

2K bits (256 X 8 or 128 X 16) / 4K bits (512 X 8 or 256 X 16)



### Function Descriptions

The K93C56/66 is accessed via a simple and versatile three-wire serial communication interface. Device operation is controlled by seven instructions issued by the host processor. A valid instruction starts with a rising edge of CS and consists of a start bit (logic "1") followed by the appropriate op code and the desired memory address location.

► Table 2: Instruction Set for the K93C56/66

Instruction	SB	OP Code	Address		Data		Comments
			x8	x16	x8	x16	
READ	1	10	A <sub>8</sub> - A <sub>0</sub>	A <sub>7</sub> - A <sub>0</sub>			Reads data stored in memory, at specified address
EWEN	1	00	11XXXXXXX	11XXXXXXX			Write enable must precede all programming modes
ERASE	1	11	A <sub>8</sub> - A <sub>0</sub>	A <sub>7</sub> - A <sub>0</sub>			Erase memory location A <sub>n</sub> - A <sub>0</sub>
WRITE	1	01	A <sub>8</sub> - A <sub>0</sub>	A <sub>7</sub> - A <sub>0</sub>	D <sub>7</sub> - D <sub>0</sub>	D <sub>15</sub> - D <sub>0</sub>	Writes memory location A <sub>n</sub> - A <sub>0</sub>
ERAL	1	00	10XXXXXXX	10XXXXXXX			Erases all memory locations. Valid only at V <sub>CC</sub> = 4.5V to 5.5V
WRAL	1	00	01XXXXXXX	01XXXXXXX	D <sub>7</sub> - D <sub>0</sub>	D <sub>15</sub> - D <sub>0</sub>	Writes all memory locations. Valid only at V <sub>CC</sub> = 4.5V to 5.5V
EWDS	1	00	00XXXXXXX	00XXXXXXX			Disables all programming instructions

Notes: The X's in the address field represent don't care values and must be clocked.

**READ (READ):** The Read (READ) instruction contains the address code for the memory location to be read. After the instruction and address are decoded, data from the selected memory location is available at the serial output pin DO. Output data changes are synchronized with the rising edges of serial clock SK. It should be noted that a dummy bit (logic "0") precedes the 8- or 16-bit data output string. The K93C56/66 supports sequential read operations. The device will automatically increment the internal address pointer and clock out the next memory location as long as Chip Select (CS) is held high. In this case, the dummy bit (logic "0") will not be clocked out between memory locations, thus allowing for a continuous stream of data to be read.

**ERASE/WRITE (EWEN):** To assure data integrity, the part automatically goes into the Erase/Write Disable (EWDS) state when power is first applied. An Erase/Write Enable (EWEN) instruction must be executed first before any programming instructions can be carried out. Please note that once in the EWEN state, programming remains enabled until an EWDS instruction is executed or V<sub>CC</sub> power is removed from the part.

**ERASE (ERASE):** The Erase (ERASE) instruction programs all bits in the specified memory location to the logical "1" state. The self-timed erase cycle starts once the ERASE instruction and address are decoded. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250 ns (TCS). A logic "1" at pin DO indicates that the selected memory location has been erased, and the part is ready for another instruction.

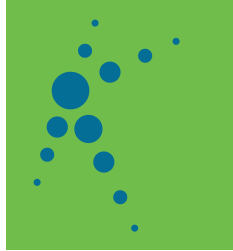
**WRITE (WRITE):** The Write (WRITE) instruction contains the 8 or 16 bits of data to be written into the specified memory location. The self-timed programming cycle, tWP, starts after the last bit of data is received at serial data input pin DI. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250 ns (TCS). A logic "0" at DO indicates that programming is still in progress. A logic "1" indicates that the memory location at the specified address has been written with the data pattern contained in the instruction and the part is ready for further instructions. A Ready/Busy status cannot be obtained if the CS is brought high after the end of the self-timed programming cycle, TWP.

**ERASE ALL (ERAL):** The Erase All (ERAL) instruction programs every bit in the memory array to the logic "1" state and is primarily used for testing purposes. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250 ns (TCS). The ERAL instruction is valid only at V<sub>CC</sub> = 5.0V ± 10%.

# K93C56/K93C66

## Three-wire Serial EEPROM

2K bits (256 X 8 or 128 X 16) / 4K bits (512 X 8 or 256 X 16)



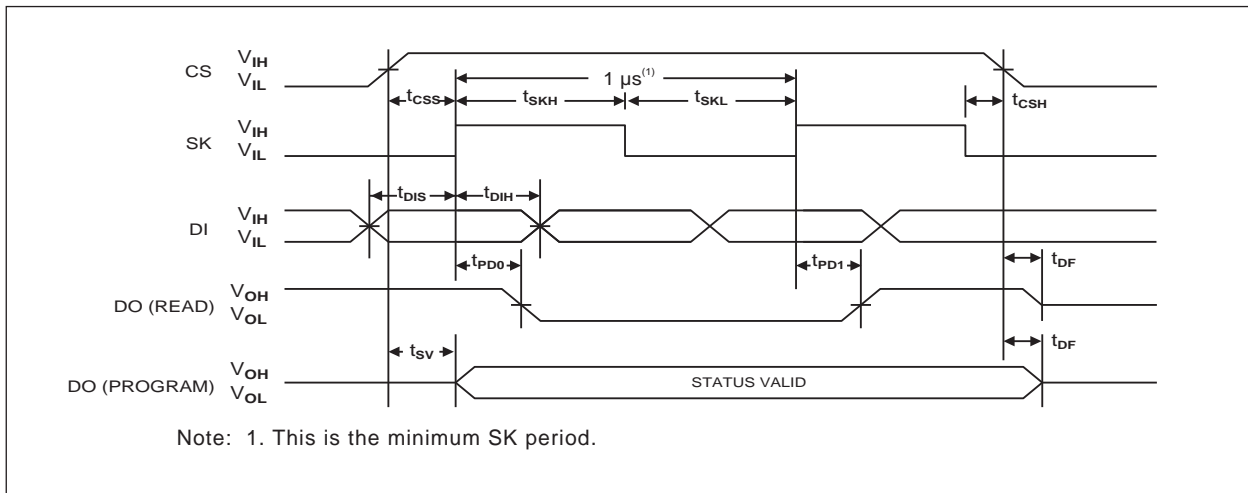
### Function Descriptions

**WRITE ALL (WRAL):** The Write All (WRAL) instruction programs all memory locations with the data patterns specified in the instruction. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250 ns (TCS). The WRAL instruction is valid only at  $V_{cc} = 5.0V \pm 10\%$ .

**ERASE/WRITE DISABLE (EWDS):** To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should be executed after all programming operations. The operation of the Read instruction is independent of both the EWEN and EWDS instructions and can be executed at any time.

### Timing Diagrams

► Figure 1: Synchronous Data Timing



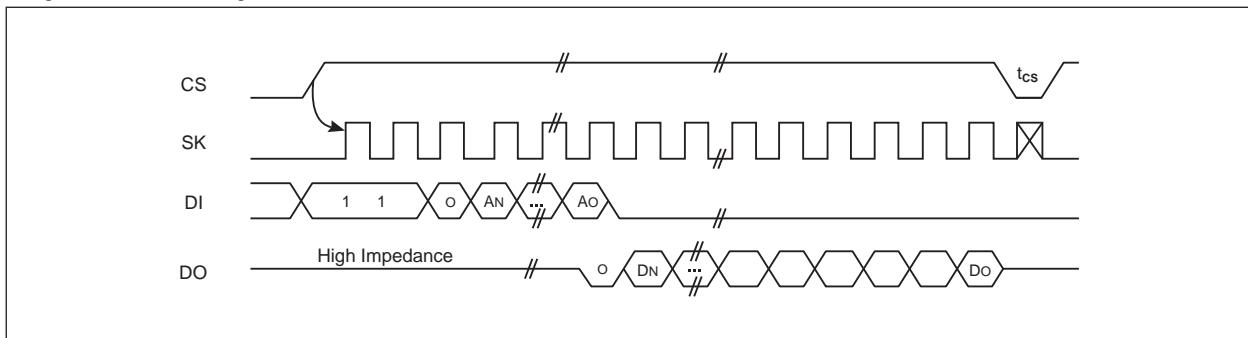
► Table 3: Organization Key for Timing Diagram

I/O	K93C56(2K)		K93C66(4K)	
	X 8	X 16	X 8	X 8
AN	A8(1)	A7(2)	A8	A7
DN	D7	D15	D7	D15

Note : 1. A8 is a DON'T CARE value, but the extra clock is required.

2. A7 is a DON'T CARE value, but the extra clock is required.

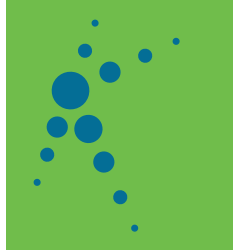
► Figure 2: READ Timing



# K93C56/K93C66

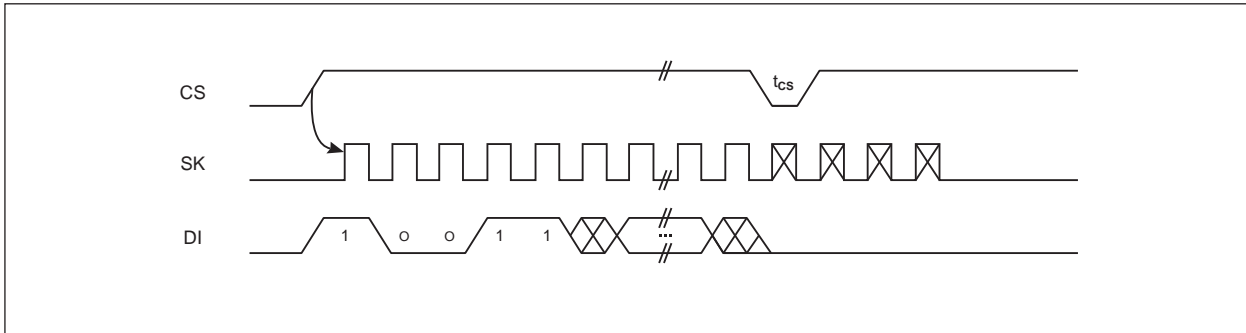
## Three-wire Serial EEPROM

2K bits (256 X 8 or 128 X 16) / 4K bits (512 X 8 or 256 X 16)

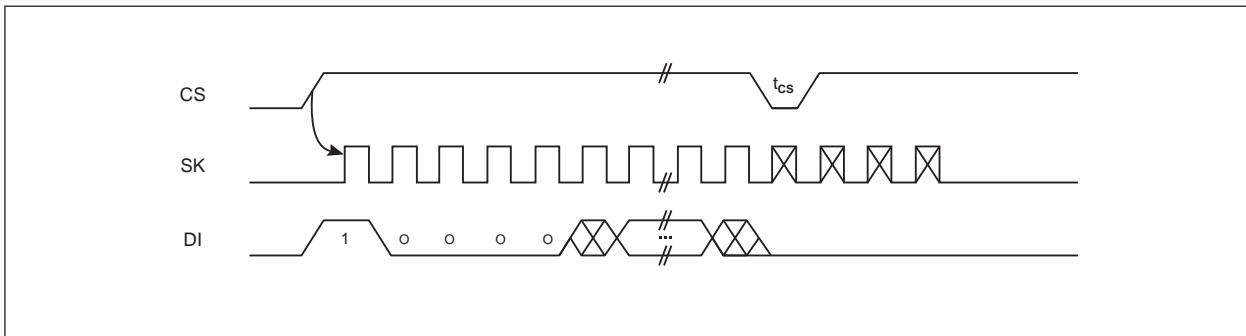


### Timing Diagrams

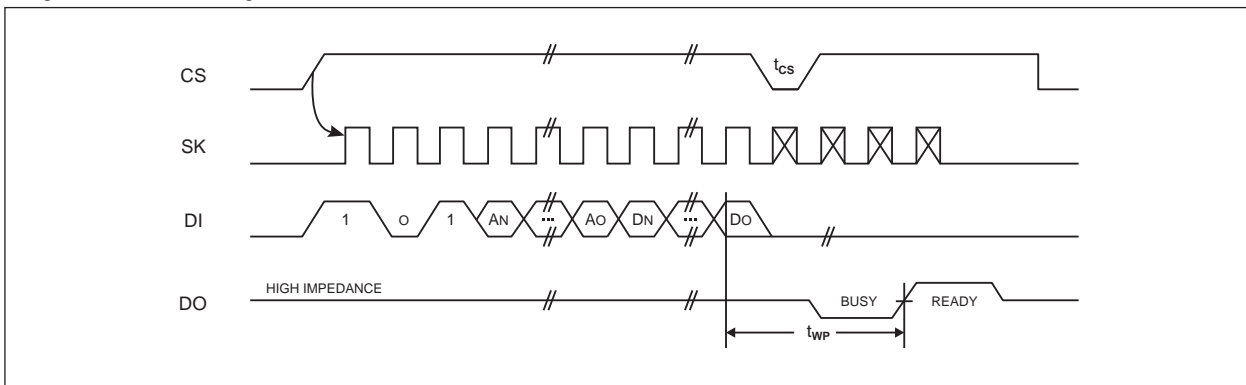
► Figure 3: EWEN Timing

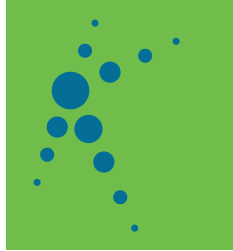


► Figure 4: EWDS Timing



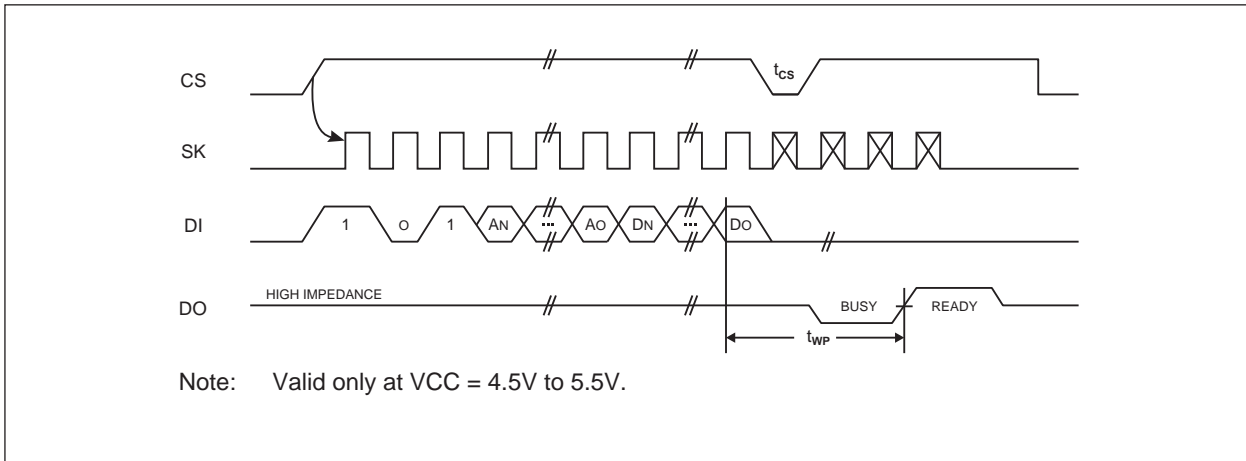
► Figure 5: WRITE Timing



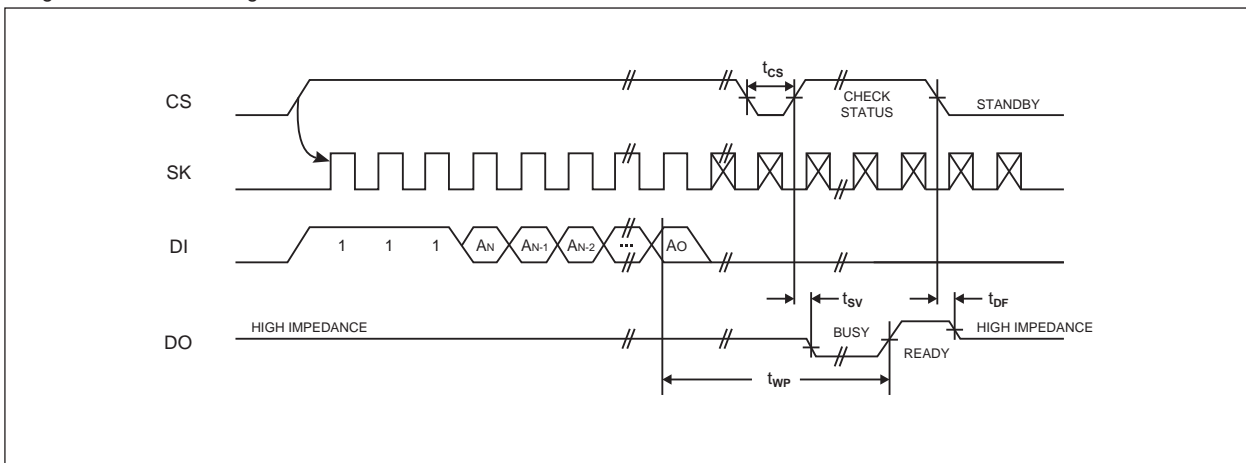


### Timing Diagrams

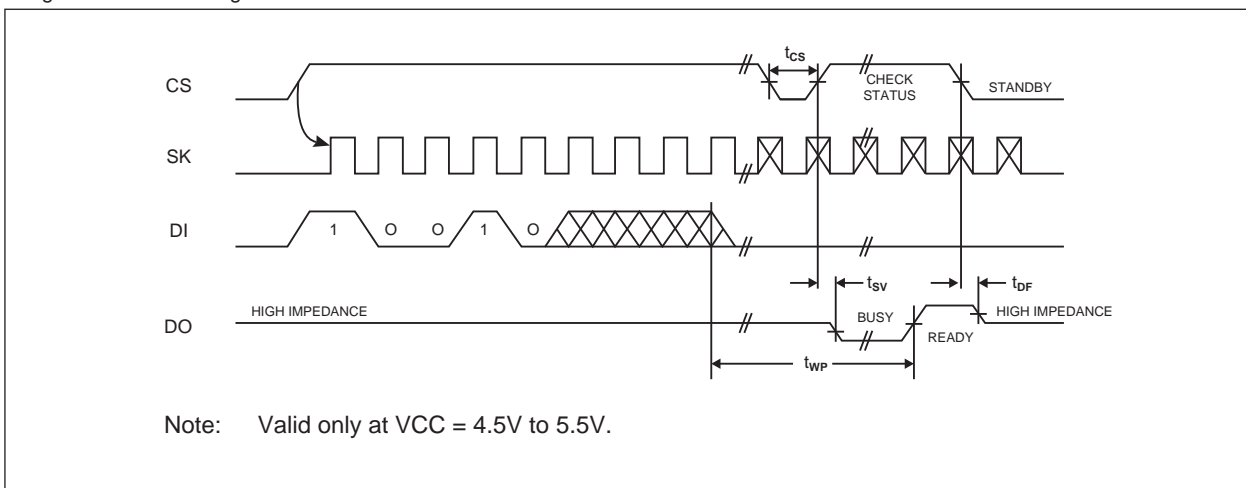
►Figure 6: WRAL Timing



►Figure 7: ERASE Timing



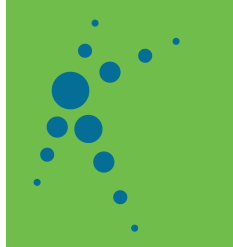
►Figure 8: ERAL Timing



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### Electrical Characteristics

#### Absolute Maximum Ratings

DC Supply Voltage . . . . . -0.3V to +6.5V

Input / Output Voltage . . . . . GND-0.3V to V<sub>CC</sub>+0.3V

Operating Ambient Temperature . . . . . -40°C to +85°C

Storage Temperature . . . . . -65°C to +150°C

#### Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

### DC Characteristics

► Applicable over recommended operating range from: T<sub>A</sub> = -40°C to +85°C, V<sub>CC</sub> = + 1.8V to + 5.5V, (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V <sub>CC1</sub>	Supply Voltage	-	1.8	-	5.5	V
V <sub>CC2</sub>	Supply Voltage	-	2.7	-	5.5	V
V <sub>CC3</sub>	Supply Voltage	-	4.5	-	5.5	V
I <sub>CC</sub>	Supply Current	V <sub>CC</sub> = 5.0V Read at 1.0 MHz Write at 1.0 MHz	-	0.5 2	2.0 3.0	mA
I <sub>SB1</sub>	Standby Current	V <sub>CC</sub> = 1.8V CS = 0V	-	-	1.0	µA
I <sub>SB2</sub>	Standby Current	V <sub>CC</sub> = 2.7V CS = 0V	-	-	1.0	µA
I <sub>SB3</sub>	Standby Current	V <sub>CC</sub> = 5.0V CS = 0V	-	-	1.0	µA
I <sub>IL(1)</sub>	Input Leakage	V <sub>IN</sub> = 0V to V <sub>CC</sub>	-	0.1	1.0	µA
I <sub>IL(2)</sub>	Input Leakage	V <sub>IN</sub> = 0V to V <sub>CC</sub>	-	2.0	3.0	µA
I <sub>OL</sub>	Output Leakage	V <sub>IN</sub> = 0V to V <sub>CC</sub>	-	0.1	1.0	µA
V <sub>IL(3)</sub>	Input Low Voltage	2.7V ≤ V <sub>CC</sub> ≤ 5.5V	-0.3	-	0.8	V
V <sub>IH(3)</sub>	Input High Voltage	2.7V ≤ V <sub>CC</sub> ≤ 5.5V	2.0	-	V <sub>CC</sub> + 0.3	V
V <sub>IL(2)</sub>	Input Low Voltage	1.8V ≤ V <sub>CC</sub> ≤ 2.7V	-0.5	-	V <sub>CC</sub> + 0.3	V
V <sub>IH(2)</sub>	Input High Voltage	1.8V ≤ V <sub>CC</sub> ≤ 2.7V	V <sub>CC</sub> x 0.7	-	V <sub>CC</sub> + 0.3	V
V <sub>OL1</sub>	Output Low Voltage	2.7V ≤ V <sub>CC</sub> ≤ 5.5V I <sub>OL</sub> = 2.1mA	-	-	0.4	V
V <sub>OH1</sub>	Output High Voltage	2.7V ≤ V <sub>CC</sub> ≤ 5.5V I <sub>OH</sub> = -0.4mA	2.4	-	V	V
V <sub>OL2</sub>	Output Low Voltage	1.8V ≤ V <sub>CC</sub> ≤ 2.7V I <sub>OL</sub> = 0.15mA	-	-	0.2	V
V <sub>OH2</sub>	Output High Voltage	1.8V ≤ V <sub>CC</sub> ≤ 2.7V I <sub>OH</sub> = -100µA	V <sub>CC</sub> -0.2	-	-	V

Note: V<sub>IL</sub> min and V<sub>IH</sub> max are reference only and are not tested.

### Pin Capacitance

► Applicable over recommended operating range from T<sub>A</sub> = 25°C, f = 1.0 MHz, V<sub>CC</sub> = +1.8V (unless otherwise noted)

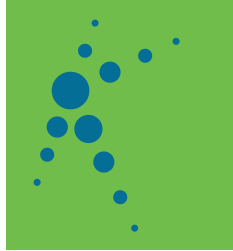
Symbol	Test Conditions	Max	Unit	Conditions
CO <sub>UT</sub>	Output Capacitance (DO)	5	pF	V <sub>OUT</sub> = 0V
C <sub>IN</sub>	Input Capacitance (CS, SK, DI, ORG)	5	pF	V <sub>IN</sub> = 0V



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### AC Characteristics

► Applicable over recommended operating range from TA = -40°C to +85°C, VCC = + 1.8V to + 5.5V

CL = 1 TTL Gate and 100pF (unless otherwise noted)

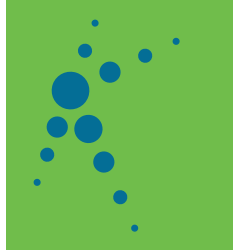
Symbol	Parameter	Test Condition		Min	Typ	Max	Units
f <sub>SK</sub>	SK Clock Frequency	4.5V ≤ V <sub>CC</sub> ≤ 5.5V		0	-	2	MHz
		2.7V ≤ V <sub>CC</sub> ≤ 5.5V		0		1	
		1.8V ≤ V <sub>CC</sub> ≤ 5.5V		0		0.25	
t <sub>SKH</sub>	SK High Time	4.5V ≤ V <sub>CC</sub> ≤ 5.5V		250	-	-	ns
		2.7V ≤ V <sub>CC</sub> ≤ 5.5V		250			
		1.8V ≤ V <sub>CC</sub> ≤ 5.5V		1000			
t <sub>SKL</sub>	SK Low Time	4.5V ≤ V <sub>CC</sub> ≤ 5.5V		250	-	-	ns
		2.7V ≤ V <sub>CC</sub> ≤ 5.5V		250			
		1.8V ≤ V <sub>CC</sub> ≤ 5.5V		1000			
t <sub>CS</sub>	Minimum CS Low Time	4.5V ≤ V <sub>CC</sub> ≤ 5.5V		250	-	-	ns
		2.7V ≤ V <sub>CC</sub> ≤ 5.5V		250			
		1.8V ≤ V <sub>CC</sub> ≤ 5.5V		1000			
t <sub>CSS</sub>	CS Setup Time	Relative to SK	4.5V ≤ V <sub>CC</sub> ≤ 5.5V	50	-	-	ns
			2.7V ≤ V <sub>CC</sub> ≤ 5.5V	50			
			1.8V ≤ V <sub>CC</sub> ≤ 5.5V	200			
t <sub>DIS</sub>	DI Setup Time	Relative to SK	4.5V ≤ V <sub>CC</sub> ≤ 5.5V	100	-	-	ns
			2.7V ≤ V <sub>CC</sub> ≤ 5.5V	100			
			1.8V ≤ V <sub>CC</sub> ≤ 5.5V	400			
t <sub>CSH</sub>	CS Hold Time	Relative to SK		0	-	-	ns
t <sub>DIH</sub>	DI Hold Time	Relative to SK	4.5V ≤ V <sub>CC</sub> ≤ 5.5V	100	-	-	ns
			2.7V ≤ V <sub>CC</sub> ≤ 5.5V	100			
			1.8V ≤ V <sub>CC</sub> ≤ 5.5V	400			
t <sub>PD1</sub>	Output Delay to "1"	AC Test	4.5V ≤ V <sub>CC</sub> ≤ 5.5V	-	-	250	ns
			2.7V ≤ V <sub>CC</sub> ≤ 5.5V			250	
			1.8V ≤ V <sub>CC</sub> ≤ 5.5V			1000	
t <sub>PD0</sub>	Output Delay to "0"	AC Test	4.5V ≤ V <sub>CC</sub> ≤ 5.5V	-	-	250	ns
			2.7V ≤ V <sub>CC</sub> ≤ 5.5V			250	
			1.8V ≤ V <sub>CC</sub> ≤ 5.5V			1000	
t <sub>SV</sub>	CS to Status Valid	AC Test	4.5V ≤ V <sub>CC</sub> ≤ 5.5V	-	-	250	ns
			2.7V ≤ V <sub>CC</sub> ≤ 5.5V			250	
			1.8V ≤ V <sub>CC</sub> ≤ 5.5V			1000	
t <sub>DF</sub>	CS to DO in High Impedance	AC Test CS = VIL	4.5V ≤ V <sub>CC</sub> ≤ 5.5V	-	-	100	ns
			2.7V ≤ V <sub>CC</sub> ≤ 5.5V			100	
			1.8V ≤ V <sub>CC</sub> ≤ 5.5V			400	
t <sub>WP</sub>	Write Cycle Time	-	-	-	1.5	5	ms
Endurance <sup>(1)</sup>	5.0V, 25°C	-	-	1M	-	-	Write Cycle

Note: 1. This parameter is characterized and is not 100% tested.

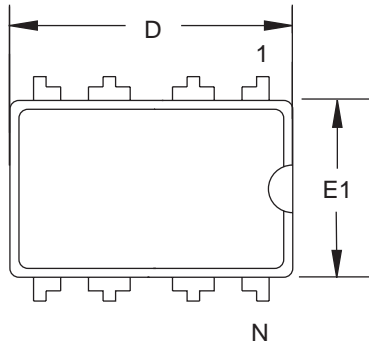
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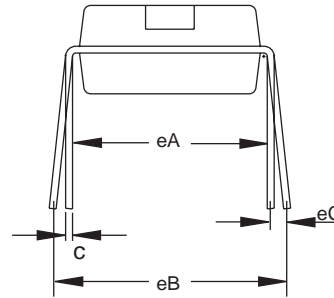
2K bits (256 X 8 or 128 X 16) / 4K bits (512 X 8 or 256 X 16)



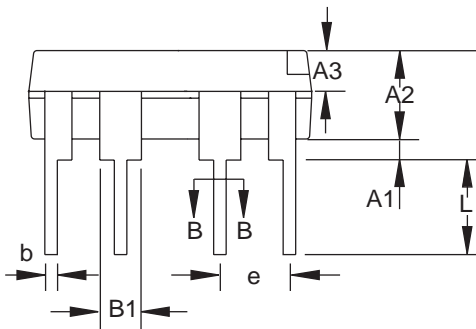
### 8-lead PDIP package diagram



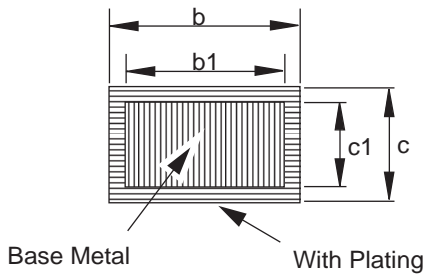
Top View



End View



Side View



Section B-B

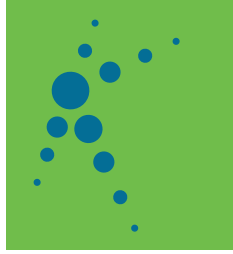
### COMMON DIMENSIONS (Unit of Measure = mm)

SYMBOL	MIN	MAX
A	3.60	4.00
A1	0.51	-
A2	3.10	3.50
A3	1.50	1.70
b	0.44	0.53
b1	0.43	0.48
B	1.52 BSC	
c	0.25	0.31
c1	0.24	0.26
D	9.05	9.45
E1	6.15	6.55
e	2.54 BSC	
eA	7.62 BSC	
eB	7.62	9.50
eC	0	0.94
L	3.00	-

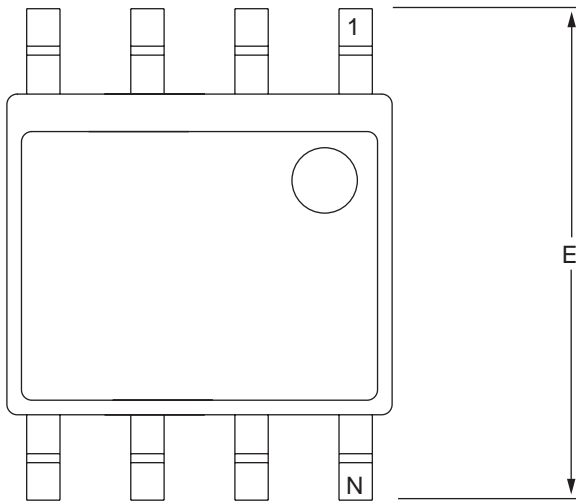
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## Three-wire Serial EEPROM

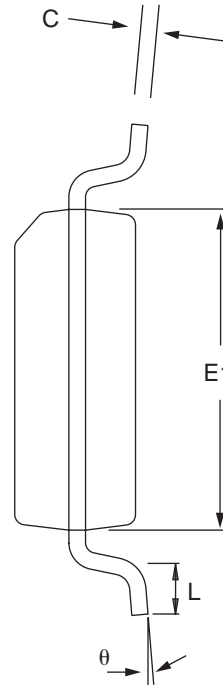
2K bits (256 X 8 or 128 X 16) / 4K bits (512 X 8 or 256 X 16)



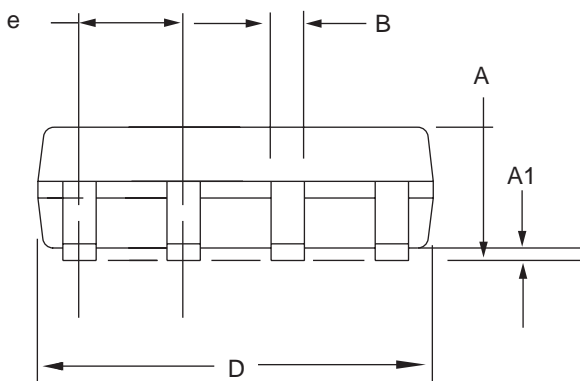
### 8-lead SOP package diagram



Top View



End View



Side View

### COMMON DIMENSIONS

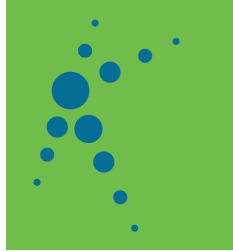
(Unit of Measure = mm)

SYMBOL	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
b	0.31	0.51
C	0.17	0.25
D	4.70	5.10
E1	3.80	4.00
E	5.79	6.20
e	1.27 BSC	
L	0.40	1.27
θ	0°	8°

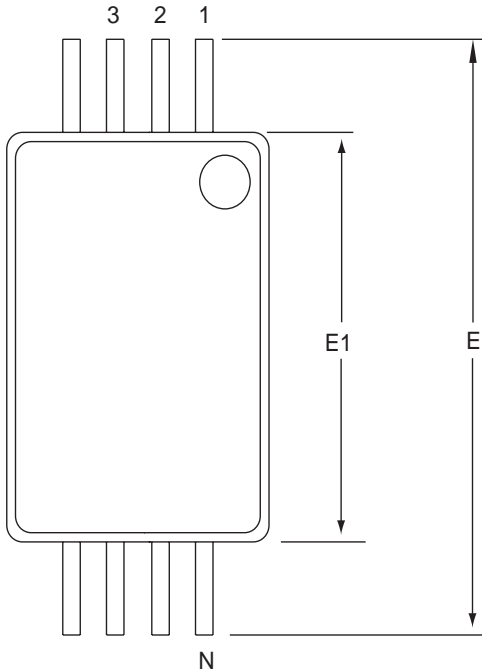
# K93C56/K93C66

## Three-wire Serial EEPROM

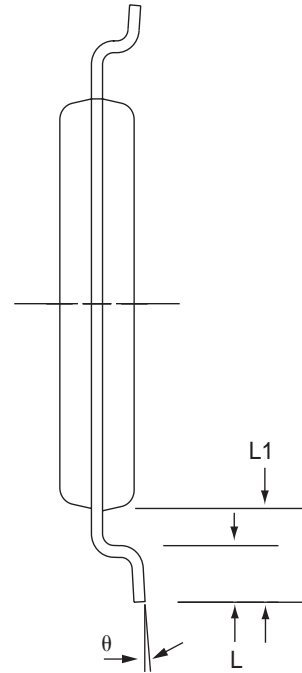
2K bits (256 X 8 or 128 X 16) / 4K bits (512 X 8 or 256 X 16)



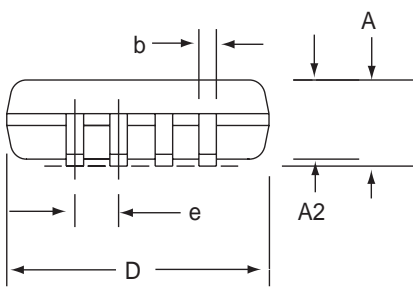
### 8-lead TSSOP package diagram



Top View



End View



Side View

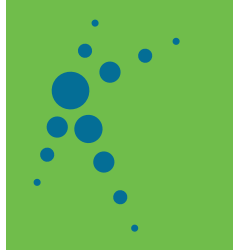
### COMMON DIMENSIONS (Unit of Measure = mm)

SYMBOL	MIN	MAX
D	2.80	3.20
E	6.20	6.60
E1	4.20	4.60
A	-	1.20
A2	0.80	1.15
b	0.19	0.30
e	0.65 BSC	
L	0.45	0.75
L1	1.00 BSC	
$\theta$	0°	8°

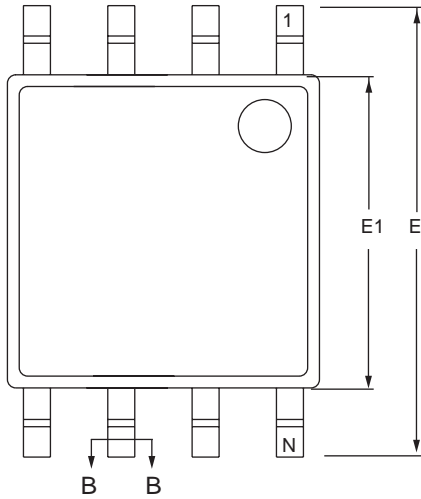
# K93C56/K93C66

## Three-wire Serial EEPROM

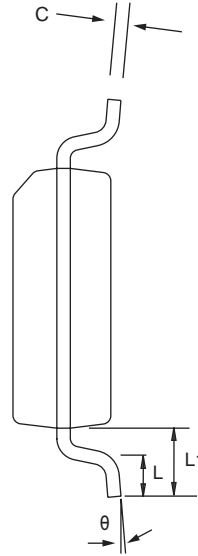
2K bits (256 X 8 or 128 X 16) / 4K bits (512 X 8 or 256 X 16)



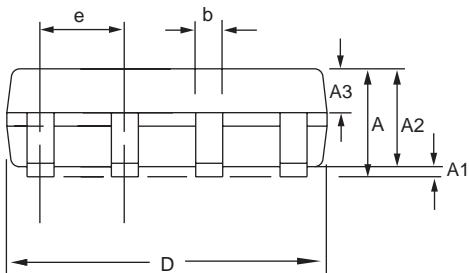
### 8-lead MSOP package diagram



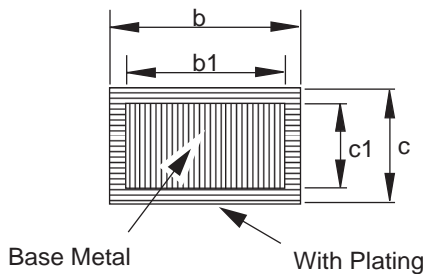
Top View



End View



Side View



Section B-B

### COMMON DIMENSIONS

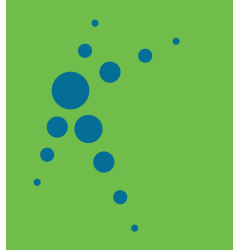
(Unit of Measure = mm)

SYMBOL	MIN	MAX
A	-	1.10
A1	0.05	0.15
A2	0.75	0.95
A3	0.30	0.40
b	0.29	0.38
b1	0.28	0.33
c	0.15	0.20
c1	0.14	0.16
D	2.90	3.10
E	4.70	5.10
E1	2.90	3.10
e	0.65 BSC	
L	0.40	0.70
L1	0.95 BSC	
θ	0°	8°

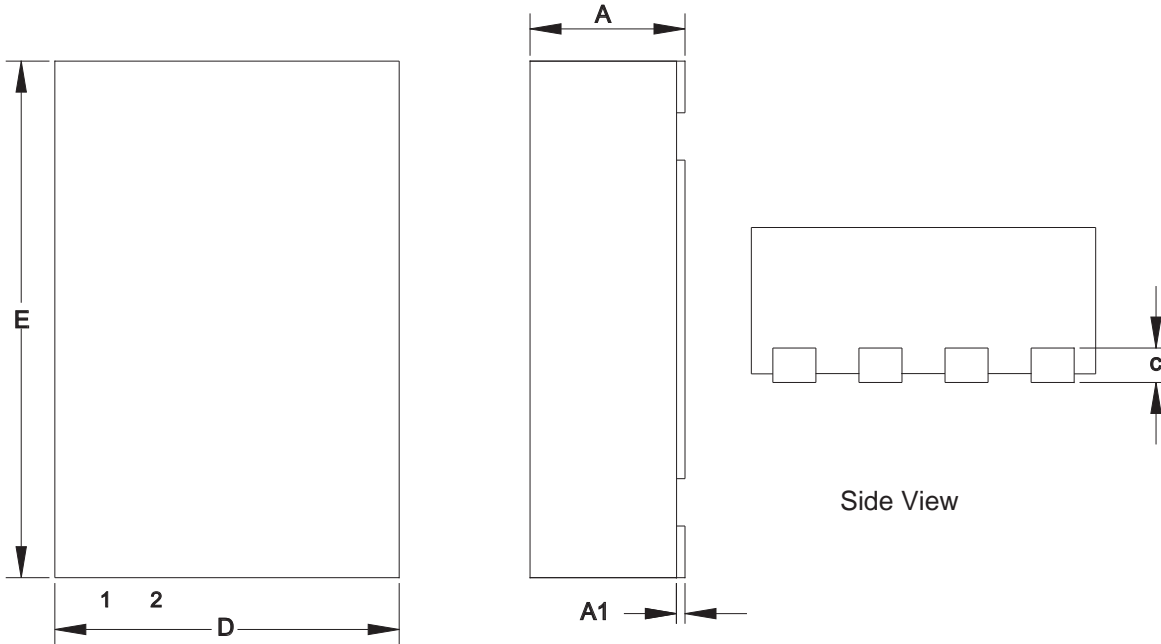
# K93C56/K93C66

## Three-wire Serial EEPROM

2K bits (256 X 8 or 128 X 16) / 4K bits (512 X 8 or 256 X 16)

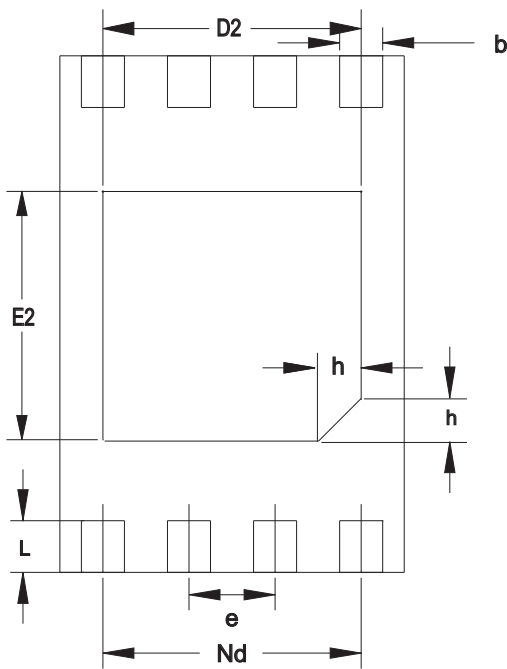


### 8-pad DFN package diagram



Top View

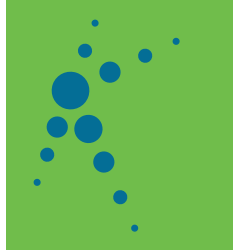
End View



Bottom View

COMMON DIMENSIONS  
(Unit of Measure = mm)

SYMBOL	MIN	MAX
A	0.70	0.80
A1	-	0.05
b	0.18	0.30
c	0.18	0.25
D	1.90	2.10
D2	1.50 REF	
e	0.50 BSC	
Nd	1.50 BSC	
E	2.90	3.10
E2	1.60 BSC	
L	0.30	0.50
h	0.20	0.30



# K93C56/K93C66

## Three-wire Serial EEPROM

2K bits (256 X 8 or 128 X 16) / 4K bits (512 X 8 or 256 X 16)

### Ordering Information

Product Name:	K	93	XXX						
Part Number:	K	93	XXX	-	X	X	X	X	X
	1	2	3	4	5	6	7	8	(version)

- |                                |                 |                               |                               |
|--------------------------------|-----------------|-------------------------------|-------------------------------|
| 1. Prefix                      | 4. Package Type | 5. Temperature Range          | 7. Plating Technology         |
| 2. Series Name                 | D = PDIP        | I = Industry (-40°C to +85°C) | Blank = Standard SnPb plating |
| 93: Three-wire (SPI) Interface | S = SOP         | 6. Pack Type                  | G = RoHS compliant            |
| 3. EEPROM Density              | T = TSSOP       | T = Tube                      | S = Green, level 1            |
| C56 = 2K bits                  | M = MSOP        | R = Tape & Reel               | X = Green, level 3            |
| C66 = 4K bits                  | N = DFN         |                               | 8. Operating Voltage          |
|                                |                 |                               | A = 1.8 to 5.5 V              |

### Available package types

Model	PDIP	SOP	TSSOP	MSOP	DFN
K93C56	√	√	√	√	√
K93C66	√	√	√	√	√

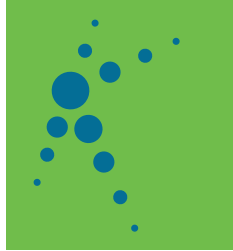
### Product Datasheet Change Notice

Datasheet Revision History		
Version	Content	Date
1.0	Initial version	Dec., 2008
1.1	Package type update	Jan., 2011
1.2	Ordering information update	May, 2011
1.3	Ordering information update	Jan., 2012

# K93C56/K93C66

## Three-wire Serial EEPROM

2K bits (256 X 8 or 128 X 16) / 4K bits (512 X 8 or 256 X 16)



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K93C Series (SPI Bus) Serial EEPROM  
Data Sheet, Revision 1.3

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