LM36272 Two-Channel LCD Backlight Driver With Integrated Bias Power

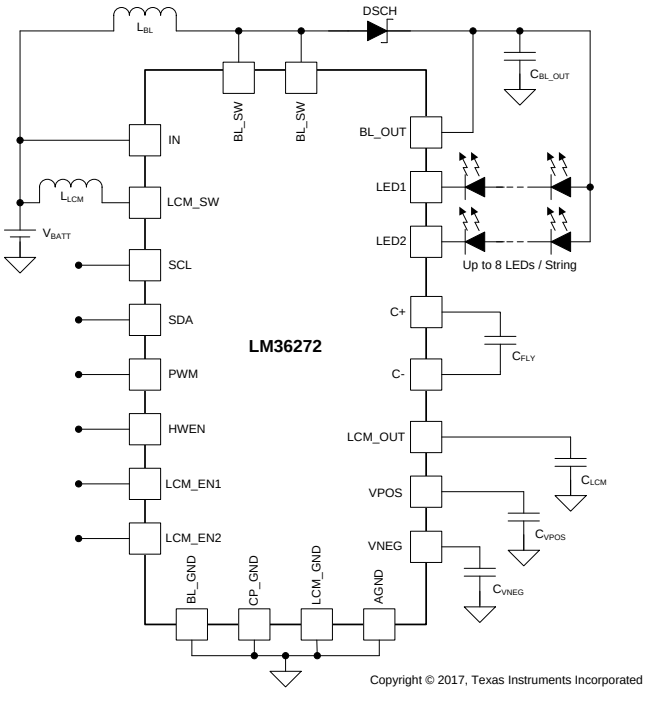
1 Features

- Drives up to Two Parallel White LED Strings (29-V Maximum V_{OUT})
- 11-Bit Exponential and Linear Dimming Control
- PWM and I^2C Brightness Control
- Backlight Operation With 4.7-µH to 15-µH Inductor
- Backlight and LCD Bias Efficiency up to 92%
- Programmable LCD Bias Voltages (±4 V to ±6.5 V With 50-mV resolution) With Up to 80-mA per Output
- 0.2% Matched LED Current From 60 µA to 30 mA
- 1% Accurate LED Current From 60 µA to 30 mA
- 2.7-V to 5-V Input Voltage Range

2 Applications

- LCD Panels With up to 16 LEDs
- Smart Phones
- Tablets and Gaming Tablets
- Home Automation Panels

Simplified Schematic



3 Description

The LM36272 is an integrated two-channel WLED driver and LCD bias supply. The ultra-compact size, high efficiency, high level of integration, and programmability allow the LM36272 to address a variety of applications without the need for hardware changes while minimizing the overall solution area.

The backlight boost provides the power to bias two parallel LED strings with up to 29-V total output voltage. The 11-bit LED current is programmable via the I^2C bus and/or controlled via a logic level PWM input from 60 µA to 30 mA. Each LED string can be independently enabled or disabled to provide zone dimming capabilities. The backlight boost can be operated efficiently with an inductance range from 4.7 µH to 15 µH, allowing for efficiency and solution size optimization.

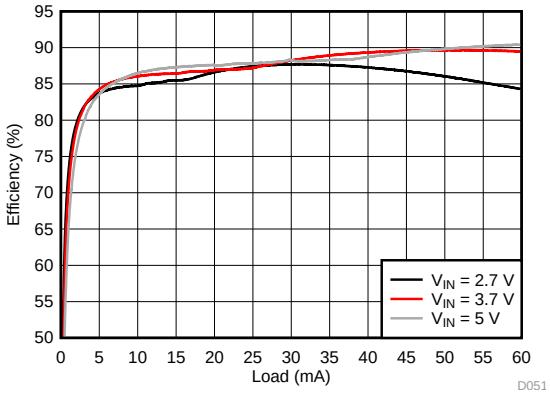
The LCD bias boost provides the power to both a positive LDO and an inverting charge pump. Both positive and negative bias supplies have programmable output voltages of ±4 V to ±6.5 V with 50-mV steps and up to ±80 mA of current capability. An auto-sequencing feature provides a programmed delay from positive to negative bias activation, with additional programmable voltage slew rate control. Two wake-up modes allow both bias outputs to be controlled with a single external signal and stay active while consuming very low quiescent current.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (MAX)
LM36272	DSBGA (24)	2.44 mm × 1.67 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Backlight Efficiency, 2P8S



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (June 2017) to Revision D — **Page**

- Added added silicon rev A1 to revision register. ... 37

Changes from Revision B (March 2017) to Revision C — **Page**

- Changed First public release of full data sheet to WEB ... 1

Changes from Revision A (January 2017) to Revision B — **Page**

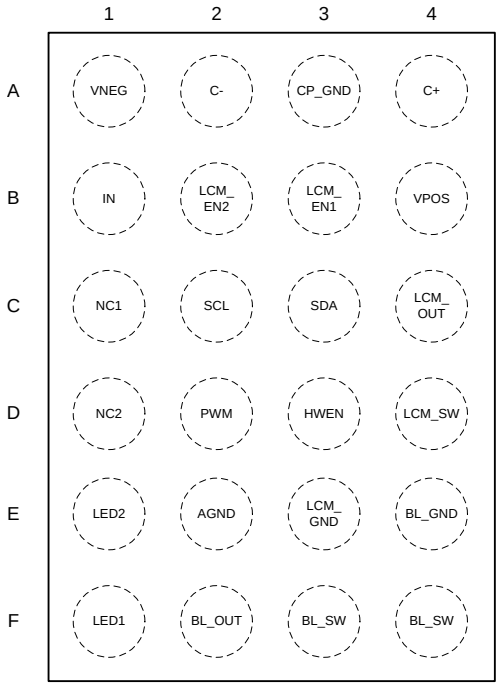
- Changed row(s) in *Abs Max* table: BL_SW from 30 V to 35 V, BL_OUT and current sink inputs (LEDX) remain at 30 V ... 5

Changes from Original (February 2016) to Revision A — **Page**

- Changed "Orderable Device" suffix on POA from "YFRR" to "YFFR" ... 1

5 Pin Configuration and Functions

YFF Package
24-Pin DSBGA
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NUMBER	NAME		
A1	VNEG	O	Inverting charge pump output. Bypass VNEG with a 10-µF ceramic capacitor to CP_GND.
A2	C-	O	Inverting charge-pump flying capacitor negative connection
A3	CP_GND	—	Charge pump GND. Connect the CNEG capacitor negative terminal to this pin.
A4	C+	O	Inverting charge-pump flying capacitor positive connection
B1	IN	I	Input voltage connection. Bypass IN with a 10-µF ceramic capacitor to GND.
B2	LCM_EN2	I	Enable for LCD bias negative output; 300-kΩ internal pulldown resistor between LCM_EN2 and GND.
B3	LCM_EN1	I	Enable for LCD bias positive output; 300-kΩ internal pulldown resistor between LCM_EN1 and GND.
B4	VPOS	O	Positive LCD bias output. Bypass VPOS with a 10-µF ceramic capacitor to GND.
C1	NC2	—	No connect; leave this pin disconnected
C2	SCL	I	Serial clock connection for I^2C-compatible interface
C3	SDA	I/O	Serial clock connection for I^2C-compatible interface
C4	LCM_OUT	O	LCD bias boost output voltage. Bypass LCM_OUT with a 10-µF ceramic capacitor to LCM_GND.
D1	NC1	—	No connect; leave this pin disconnected
D2	PWM	I	PWM input for duty cycle current control; 300-kΩ internal pulldown resistor between PWM and GND.
D3	HWEN	I	Active high chip enable; 300-kΩ internal pulldown resistor between HWEN and GND.
D4	LCM_SW	O	LCD bias boost inductor connection
E1	LED2	I	Current sink 2 input. Connect the cathode of LED string 2 to this pin. Leave this pin disconnected if not used.

Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NUMBER	NAME		
E2	AGND	—	Analog ground connection. Connect AGND directly to GND on the PCB.
E3	LCM_GND	—	LCD bias boost GND connection. Connect LCM_GND to the negative terminal of the LCD bias output capacitor.
E4	BL_GND	—	Backlight boost output capacitor GND connection
F1	LED1	I	Current sink 1 input. Connect the cathode of LED string 1 to this pin. Leave this pin disconnected if not used.
F2	BL_OUT	O	Backlight boost output voltage sense connection. Connect to the positive terminal of backlight boost output capacitor.
F3	BL_SW	O	Backlight boost inductor connection
F4	BL_SW	O	Backlight boost inductor connection

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
Voltage on IN, HWEN, LCM_EN1, LCM_EN2, SCL, SDA, PWM	–0.3	6	V
Voltage on LCM_SW, LCM_OUT, VPOS, C+	–0.3	9	V
Voltage on VNEG, C–	–7	0.3	V
Voltage on BL_SW	–0.3	35	V
Voltage on BL_OUT, LED1, LED2	–0.3	30	V
Continuous power dissipation	Internally limited		
Maximum junction temperature, $T_{J(MAX)}$		150	°C
Storage temperature, T_{stg}	–45	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the AGND pin.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)(1) (2).

	MIN	MAX	UNIT
Input voltage, V_{IN}	2.7	5	V
Operating ambient temperature, T_A(3)	–40	85	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the AGND pin.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to-ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (R_{\theta JA} \times P_{D-MAX})$.

6.4 Thermal Information

THERMAL METRIC(1)		LM36272 DSBGA (YFF) (24 PINS)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	63.1	°C/W
$R_{\theta JC}$	Junction-to-case (top) thermal resistance	0.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	11.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Unless otherwise specified, typical limits apply at 25°C, minimum and maximum limits apply over the full operating ambient temperature range (−40°C ≤ T_A ≤ 85°C), and V_{IN} = 3.6 V.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
CURRENT CONSUMPTION							
I_{SD}	Shutdown current	HWEN = 0			0.2	2.8	µA
I_Q	Quiescent current, device not switching	HWEN = V_{IN}, LCM boost disabled			1	7	µA
I_{LCM_EN}	Bias power no load supply current	VPOS, VNEG enabled with no load, backlight boost disabled, typical application circuit (not ATE tested)			0.5	10	µA
BACKLIGHT LED CURRENT SINKS (LED1, LED2, LED3, LED4)							
I_{LED_MAX}	Maximum output current (per string)	2.7 V ≤ V_{IN} ≤ 5 V, linear or exponential mode			30		mA
I_{LED}	LED current accuracy(1)	2.7 V ≤ V_{IN} ≤ 5 V, 60 µA < I_{LED} < 30 mA, linear or exponential mode		–3%		3%	
I_{MATCH}	I_{LED} current matching(2)	2.7 V ≤ V_{IN} ≤ 5 V, 60 µA ≤ I_{LED} ≤ 30 mA, linear or exponential mode		–2%	0.2%	2%	
I_{LED_MIN}	Minimum LED current (per string)	Linear or exponential mode			60		µA
I_{STEP}	LED current step size (code to code)	Exponential mode(3)			0.3%		
		Linear mode			14.63		µA
BACKLIGHT BOOST							
OVP threshold		ON threshold, 2.7 V ≤ V_{IN} ≤ 5 V	011 to 111	28.5	29	29.5	V
			010	24.5	25	25.5	
			001	20.5	21	21.5	
			000	16.3	17	17.7	
OVP hysteresis		OFF threshold			0.5		V
Efficiency	Boost efficiency	V_{IN} = 3.6 V, I_{BLED} = 5 mA/string, (P_{OUT}/P_{IN}), Typical Application Circuit (not ATE tested)			90%		
V_{HR}	Regulated current-sink headroom voltage (boost feedback voltage)	I_{LED} = 30 mA			310		mV
		I_{LED} = 5 mA			120		mV
V_{HR_MIN}	Current-sink minimum headroom voltage	I_{LED} = 95% of nominal, I_{LED} = 5 mA			30	50	mV
R_{DSON}	NMOS switch on resistance	I_{SW} = 250 mA			0.2		Ω
I_{CL}	NMOS switch current limit	2.7 V ≤ V_{IN} ≤ 5 V	00	792	900	1008	mA
			01	1056	1200	1344	mA
			10	1320	1500	1680	mA
			11	1584	1800	2016	mA
f_{BL_SW}	Switching frequency	2.7 V ≤ V_{IN} ≤ 5 V	500-kHz mode	450	500	550	kHz
			1-MHz mode	900	1000	1100	
D_{MAX}	Maximum duty cycle	V_{IN} = 2.7 V, f_{LED_SW} = 1 MHz		93%	94%		
DEVICE PROTECTION							
TSD	Thermal shutdown	Not ATE tested			140		°C

(1) Output current accuracy is the difference between the actual value of the output current and programmed value of this current.
(2) LED current matching is the maximum difference between any string current and the average string current, divided by the average string current. This is calculated as (I_{LEDX} – I_{LED_AVE}) / I_{LED_AVE} × 100.
(3) LED current step size from code to code in exponential mode is typically 0.304%, given as (1 – ($I_{LED(CODE+1)}$) / $I_{LED(CODE)}$).

Electrical Characteristics (continued)

Unless otherwise specified, typical limits apply at 25°C, minimum and maximum limits apply over the full operating ambient temperature range (−40°C ≤ T_A ≤ 85°C), and V_{IN} = 3.6 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DISPLAY BIAS (LCM BOOST)						
V_{OVP_LCM}	LCM bias boost overvoltage protection	On threshold, 2.7 V ≤ V_{IN} ≤ 5 V		7.8		V
f_{LCM_SW}	Switching frequency(4)	2.7 V ≤ V_{IN} ≤ 5 V (continuous conduction mode)		2500		kHz
V_{LCM_OUT}	LCM boost output voltage range		4		7.15	V
	Efficiency	V_{IN} = 3.6 V, V_{LCM_OUT} = 5.9 V, 6 mA < I_{LCM_OUT} < 160mA, Typical Application Circuit (not ATE tested)		92%		
	Output voltage step size			50		mV
$I_{LCM\_BOOST\_CL}$	Valley current limit			1000		mA
R_{DSON_LCM}	High-side MOSFET on resistance	V_{IN} = V_{GS} = 3.6 V		170		mΩ
	Low-side MOSFET on Resistance	V_{IN} = V_{GS} = 3.6 V		290		
$V_{LCM\_OUT\_RIPPLE}$	Peak-to-peak ripple voltage(4)	$I_{LOAD\_LCM\_BOOST}$ = 5 mA and 50 mA, C_{BST} = 20 µF		50		mVpp
$V_{LCM\_OUT\_LINE\_TRANSIENT}$	LCM_OUT line transient response(4)	V_{IN} + 500 mVp-p AC square wave, Tr = 100 mV/µs, 200 Hz, 12.5% DS at 5 mA, I_{LOAD} = 5 mA, C_{IN} = 10 µF	–50	±25	50	mV
$V_{LCM\_OUT\_LOAD\_TRANSIENT}$	LCM_OUT load transient response(4)	0 mA to 150 mA, $t_{RISE/FALL}$ = 100 mA/µs, C_{IN} = 10 µF	–150		150	mV
$t_{LCM\_OUT\_ST}$	Start-up time (LCM_OUT), V_{LCM_OUT} = 10% to 90%(4)	C_{LCM_OUT} = 20 µF			1000	µs
DISPLAY BIAS POSITIVE OUTPUT (VPOS)						
V_{VPOS}	Programmable output voltage range		4		6.5	V
	Output voltage step size			50		mV
	Output voltage accuracy	Output voltage = 5.4 V	–1.5%		1.5%	
I_{VPOS_MAX}	Maximum output current		80			mA
I_{VPOS_CL}	Output current limit			180		mA
$I_{RUSH\_PK\_VPOS}$	Peak start-up inrush current(4)	V_{LCM_OUT} = 6.3 V, V_{POS} = 5.8 V, C_{VPOS} = 10 µF (nominal)			250	mA
$V_{VPOS\_LINE\_TRANSIENT}$	LDO_VPOS line transient response(4)	V_{IN} + 500 mVp-p AC square wave, Tr = 100 mV/µs, 200 Hz at 25 mA, C_{IN} = 10 µF (nominal)	–50		50	mV
$V_{VPOS\_LOAD\_TRANSIENT}$	LDO_VPOS load transient response(4)	Load current step 0 mA to 50 mA, C_{VPOS} = 10 µF (nominal)	–50		50	mV
$V_{VPOS\_DC\_REG}$	DC load regulation(4)	0 mA ≤ I_{LOAD_VPOS} ≤ $I_{LOAD\_VPOS\_MAX}$			20	mV
V_{DO_VPOS}	VPOS dropout voltage(5)	I_{LOAD_VPOS} = $I_{LOAD\_VPOS\_MAX}$ V_{VPOS} = 5.7 V			160	mV
$PSSR_{VPOS}$	Power supply rejection ratio (LDO_VPOS)(4)	f = 10 Hz to 500 kHz at I_{MAX}/2 V_{LCM_OUT} – V_{VPOS} ≥ 300 mV	25			dB
t_{ST_VPOS}	Start-up time (LDO_VPOS)(6) V_{VPOS} = 10% to 90%(4)	C_{VPOS} = 10 µF v		800		µs
R_{PD_VPOS}	Output pulldown resistor (VPOS)	VPOS pulldown in shutdown	30	80	270	Ω
Pulldown resistance on LCM_EN1		Not ATE tested		300		kΩ

(4) Limits set by characterization and/or simulation only.
(5) V_{IN_VPOS} – V_{VPOS} when V_{VPOS} has dropped 100 mV below target.
(6) Typical value only for information.

Electrical Characteristics (continued)

Unless otherwise specified, typical limits apply at 25°C, minimum and maximum limits apply over the full operating ambient temperature range (−40°C ≤ T_A ≤ 85°C), and V_{IN} = 3.6 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DISPLAY BIAS NEGATIVE OUTPUT (VNEG)						
V_{NEG_SHORT}	NEG output short circuit protection	V_{NEG} to CP_GND, VNEG rises to % of target		84%		
V_{VNEG}	Efficiency(6)	V_{LCM_OUT} = 5.7 V, V_{NEG} = –5.4 V, I_{NEG} > –5 mA		92%		
	Programmable output voltage range		–6.5		–4	V
	Output voltage step size			50		mV
	Output accuracy	Output voltage = –5.4 V	–1.5%		1.5%	
$I_{LOAD\_VNEG\_MAX}$	Maximum output current	V_{LCM_OUT} = 5.9 V, V_{NEG} = –5.4 V	80			mA
I_{VNEG_CL}	Output current limit			135		mA
R_{DSON_VNEG}	CP FET ON resistance	Q1		350		mΩ
		Q2		240		
		Q3		240		
V_{VNEG_RIPPLE}	Peak-to-peak ripple voltage(4)	I_{NEG} = –5 mA and –50 mA, C_{VNEG} = 10 µF (nominal)			60	mVpp
$V_{VNEG\_LINE\_TRANSIENT}$	VNEG line transient response(4)	V_{IN} + 500 mVp-p AC square wave, 100 mV/µs 200 Hz, 12.5% duty at 5 mA	–50	±25	50	mV
$V_{VNEG\_LOAD\_TRANSIENT}$	V_{VNEG} load transient response(4)	0 to –50 mA step, $t_{RISE/FALL}$ = 1 µs, C_{VNEG} = 10 µF (nominal)			100	mV
t_{SU_VNEG}	V_{VNEG} start-up time, V_{VNEG} = 10% to 90%(4)	V_{VNEG} = –6.5 V, C_{VNEG} = 10 µF (nominal)			1	ms
R_{VNEG}	Output pullup resistor (VNEG to CP_GND)(4)	VNEG pullup in shutdown		6	20	Ω
Pulldown resistance on LCM_EN2		Not ATE tested		300		kΩ
PWM INPUT						
f_{PWM_INPUT}	PWM input frequency(6)	2.7 V ≤ V_{IN} ≤ 5 V	50		50000	Hz
t_{MIN_ON}	Minimum pulse ON time(4)	24-MHz sample rate	183.3			ns
		4-MHz sample rate	1100			
		1-MHz sample rate	4400			
t_{MIN_OFF}	Minimum pulse OFF timet(4)	24-MHz sample rate	183.3			ns
		4-MHz sample rate	1100			
		1-MHz sample rate	4400			
$t_{START-UP}$	Turnon delay from PWM = 0 to PWM = 50% duty cycle	4-MHz sample rate		3.5		ms
PWM_{RES}	PWM input resolution	50 Hz < f_{PWM} < 11 kHz		11		bits
t_{GLITCH}	PWM input glitch rejection	Filter = 00		0		ns
		Filter = 01		100		
		Filter = 10		150		
		Filter = 11		200		
LOGIC INPUTS (PWM, HWEN, EN_POS, EN_NEG, SCL, SDA, EN_BL)						
V_{IL}	Input logic low	2.7 V ≤ V_{IN} ≤ 5 V	0		0.4	V
V_{IH}	Input logic high	2.7 V ≤ V_{IN} ≤ 5 V	1.2		V_{IN}	V
LOGIC OUTPUTS (SDA)						
V_{OL}	Output logic low	2.7 V ≤ V_{IN} ≤ 5 V, I_{OL} = 3 mA			0.4	V

6.6 I²C Timing Requirements (Fast Mode)

Over operating free-air temperature range; limits apply over 2.5 V ≤ V_{IN} ≤ 5 V (unless otherwise noted). See Figure 1.

			MIN	MAX	UNIT
t_{LOW_SCL}	SCL low clock period		0.5		µs
t_{HIGH_SCL}	SCL high clock period		0.26		µs
f_{SCL}	SCL clock frequency		1		MHz
t_{SU_DAT}	Data in setup time to SCL high		50		ns
t_{V_DAT}	Data valid time			0.45	µs
t_{HD_DAT}	Data out stable after SCL low		0		
t_{START}	SDA low setup time to SCL low (start)		260		ns
t_{STOP}	SDA high hold time after SCL high (stop)		260		ns
t_{RISE}	SDA/SCL rise time	V_{PULLUP} = 1.8 V, R_{PULLUP} = 1 kΩ, C_{BUS} = 100 pF		120	ns
t_{FALL}	SDA/SCL fall time	V_{PULLUP} = 1.8 V, R_{PULLUP} = 1 kΩ, C_{BUS} = 100 pF		120	ns

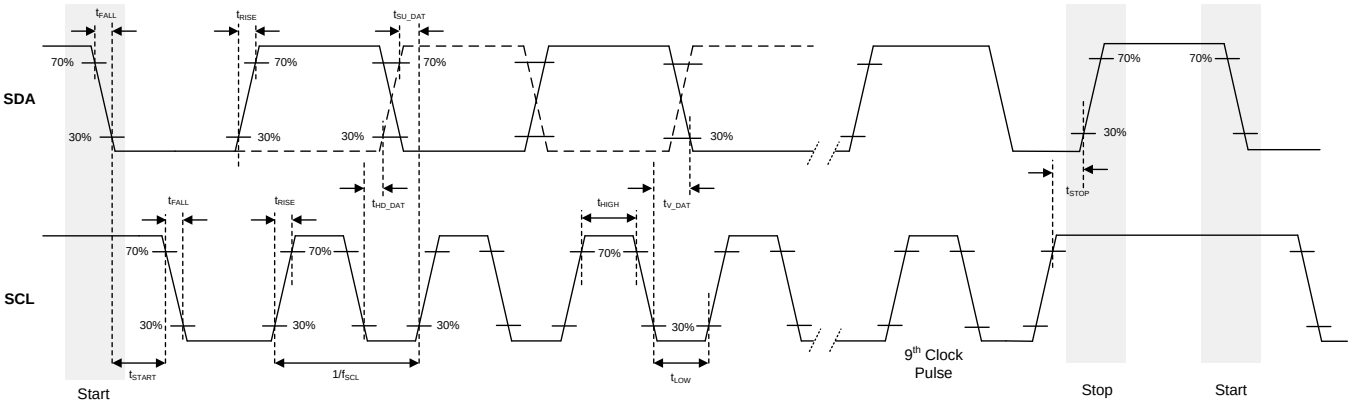


Figure 1. I²C Timing Parameters

6.7 Typical Characteristics

Ambient temperature is 25°C and V_{IN} is 3.7 V unless otherwise noted.

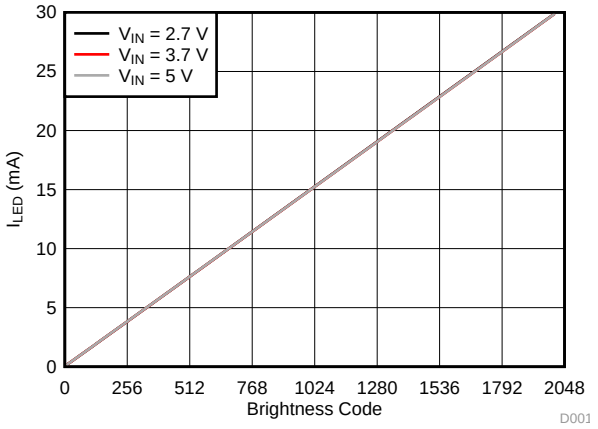


Figure 2. Backlight LED Current, Linear Control

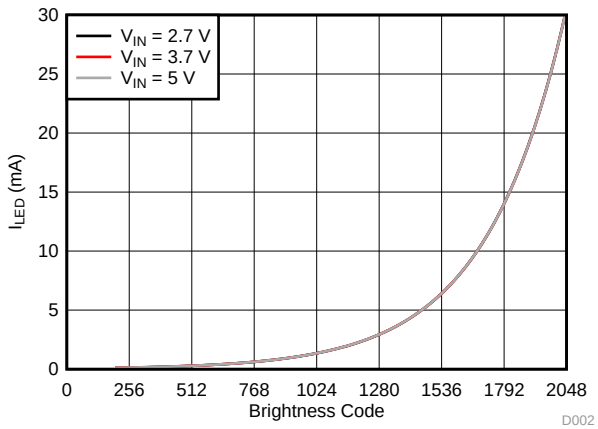


Figure 3. Backlight LED Current, Exponential Control

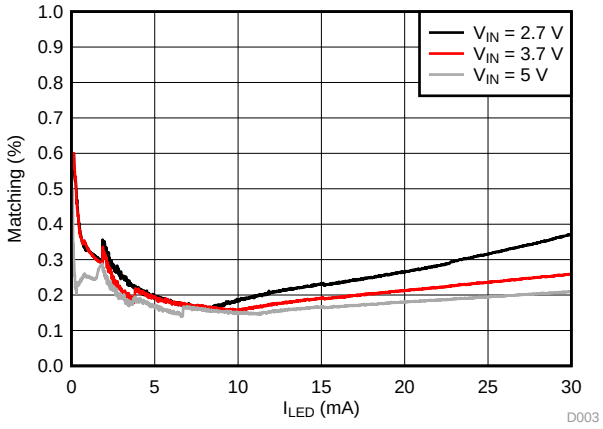


Figure 4. Backlight LED Current Matching

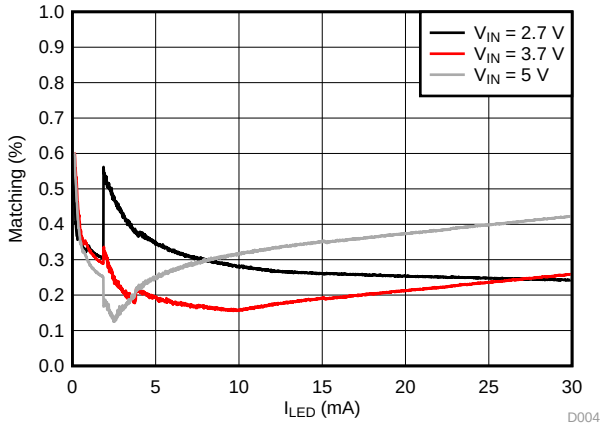


Figure 5. Backlight LED Current Matching

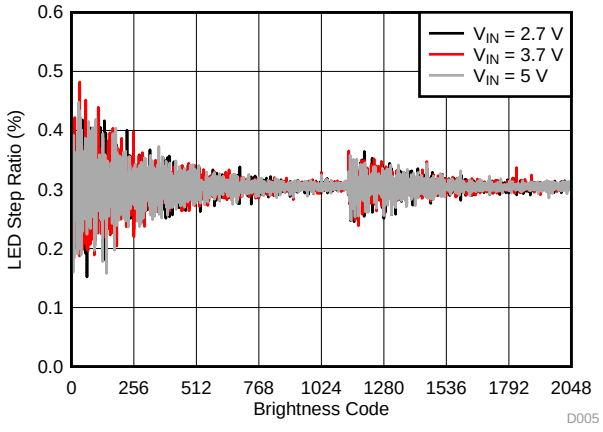


Figure 6. Backlight LED Current-Step Ratio

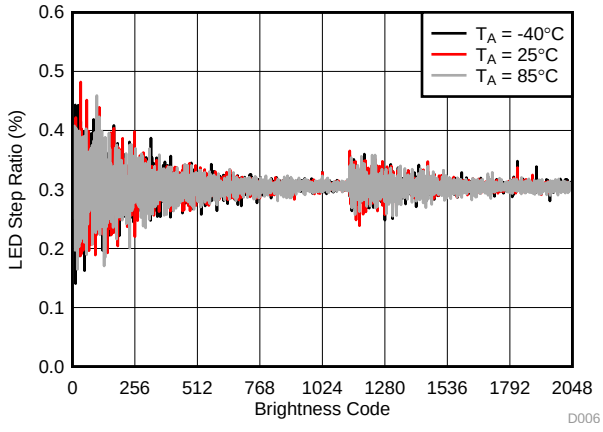


Figure 7. Backlight LED Current-Step Ratio

Typical Characteristics (continued)

Ambient temperature is 25°C and V_{IN} is 3.7 V unless otherwise noted.

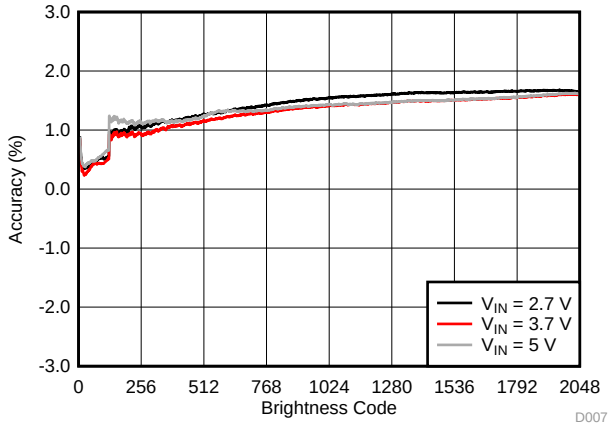


Figure 8. Backlight LED Current Accuracy

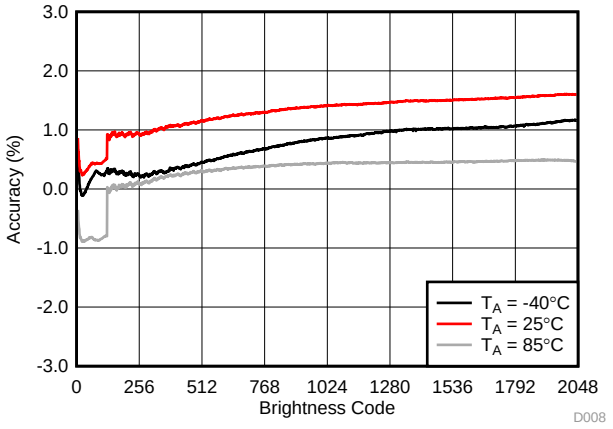
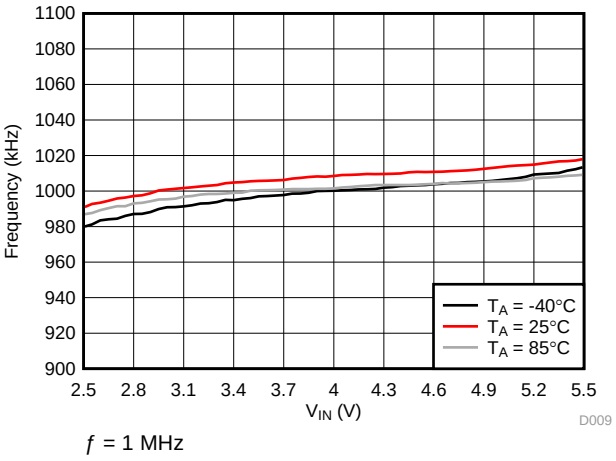
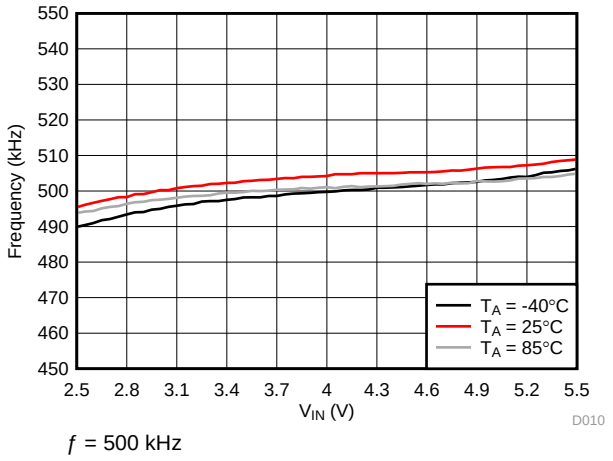


Figure 9. Backlight LED Current Accuracy



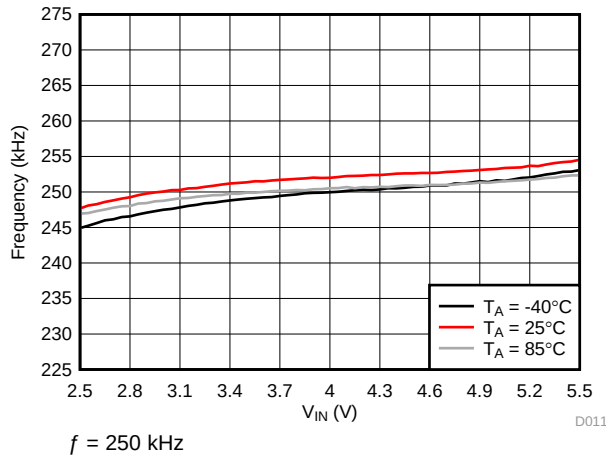
f = 1 MHz

Figure 10. Backlight Boost Frequency



f = 500 kHz

Figure 11. Backlight Boost Frequency



f = 250 kHz

Figure 12. Backlight Boost Frequency

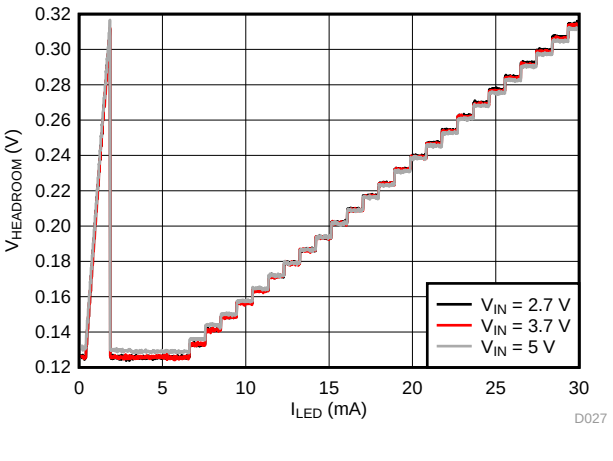


Figure 13. Backlight Regulated Headroom Voltage

Typical Characteristics (continued)

Ambient temperature is 25°C and V_{IN} is 3.7 V unless otherwise noted.

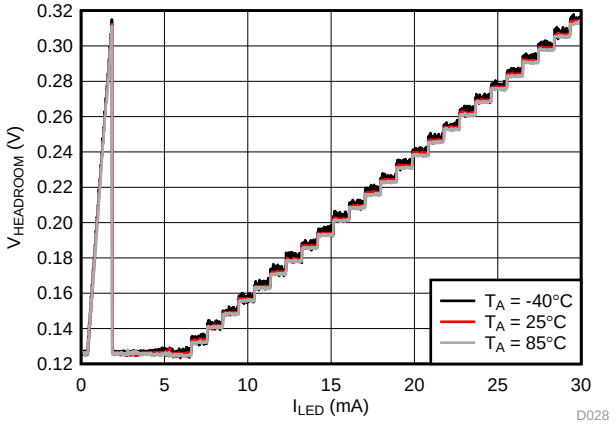
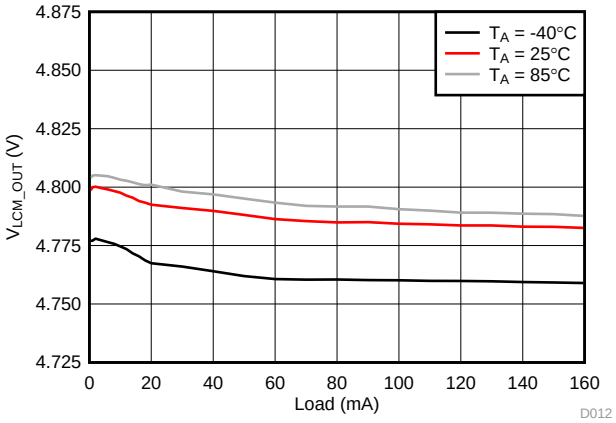
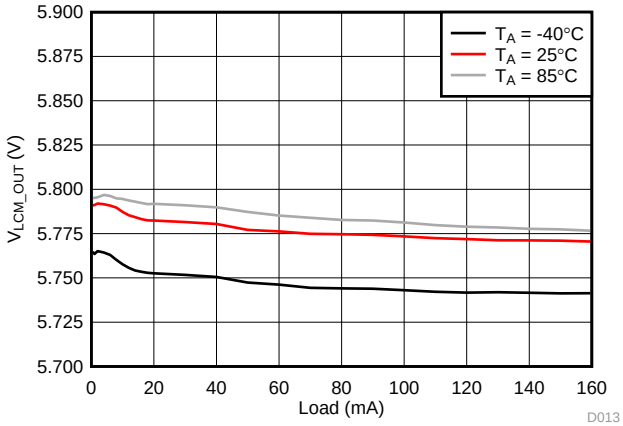


Figure 14. Backlight Regulated Headroom Voltage



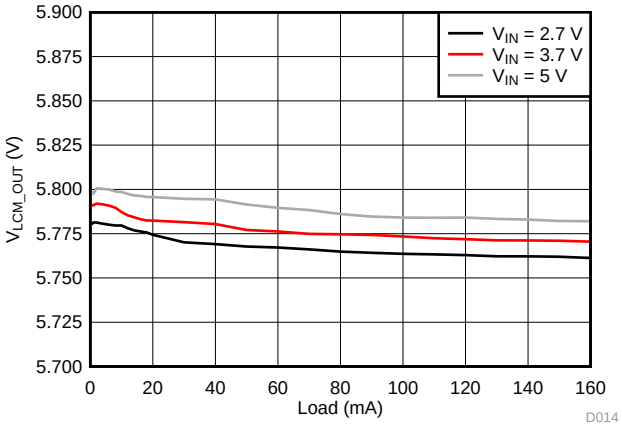
V_{LCM_OUT} = 4.8 V

Figure 15. V_{LCM_OUT} Load Regulation



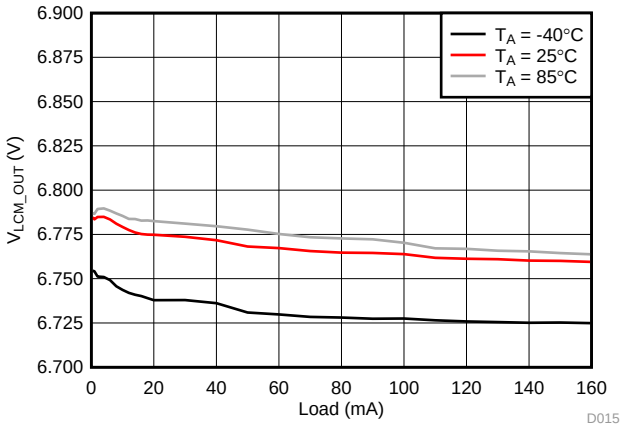
V_{LCM_OUT} = 5.8 V

Figure 16. V_{LCM_OUT} Load Regulation



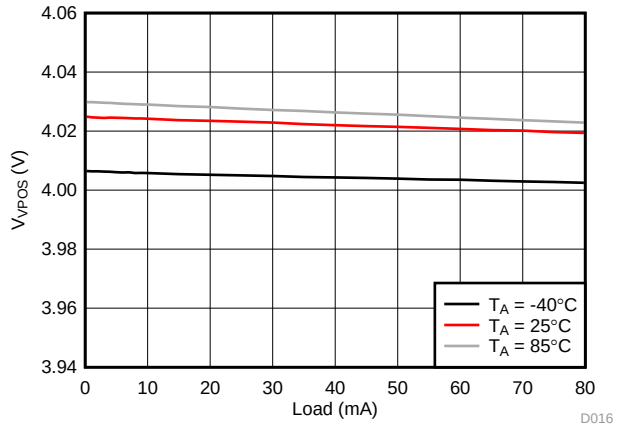
V_{LCM_OUT} = 5.8 V

Figure 17. V_{LCM_OUT} Load Regulation



V_{LCM_OUT} = 6.8 V

Figure 18. V_{LCM_OUT} Load Regulation

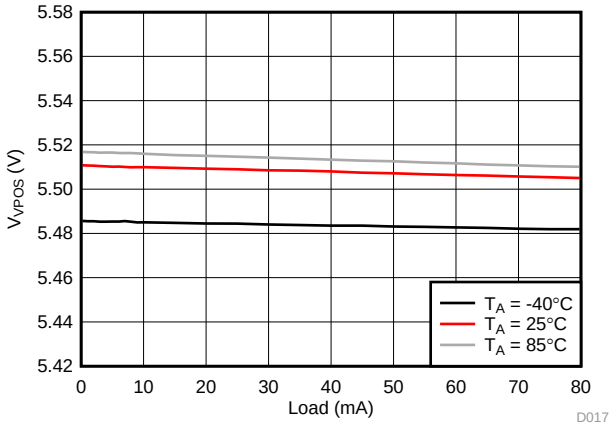


V_{VPOS} = 4 V V_{LCM_OUT} = 4.3 V

Figure 19. V_{VPOS} Load Regulation

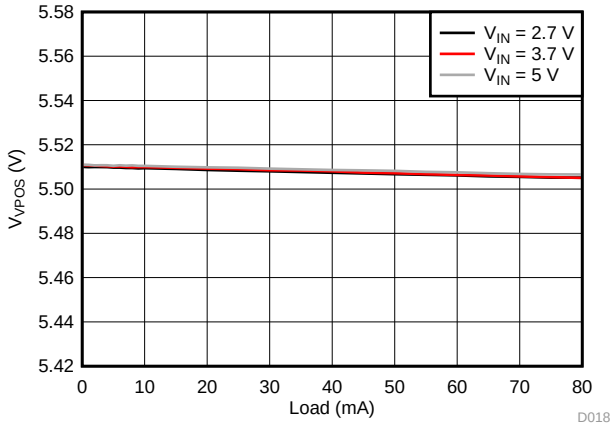
Typical Characteristics (continued)

Ambient temperature is 25°C and V_{IN} is 3.7 V unless otherwise noted.



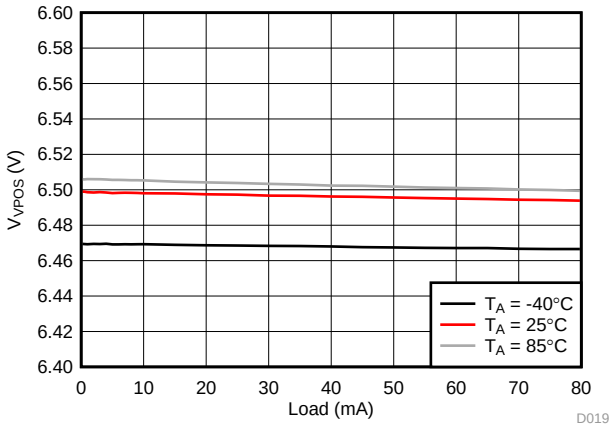
V_{VPOS} = 5.5 V V_{LCM_OUT} = 5.8 V

Figure 20. V_{VPOS} Load Regulation



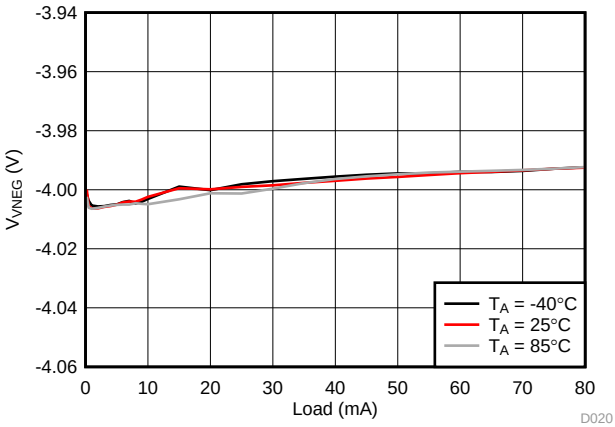
V_{VPOS} = 5.5 V V_{LCM_OUT} = 5.8 V

Figure 21. V_{VPOS} Load Regulation



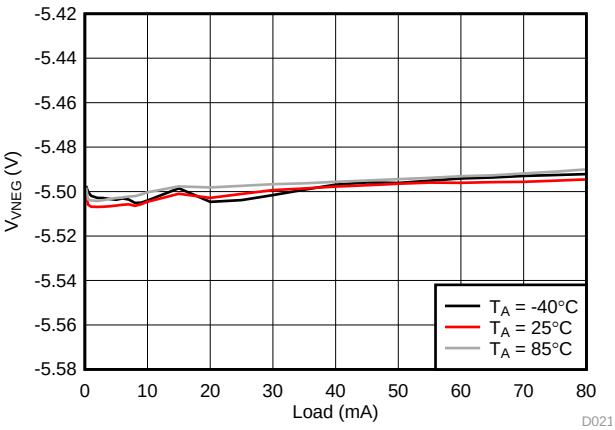
V_{VPOS} = 6.5 V V_{LCM_OUT} = 6.8 V

Figure 22. V_{VPOS} Load Regulation



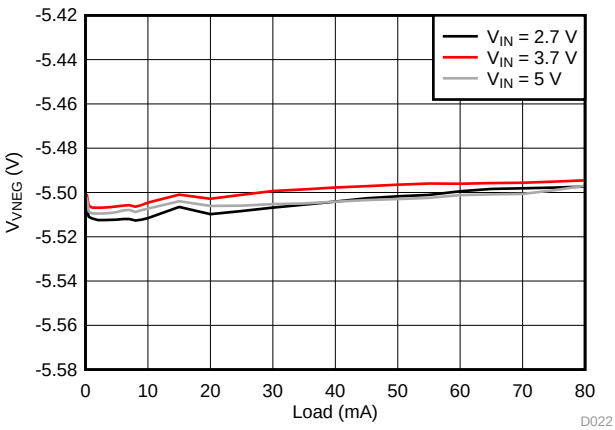
V_{VNEG} = –4 V V_{LCM_OUT} = 4.3 V

Figure 23. V_{VNEG} Load Regulation



V_{VNEG} = –5.5 V V_{LCM_OUT} = 5.8 V

Figure 24. V_{VNEG} Load Regulation

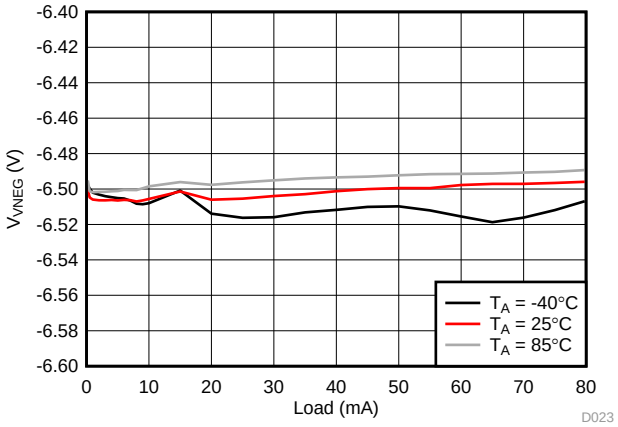


V_{VNEG} = –5.5 V V_{LCM_OUT} = 5.8 V

Figure 25. V_{VNEG} Load Regulation

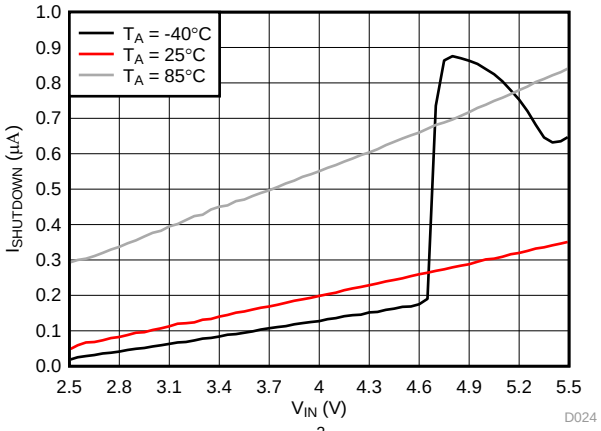
Typical Characteristics (continued)

Ambient temperature is 25°C and V_{IN} is 3.7 V unless otherwise noted.



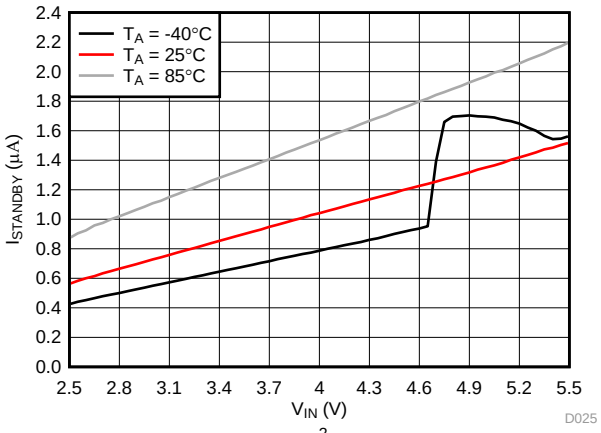
V_{VNEG} = –6.5 V V_{LCM_OUT} = 6.8 V

Figure 26. V_{VNEG} Load Regulation



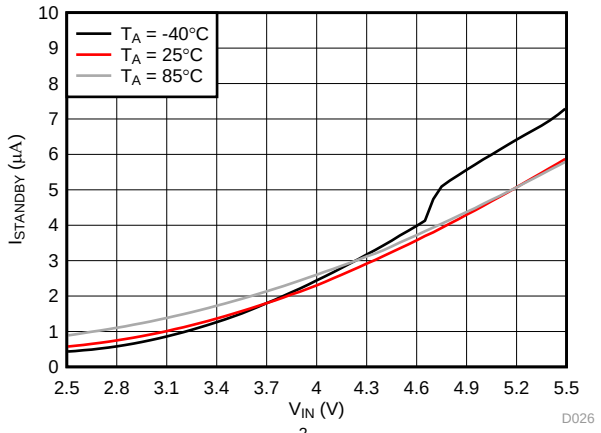
V_{HWEN} = 0 V I^2C = 0 V

Figure 27. Iq Shutdown



$V_{HWEN} = V_{IN}$ $I^2C = V_{IN}$

Figure 28. I_Q Standby



V_{HWEN} = 1.8 V I^2C = 1.8 V

Figure 29. I_Q Standby

7 Detailed Description

7.1 Overview

The LM36272 is a single-chip, complete backlight and LCM power solution. The device operates over the 2.7-V to 5-V input voltage range.

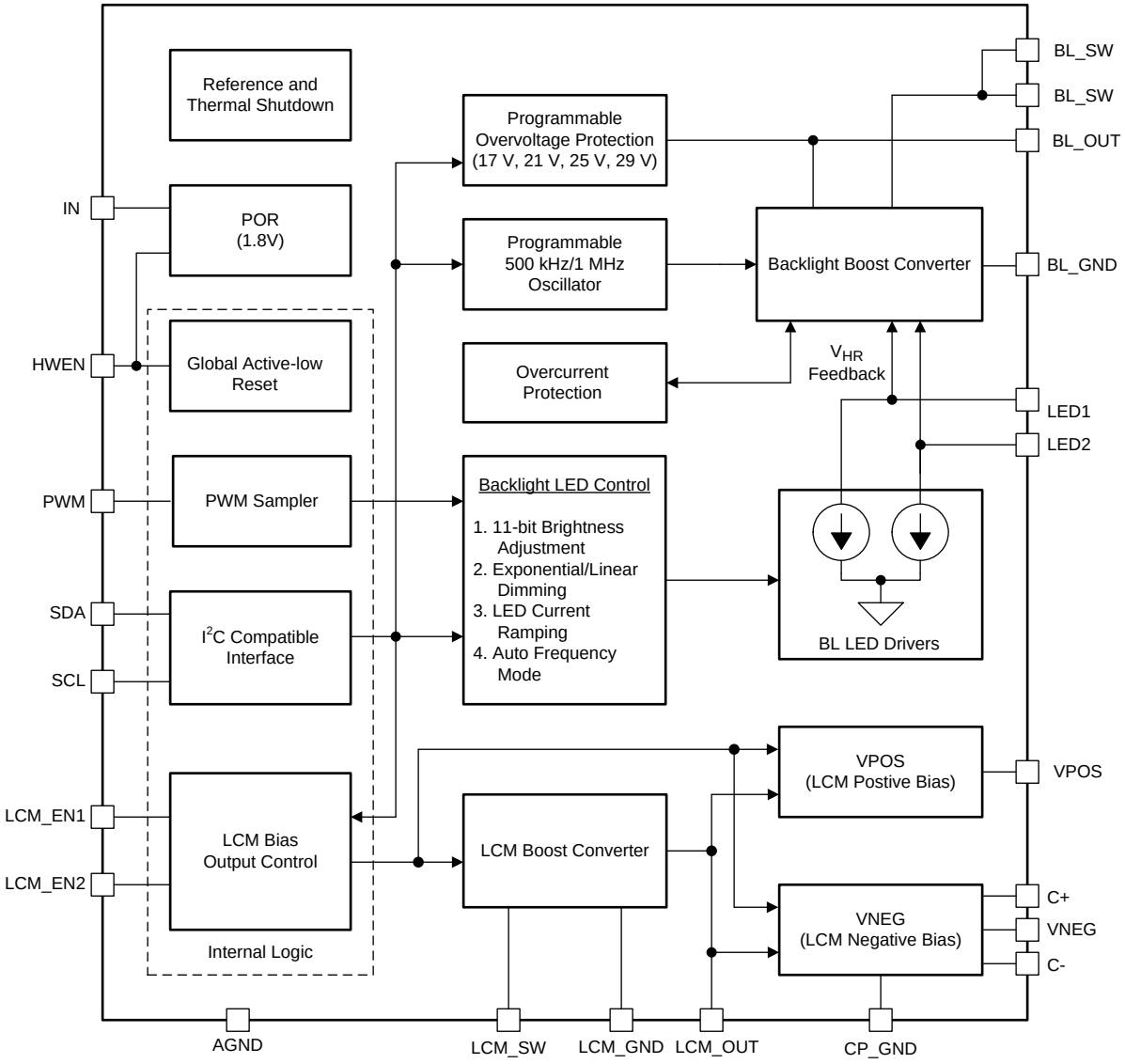
The backlight block consists of an inductive boost plus two current sink white-LED drivers designed to power from one to two LED strings with up to eight LEDs each (up to 28 V typical), with a maximum of 30 mA per string. A higher number of LEDs per string can be supported if the total output power requirement for the boost does not exceed 2.5 Watts. The power for the LED strings comes from an integrated asynchronous backlight boost converter with three selectable switching frequencies to optimize performance or solution area. LED current is regulated by the low-headroom current sinks. The inductive backlight boost automatically adjusts its output voltage to keep the active current sinks in regulation, while minimizing current sink headroom voltage. The 11-bit LED current is set via an I^2C interface, via a logic level PWM input, or a combination of both.

The LCM bias power portion of the LM36272 consists of a synchronous LCM bias boost converter, inverting charge pump, and an integrated LDO. The LCM positive bias voltage VPOS (up to 6.5 V) is post-regulated from the LCM bias boost converter output voltage. The LCM negative bias voltage VNEG (down to –6.5 V) is generated from the LCM bias boost converter output using a regulated inverting charge pump.

The LM36272 flexible control interface consists of an HWEN active low reset input, LCM_EN1 and LCM_EN2 inputs for VPOS and VNEG enable control, PWM input for content adaptive backlight control (CABC), and an I^2C-compatible interface.

Additionally, there is a flag register with flag and status bits. The user can read back this register and determine if a fault or warning message has been generated.

7.2 Functional Block Diagram



7.3 Features Description

7.3.1 Enabling the LM36272

The LM36272 has a logic level input HWEN which serves as the master enable/disable for the device. When HWEN is low the device is disabled, the registers are reset to their default state, the I^2C bus is inactive, and the device is placed in a low-power shutdown mode. When HWEN is forced high the device is enabled, and I^2C writes are allowed to the device.

Features Description (continued)

7.3.2 Backlight

The high voltage required by the LED strings is generated with an asynchronous backlight boost converter. An adaptive voltage control loop automatically adjusts the output voltage based on the voltage over the LED drivers LED1 and LED2. The LM36272 has three switching frequency modes, 1 MHz, 500 kHz, and 250 kHz. These are set via the BL_FREQ Select bit, register 0x03 bit[7] and by utilizing the auto-frequency feature (refer to *Auto Switching Frequency*). Operation in low-frequency mode results in better efficiency at lighter load currents due to the decreased switching losses. Operation in high-frequency mode gives better efficiency at higher load currents due to the reduced inductor current ripple and the resulting lower conduction losses in the MOSFET and inductor.

Features Description (continued)

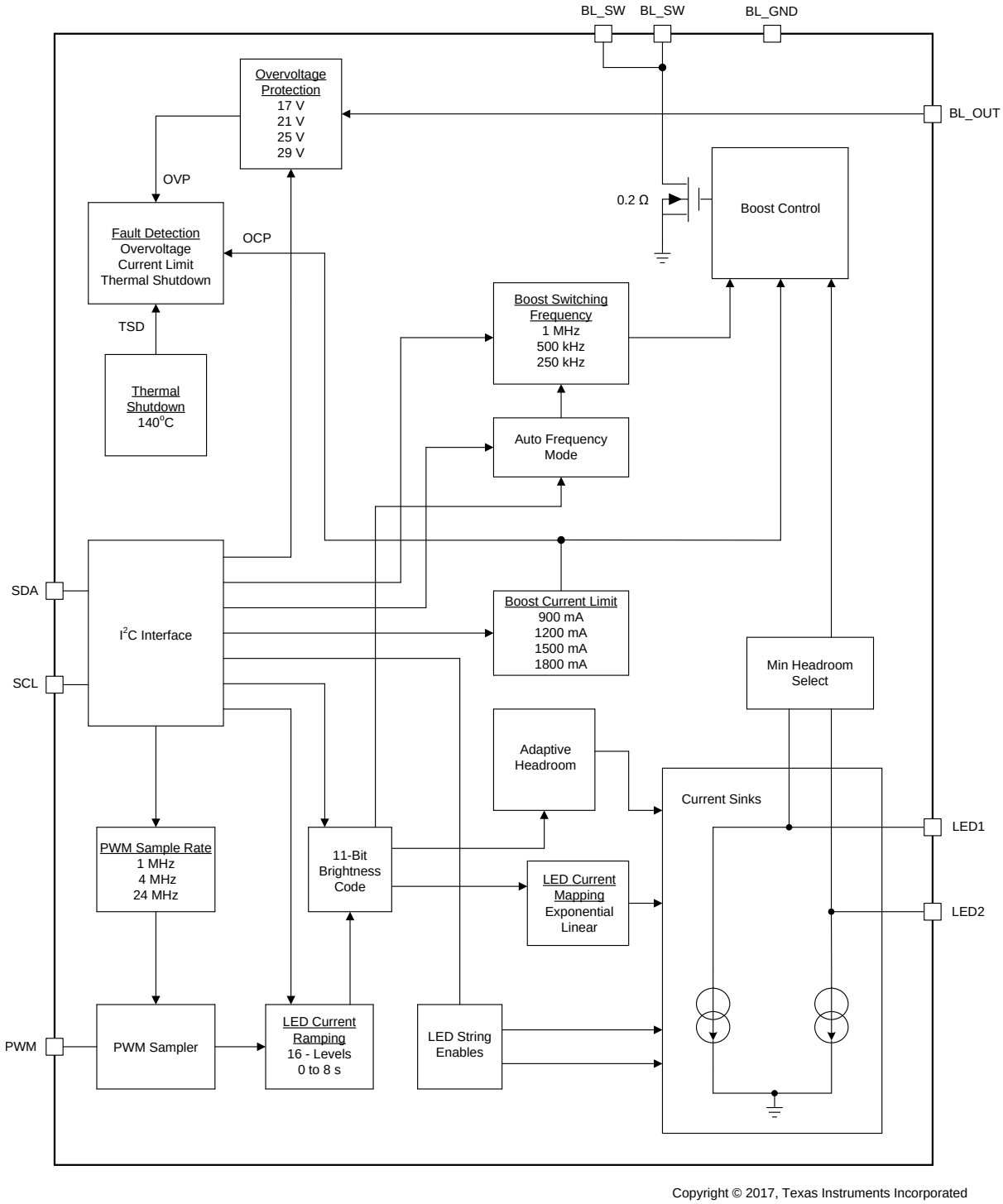


Figure 30. Backlight Block Diagram

7.3.2.1 Current Sink Enable

Each current sink in the device has a separate enable input. This allows for a one-string or two-string application. Once the correct LED string configuration is programmed and a non-zero code is written to the brightness registers, the device can be enabled by writing the backlight enable bit high (register 0x08 bit[4]).

Features Description (continued)

The default settings for the device are backlight enable bit set to 0, all backlight strings disabled, PWM input disabled, linear mapped mode, and the brightness level set to 30 mA per string.

When PWM is enabled, the LM36272 actively monitors the PWM input. After a non-zero PWM duty cycle is detected, the LM36272 multiplies the duty cycle with the programmed I^2C brightness code to give an 11-bit brightness value between 60 µA and 30 mA. Figure 31 and Figure 32 describe the start-up timing for operation with I^2C controlled current and with PWM controlled current.

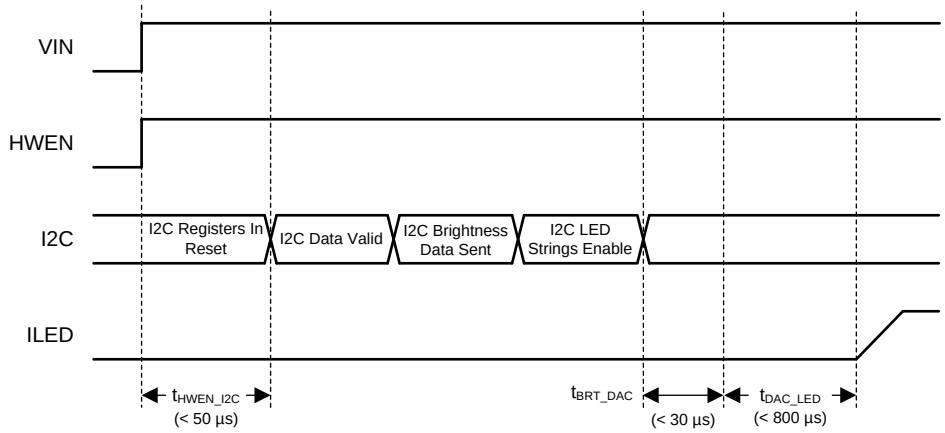


Figure 31. Enabling the LM36272 via I^2C

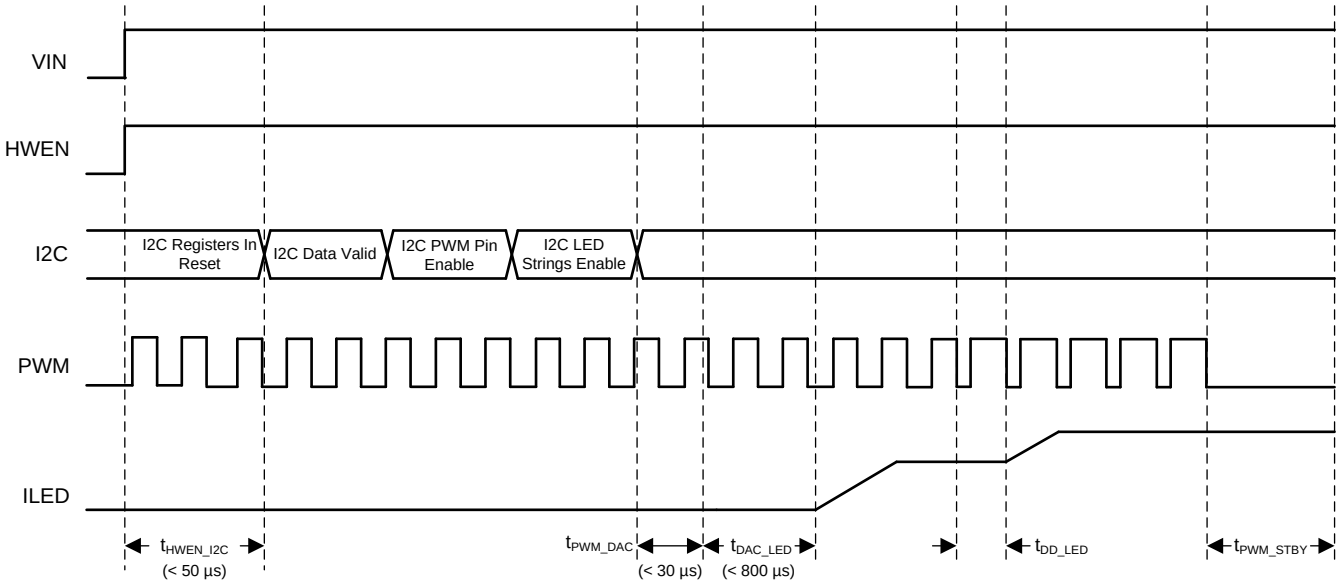


Figure 32. Enabling the LM36272 via PWM

The LM36272 backlight can be enabled or disabled in various ways. When disabled, the device is considered shut down, and the quiescent current drops to I_{SHDN}. When the device is in standby, it returns to the $I_{STANDBY}$ current level retaining all programmed register values. Table 1 describes the different backlight operating states for the LM36272.

Features Description (continued)

Table 1. Backlight Operating Modes

HWEN	BL_EN 0x08[4]	PWM INPUT	I²C BRIGHTNESS 0x05[7:0] 0x04[2:0]	CURRENT SINK ENABLES 0x08[1:0]	PWM EN 0x02[0]	PWM RAMP 0x02[1]	FEEDBACK DISABLES 0x10[4:3]	MAPPING MODE 0x02[3]	ACTION
0	X	X	X	X	X	X	X	X	Shutdown
1	0	X	X	X	X	X	X	X	Standby(1)
1	1	X	0x000	00	X	X	X	X	Standby(1)
1	1	X	≥0x001	≥01	0	X	<11	0 = Exponential Mode 1 = Linear Mode	-Backlight boost enabled -Selected current sink(s) enabled -I²C control only
1	1	Duty cycle = 0	X	≥01	1	X	<11	X	Standby(1)
1	1	Duty cycle > 0	≥0x001	≥01	1	0	<11	0 = Exponential Mode 1 = Linear Mode	-Backlight boost enabled -Selected current sink(s) enabled -I²C × PWM (after ramper) -No ramp between PWM duty-cycle change
1	1	Duty cycle > 0	≥0x001	≥01	1	1	<11	0 = Exponential Mode 1 = Linear Mode	-Backlight boost enabled -Selected current sink(s) enabled -I²C × PWM (before ramper)
1	1	Duty cycle > 0	≥0x001	≥01	1	0	11	0 = Exponential Mode 1 = Linear Mode	-Backlight boost disabled -Selected current sink(s) enabled -I²C × PWM (after ramper)
1	1	Duty cycle > 0	≥0x001	≥01	1	1	11	0 = Exponential Mode 1 = Linear Mode	-Backlight boost disabled -Selected current sink(s) enabled -I²C × PWM (before ramper)

(1) Standby implies the backlight boost and current sinks are shut down. Register writes are still possible. Shutdown implies that the device is in reset and no I²C communication is possible.

7.3.2.2 Brightness Mapping

There are two different ways to map the brightness code (or PWM duty cycle) to the LED current: linear and exponential mapping.

7.3.2.2.1 Linear Mapping

For linear mapped mode the LED current increases proportionally to the 11-bit brightness code and follows the relationship:

$$I_{LED} = 45.37\ \mu A + 14.63\ \mu A \times Code \quad (1)$$

This is valid from codes 1 to 2047. Code 0 programs 0 current. Code is an 11-bit code that can be the I²C brightness code or the product of the I²C brightness code and the PWM duty cycle.

7.3.2.2.2 Exponential Mapping

In exponential mapped mode the LED current follows the relationship:

$$I_{LED} = 60\ \mu A \times 1.003040572^{Code} \quad (2)$$

This results in an LED current step size of approximately 0.304% per code. This is valid for codes from 1 to 2047. Code 0 programs 0 current. Code is an 11-bit code that can be the I²C brightness code or the product of the I²C brightness code and the PWM duty cycle. Figure 33 details the LED current exponential response.

The 11-bit (0.304%) per code step is small enough such that the transition from one code to the next in terms of LED brightness is not distinguishable to the eye. This, therefore, gives a perfectly smooth brightness increase between adjacent codes.

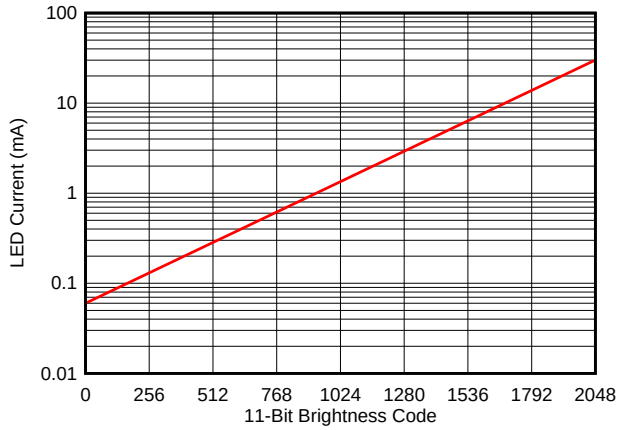


Figure 33. LED Current vs Brightness Code (Exponential Mapping)

7.3.2.3 Backlight Brightness Control Modes

The LM36272 has 2 brightness control modes:

1. I^2C only brightness control
2. I^2C × PWM brightness control

7.3.2.3.1 I^2C Brightness Control (PWM Pin Disabled)

If the PWM pin is disabled the I^2C brightness registers are in control of the LED current, and the PWM input is disabled. The brightness data (BRT) is the concatenation of the two brightness registers (3 LSBs) and (8 MSBs) (registers 0x04 and 0x05, respectively). The LED current only changes when the MSBs are written, meaning that to do a full 11-bit current change via I^2C, first the 3 LSBs are written and then the 8 MSBs are written. In this mode the ramper only controls the time from one I^2C brightness set-point to the next Figure 34.

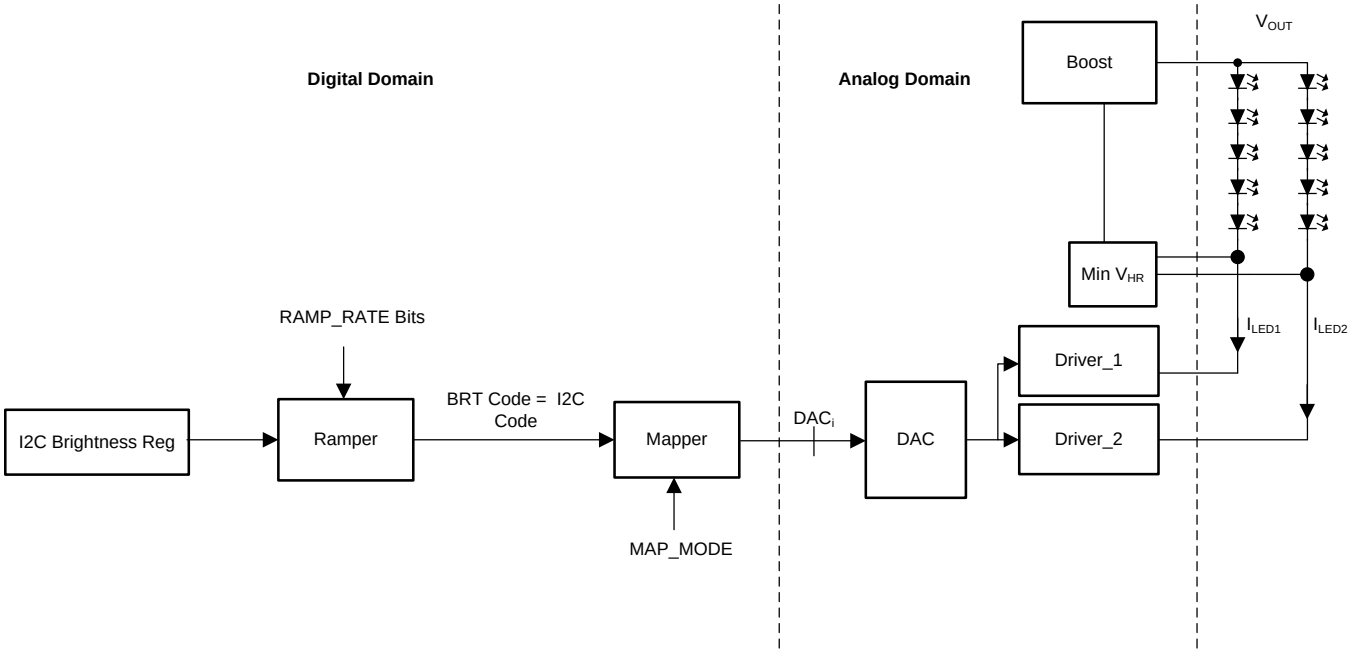


Figure 34. I^2C Only Brightness Control

7.3.2.3.2 I²C × PWM Brightness Control (PWM Pin Enabled)

If the PWM pin is enabled both the I²C brightness code and the PWM duty-cycle control the LED current.

With linear mapping the PWM duty cycle-to-current response is approximated by Equation 3:

$$I_{LED} = 45.37\ \mu A + 14.63\ \mu A \times I^2C\ BRGT\ CODE \times PWM\ D/C \quad (3)$$

With exponential mapping the PWM duty cycle-to-current response is approximated by Equation 4:

$$I_{LED} = 60\ \mu A \times 1.003040572^{I2C\ BRGT\ CODE \times PWM\ D/C} \quad (4)$$

7.3.2.3.2.1 PWM Ramper

The PWM ramp option (register 0x02 bit[1]) determines whether the ramper is active or inactive during a change in PWM duty cycle.

The ramper smooths the transition from one brightness value to another. Ramp time can be adjusted from 0 ms to 8000 ms with LED Current Ramp [3:0] bits (register 0x03 bits [6:3]). Ramp time is used for sloping both up and down. Ramp time always remains the same regardless of the amount of change in brightness.

In PWM mode the behavior of the ramper depends on the state of the PWM Ramp bit (register 0x02, bit [1]). If the PWM Ramp bit is set to 0, there is no LED current ramping between PWM duty cycle changes. The PWM duty cycle is multiplied with the I²C brightness code at the output of the ramper (see Figure 35). If this bit is set to 1, ramping is achieved between I²C × PWM currents (see Figure 36).

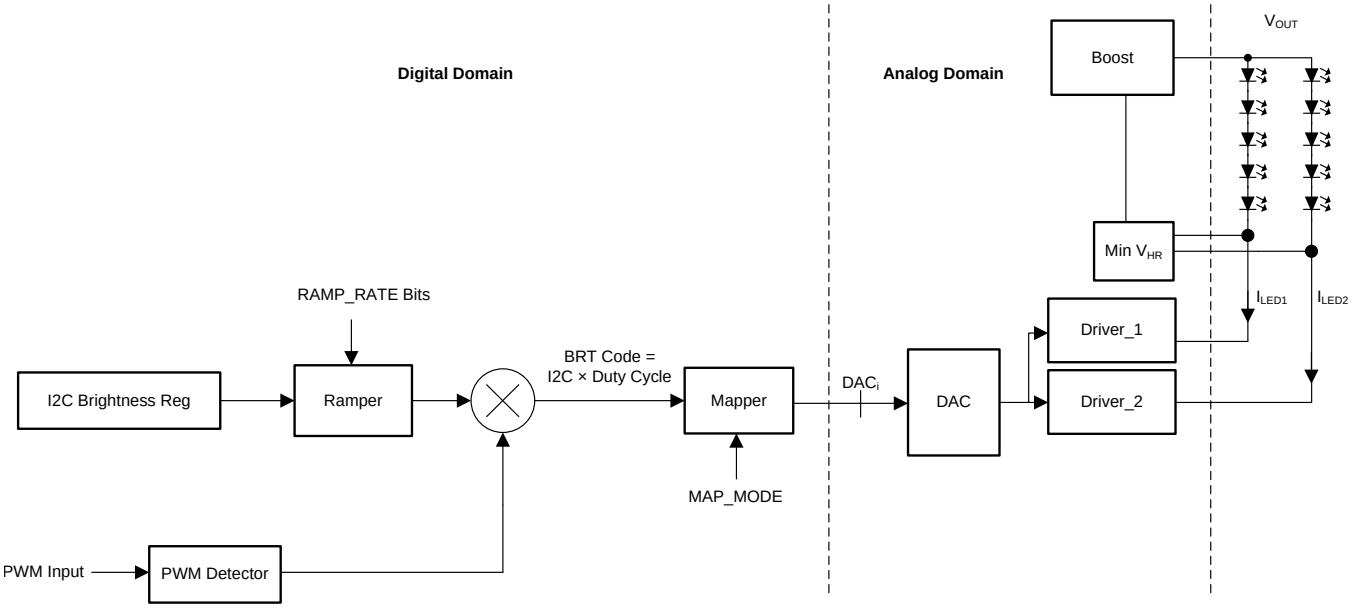


Figure 35. (I²C + PWM) Brightness Control, PWM Ramper Disabled

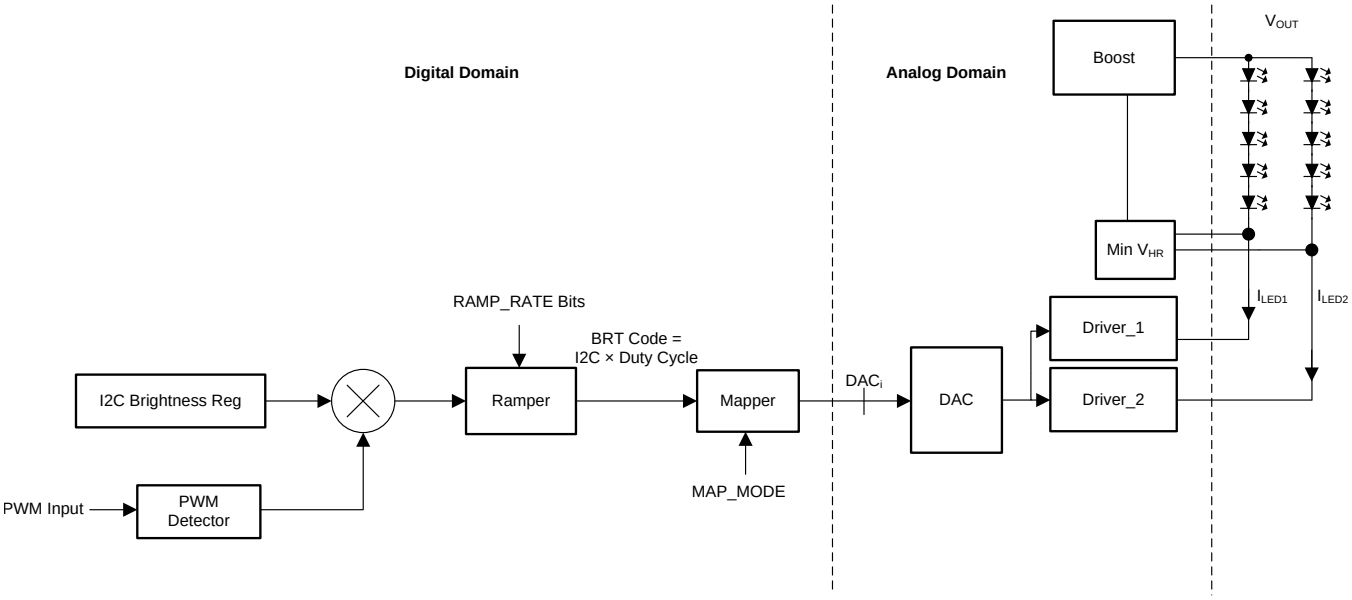


Figure 36. (I²C + PWM) Brightness Control, PWM Ramper Enabled

7.3.2.4 Boost Switching Frequency

The M36272 has two programmable switching frequencies: 500 kHz and 1 MHz. These are set via the Backlight Configuration 2 register (register 0x03 bit [7]). Operation at 1 MHz is primarily beneficial when efficiency at high load current is more important. For maximum efficiency across the entire load current range the device incorporates an automatic frequency shift mode (see *Auto Switching Frequency*).

7.3.2.4.1 Minimum Inductor Select

The LM36272 can use inductors in the range of 4.7 µH to 15 µH. In order to optimize the converter response to changes in V_{IN} and load, the Backlight Boost L Select bits (register 0x11 bits [7:6]) must be selected depending on the nominal value of inductance chosen.

7.3.2.5 Boost Feedback Gain Select

The Boost Integral and Proportional Feedback Gain Select bits in Option 2 register (bits [3:2] and bits[5:4] in register 0x11) contain adjustment parameters for the LM36272 internal loop gain. The optimized settings using a 1-uF capacitor at BL_OUT are the default settings of 01 and 11 for Integral and Proportional, respectively.

7.3.2.6 Auto Switching Frequency

To take advantage of frequency vs load dependent losses, the LM36272 can automatically change the boost switching frequency based on the programmed brightness code. In addition to the register programmable switching frequencies of 500 kHz and 1 MHz, the auto-frequency mode also incorporates a low-frequency selection of 250 kHz. It is important to note that the 250-kHz frequency is only accessible in auto-frequency mode and has a maximum boost duty cycle (D_{MAX}) of 50%.

Auto-frequency mode operates by using two programmable registers (Backlight Auto Frequency Low Threshold (register 0x06) and Backlight Auto Frequency High Threshold (register 0x07)). The high threshold determines the switchover from 1 MHz to 500 kHz. The low threshold determines the switchover from 500 kHz to 250 kHz. Both the High and Low Threshold registers take an 8-bit code which is compared against the 8 MSB of the brightness register (register 0x05). Table 2 details the boundaries for this mode.

Table 2. Auto Switching Frequency Operation

BRIGHTNESS CODE MSBs (Register 0x05 bits[7:0])	BOOST SWITCHING FREQUENCY
< Auto Frequency Low Threshold (register 06 Bits[7:0])	250 kHz (D_{MAX} = 50%)

Table 2. Auto Switching Frequency Operation (continued)

BRIGHTNESS CODE MSBs (Register 0x05 bits[7:0])	BOOST SWITCHING FREQUENCY
> Auto Frequency Low Threshold (Register 06 Bits[7:0]) and < Auto Frequency High Threshold (Register 07 Bits[7:0])	500 kHz
≥ Auto Frequency High Threshold (register 07 Bits[7:0])	1 MHz

Automatic-frequency mode is enabled whenever there is a non-zero code in either the Auto-Frequency High or Auto-Frequency Low registers. To disable the auto-frequency shift mode, set both registers to 0x00. When automatic-frequency select mode is disabled, the switching frequency operates at the programmed frequency (Register 0x03 bit[7]) across the entire LED current range. Table 3 provides a guideline for selecting the auto frequency threshold settings at V_{IN} = 3.7 V. The actual setting must be verified in the application and optimized for the desired input voltage range.

Table 3. Auto Frequency Threshold Settings Examples, V_{IN} = 3.7 V

CONDITION (V_f = 3.35 V at I_{LED} = 30 mA)	INDUCTOR (µH)	RECOMMENDED AUTO FREQUENCY HIGH THRESHOLD	RECOMMENDED AUTO FREQUENCY LOW THRESHOLD
2 × 4 LEDs	10	0x65 (12 mA)	0x43 (8 mA)
2 × 5 LEDs	10	0x5C (11 mA)	0x42 (7.9 mA)
2 × 6 LEDs	10	0x54 (10 mA)	0x3F (7.5 mA)
2 × 7 LEDs	10	0x4F (9.4 mA)	0x36 (6.5 mA)
2 × 8 LEDs	10	0x65 (12 mA)	0x3F (7.5 mA)

7.3.2.7 PWM Input

The PWM input is a sampled input which converts the input duty cycle information into an 11-bit brightness code. The use of a sampled input eliminates any noise and current ripple that traditional PWM controlled LED drivers are susceptible to. It also allows the PWM duty cycle to LED current response to have the same high accuracy and matching that is offered in the I^2C brightness control.

The PWM input uses logic level thresholds with V_{IH_MIN} = 1.25 V and V_{IL_MAX} = 0.4 V. Because this is a sampled input, there are limits on the maximum PWM input frequency as well as the resolution that can be achieved.

7.3.2.7.1 PWM Sample Frequency

There are three selectable sample rates for the PWM input. The choice of sample rate depends on three factors:

1. Required PWM resolution (input duty cycle to brightness code, with 11 bits maximum)
2. PWM input frequency
3. Efficiency

7.3.2.7.1.1 PWM Resolution and Input Frequency Range

The PWM input frequency range is 50 Hz to 50 kHz. To achieve the full 11-bit maximum resolution of PWM duty cycle to the LED brightness code (BRT), the input PWM duty cycle must be ≥ 11 bits, and the PWM sample period ($1/f_{SAMPLE}$) must be smaller than the minimum PWM input pulse width. Figure 37 shows the possible brightness code resolutions based on the input PWM frequency. The minimum PWM frequency for each PWM sample rate is described in *PWM Timeout*.

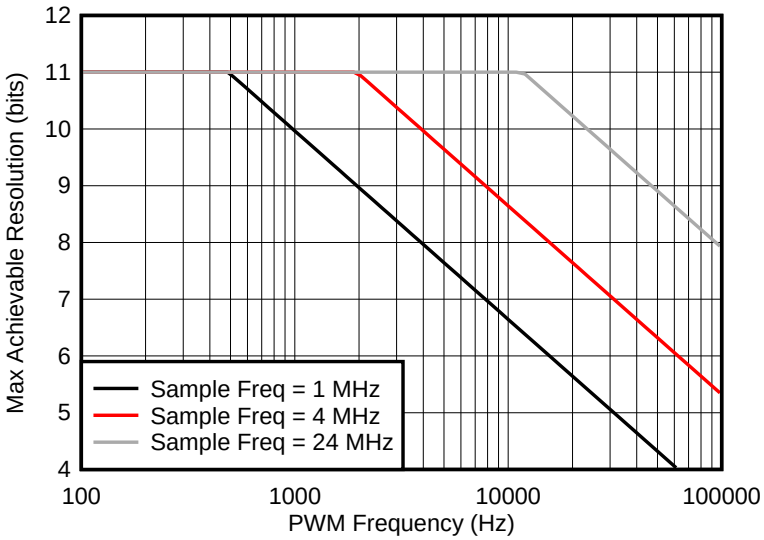


Figure 37. PWM Sample Rate, Resolution, and PWM Input Frequency

7.3.2.7.1.2 PWM Sample Rate and Efficiency

Efficiency is maximized when the lowest f_{SAMPLE} is chosen because this lowers the quiescent operating current of the device. Table 4 describes the typical efficiency tradeoffs for the different sample clock settings.

Table 4. PWM Sample Rate Trade-Offs

PWM SAMPLE RATE (f_{SAMPLE})		TYPICAL INPUT CURRENT, DEVICE ENABLED I_{LED} = 10 mA/string, 2 × 6 LEDs	TYPICAL EFFICIENCY
0x03 Bit[2]	0x12 Bit[0]	f_{SW} = 1 MHz	V_{IN} = 3.7 V
0	0	1.573 mA	87.7%
1	0	1.635 mA	87.65%
X	1	2.358 mA	87%

7.3.2.7.1.2.1 PWM Sample Rate Example

The number of bits of resolution on the PWM input varies according to the PWM sample rate and PWM input frequency (see Table 5).

Table 5. PWM Resolution vs PWM Sample Rate

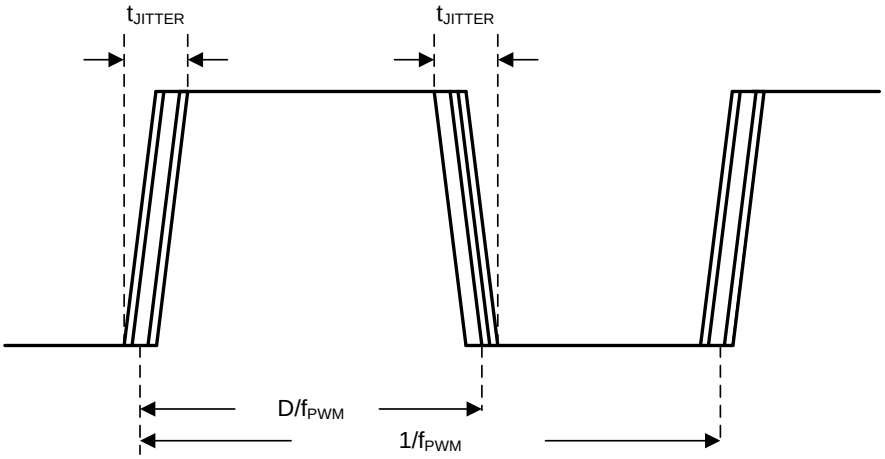
PWM FREQUENCY (kHz)	RESOLUTION (PWM SAMPLE RATE = 1 MHz)	RESOLUTION (PWM SAMPLE RATE = 4 MHz)	RESOLUTION (PWM SAMPLE RATE = 24 MHz)
0.4	11	11	11
2	9	11	11
12	6.4	8.4	11

7.3.2.7.2 PWM Hysteresis

To prevent jitter at the input PWM signal from feeding through the PWM path and causing oscillations in the LED current, the LM36272 offers 4 selectable hysteresis settings. The hysteresis options for the 1-MHz and 4-MHz PWM sample rate settings are 1, 2, 4, and 6 bits and for the 24-MHz PWM sample rate setting 0, 1, 2, and 3 bits. The hysteresis works by forcing a specific number of 11-bit LSB code transitions to occur in the input duty cycle before the LED current changes. Table 6 describes the hysteresis. The hysteresis only applies during the change in direction of brightness currents. Once a change in the direction of the LED current has taken place, the PWM input must over come the required LSB(s) of the hysteresis setting before the brightness change takes effect. Once the initial hysteresis has been overcome and the direction in brightness change remains the same, the PWM to current response changes with no hysteresis.

Table 6. PWM Input Hysteresis

HYSTERESIS SETTING (0x03 Bits[1:0])	MIN CHANGE IN PWM PULSE WIDTH (Δt) REQUIRED TO CHANGE LED CURRENT, AFTER DIRECTION CHANGE (for f_{PWM} < 11.7 kHz)	MIN CHANGE IN PWM DUTY CYCLE (ΔD) REQUIRED TO CHANGE LED CURRENT AFTER DIRECTION CHANGE	MIN (ΔI_{LED}), INCREASE FOR INITIAL CODE CHANGE	
			EXPONENTIAL MODE	LINEAR MODE
0 LSB (24 MHz sample rate only)	$1/(f_{PWM} \times 2047)$	0.05%	0.30%	0.05%
1 LSB	$1/(f_{PWM} \times 1023)$	0.10%	0.61%	0.10%
2 LSBs	$1/(f_{PWM} \times 511)$	0.20%	1.21%	0.20%
3 LSBs (24-MHz sample rate only)	$1/(f_{PWM} \times 255)$	0.39%	2.40%	0.39%
4 LSBs (1-MHz and 4-MHz sample rate only)	$1/(f_{PWM} \times 127)$	0.78%	4.74%	0.78%
6 LSBs (1-MHz and 4-MHz sample rate only)	$1/(f_{PWM} \times 31)$	3.12%	17.66%	3.12%



- D is t_{JITTER} x f_{PWM} or equal to #LSB's = ΔD x 2048 codes.
- For 11-bit resolution, #LSBs is equal to a hysteresis setting of LN(#LSB's)/LN(2).
- For example, with a t_{JITTER} of 1 µs and a f_{PWM} of 5 kHz, the hysteresis setting should be: LN(1 µ s x 5 kHz x 2048)/LN(2) = 3.35 (4 LSBs).

Figure 38. PWM Hysteresis Example

7.3.2.7.3 PWM Step Response

The LED current response due to a step change in the PWM input is approximately 2 ms to go from minimum LED current to maximum LED current.

7.3.2.7.4 PWM Timeout

The LM36272 PWM timeout feature turns off the boost output when the PWM is enabled and there is no PWM pulse detected. The timeout duration changes based on the PWM sample rate selected which results in a minimum supported PWM input frequency. The sample rate, timeout, and minimum supported PWM frequency are summarized in Table 7.

Table 7. PWM Timeout and Minimum Supported PWM Frequency vs PWM Sample Rate

SAMPLE RATE	TIMEOUT	MINIMUM SUPPORTED PWM FREQUENCY
1 MHz	25 msec	48 Hz
4 MHz	3 msec	400 Hz
24 MHz	0.6 msec	2000 Hz

7.3.2.7.5 PWM-to-Digital Code Readback

In PWM mode, registers 0x12 and 0x13 contain the PWM duty cycle to the 11-bit code conversion information. Register 0x12 contains the 8 LSBs of the brightness code and register 0x13 the 3 MSBs. To translate this reading to the actual LED current setting of the LM36272, convert it to the corresponding duty cycle and multiply it by the brightness level setting in the brightness registers (0x04 and 0x05). For example, if the 11-bit brightness code is set to 0x554 (decimal 1364) and the PWM-to-digital code readback is 0x3FF (decimal 1023) in linear mode, the expected LED current is approximately: I_{LED} = 45.37 µA + ((1023 / 2047) × 14.63 × 1364) µA = 10.018 mA (approximately 50% duty cycle).

7.3.2.8 Regulated Headroom Voltage

In order to optimize efficiency, current accuracy, and string-to-string matching the LED current sink regulated headroom voltage (V_{HR}) varies with the target LED current. Figure 39 details the typical variation of V_{HR} with LED current. This allows for increased solution efficiency as the dropout voltage of the LED driver changes. Furthermore, in order to ensure that all current sinks remain in regulation whenever there is a mismatch in string voltages, the minimum headroom voltage between VLED1, VLED2 becomes the regulation point for the boost converter. For example, if the LEDs connected to LED1 require 12 V and the LEDs connected to LED2 require 12.5 V at the programmed current, then the voltage at LED1 is VHR + 0.5 V and the voltage at LED2 is V_{HR}. In other words, the boost makes the cathode of the highest voltage LED string the regulation point.

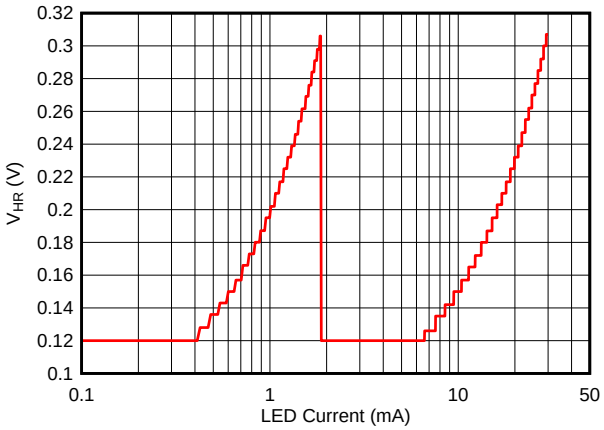


Figure 39. LM36272 Typical Exponential Regulated Headroom Voltage vs Programmed LED Current

7.3.2.9 Backlight Fault Protection and Faults

7.3.2.9.1 Backlight Overvoltage Protection (OVP)

The LM36272 provides an OVP that monitors the LED boost output voltage (V_{BL_OUT}) and protects BL_OUT and BL_SW from exceeding safe operating voltages. The OVP threshold can be set to 17 V, 21 V, 25 V, or 29 V with register 0x02 bits[7:5]. Once an OVP event has been detected, the BL_OVP flag is set in the Flags Register, and the subsequent behavior depends on the state of bit OVP_Mode in the Backlight Configuration 1 Register: If OVP_Mode is set to 0, as soon as V_{BL_OUT} falls below the backlight OVP threshold, the LM36272 begins switching again. If OVP_Mode is set to 1 and the device detects three occurrences of $V_{BL\_OUT} > V_{OVP\_BL}$ while any of the enabled current sink headroom voltages drops below 40 mV, the Backlight Boost OVP flag is set, the Backlight Enable bit is cleared, and the LM36272 enters standby mode. When the device is shut down due to a Backlight Boost OVP fault, the Flags register must be read back before the device can be reenabled.

7.3.2.9.2 Backlight Overcurrent Protection (OCP)

The LM36272 has 4 selectable OCP thresholds (900 mA, 1200 mA, 1500 mA, and 1800 mA). These are programmable in register 0x11 bits[1:0]. The OCP threshold is a cycle-by-cycle current limit and is detected in the internal low-side NFET. Once the threshold is hit the NFET turns off for the remainder of the switching period.

If enough overcurrent threshold events occur, the BL_OCP Flag (register 0x0F, bit[0]) is set. To avoid transient conditions from inadvertently setting the BL_OCP Flag, a pulse density counter monitors OCP threshold events over a 128-µs period. If 8 consecutive 128-µs periods occur where the pulse density count has found 2 or more OCP events, then the BL_OCP Flag is set.

During device start-up and during brightness code changes, there is a 4-ms blank time where BL OCP events are ignored. As a result, if the device starts up in an overcurrent condition there is an approximate 5-ms delay before the BL_OCP Flag is set.

7.3.3 LCM Bias

7.3.3.1 Display Bias Boost Converter (V_{VPOS}, V_{VNEG})

A single high-efficiency boost converter provides a positive voltage rail, V_{LCM_OUT}, which serves as the power rail for the LCM VPOS and VNEG outputs.

- The V_{VPOS} output LDO has a programmable range from 4 V up to 6.5 V with 50-mV steps and can supply up to 80 mA.
- The V_{VNEG} output is generated from a regulated, inverting charge pump and has an adjustable range of –6.5 V up to –4 V with 50-mV steps and a maximum load of 80 mA.

Boost voltage also has a programmable range from 4 V up to 7.15 V with 50-mV steps. Refer to Table 22, Table 23 and Table 24 for V_{LCM_OUT}, V_{VPOS} and V_{VNEG} voltage settings. When selecting a suitable boost-output voltage, the following estimation can be used: $V_{LCM\_OUT} = \max(V_{VPOS}, |V_{VNEG}|) + V_{HR}$, where $V_{HR} \geq 200$ mV for lower currents and $V_{HR} \geq 300$ mV for higher currents. When the device input voltage (V_{IN}) is greater than the programmed LCM boost output voltage, the boost voltage is regulated to V_{IN} + 100 mV. V_{VPOS} and V_{VNEG} voltage settings cannot be changed while they are enabled. V_{VPOS} and V_{VNEG} register setting targets take effect only after the outputs are disabled and re-enabled. However, the V_{LCM_OUT} target changes immediately upon a register write.

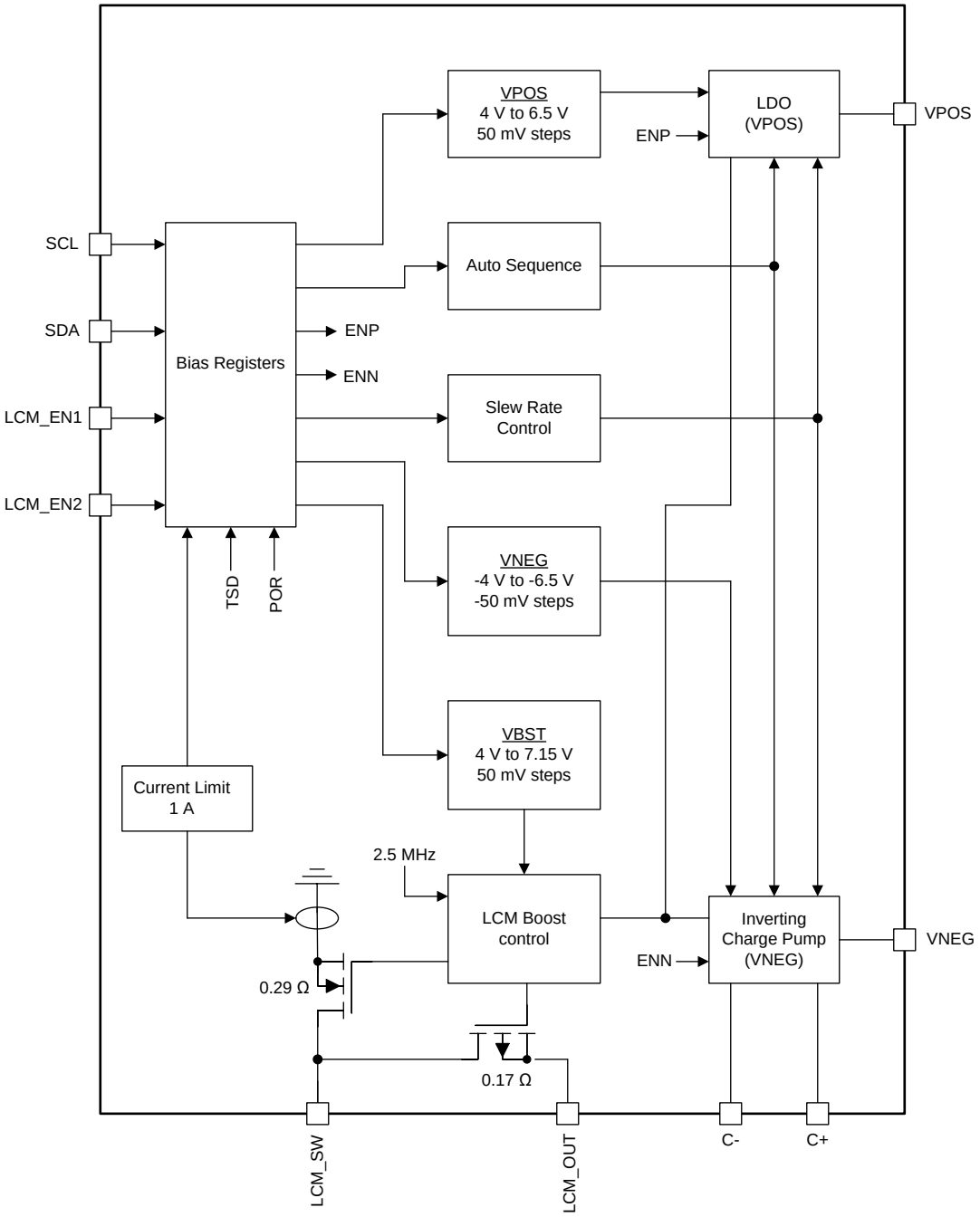


Figure 40. LCM Boost Block Diagram

The LCM Bias outputs can be controlled either by pins LCM_EN1 and LCM_EN2 or register bits VPOS_EN and VNEG_EN, register 0x09 bits[2:1]. Setting bit EXT_EN, register 0x09 bit[0], to 1 allows pins LCM_EN1 and LCM_EN2 to control VPOS and VNEG, respectively, while setting this bit to 0 yields control to bits VPOS_EN and VNEG_EN. Refer to Table 8 for LCM bias control information.

Table 8. LCM Operating Modes

HWEN	LCM_EN2 INPUT	LCM_EN1 INPUT	LCM_EN MODE 0x09[7:5]	VPOS_EN 0x09[2]	VNEG_EN 0x09[1]	EXT_EN 0x09[0]	ACTION
0	X	X	XXX	X	X	X	Device shutdown
1	0	0	000	X	X	1	Standby(1)
1	X	X	100	0	0	0	Standby(1)
1	0	1	100	X	X	1	VPOS enabled via external input
1	1	0	100	X	X	1	VNEG enabled via external input
1	1	1	100	X	X	1	VPOS and VNEG enabled via external input
1	X	X	100	1	0	0	VPOS enabled via I^2C
1	X	X	100	0	1	0	VNEG enabled via I^2C
1	X	X	100	1	1	0	VPOS and VNEG enabled via I^2C
1	X	X	101	1	1	0	VPOS and VNEG enabled via I^2C with auto-sequencing
1	1	X	101	X	X	1	VPOS and VNEG enabled via LCM_EN2 with auto-sequencing
1	1	X	110	1	0	X	WAKE1 $V_{VPOS} = V_{IN}$ $V_{VNEG} = GND$
1	1	X	110	0	1	X	WAKE1 $V_{VPOS} = GND$ $V_{VNEG} = -V_{IN}$
1	1	X	110	1	1	X	WAKE1 $V_{VPOS} = V_{IN}$ $V_{VNEG} = -V_{IN}$
1	0	X	110	1	1	X	WAKE1 Standby(1)
1	1	X	110	0	0	X	WAKE1 Standby(1)
1	1	X	111	1	0	X	WAKE2 V_{VPOS} = programmed target V_{VNEG} = disabled
1	1	X	111	0	1	X	WAKE2 V_{VPOS} = disabled V_{VNEG} = programmed target
1	1	X	111	1	1	X	WAKE2 V_{VPOS} = programmed target V_{VNEG} = programmed target
1	1	X	111	0	0	X	WAKE2 Standby(1)
1	0	X	111	1	1	X	WAKE2 Standby(1)

(1) Standby implies that VPOS and VNEG are either high impedance or being internally pulled low via the active pulldown, and that the LCM boost is off. Shutdown implies that the device is in reset and no I^2C communication is possible.

7.3.3.2 Auto Sequence Mode

If this mode is selected the LM36272 controls the turnon and turnoff of VPOS and VNEG as shown in Figure 41.

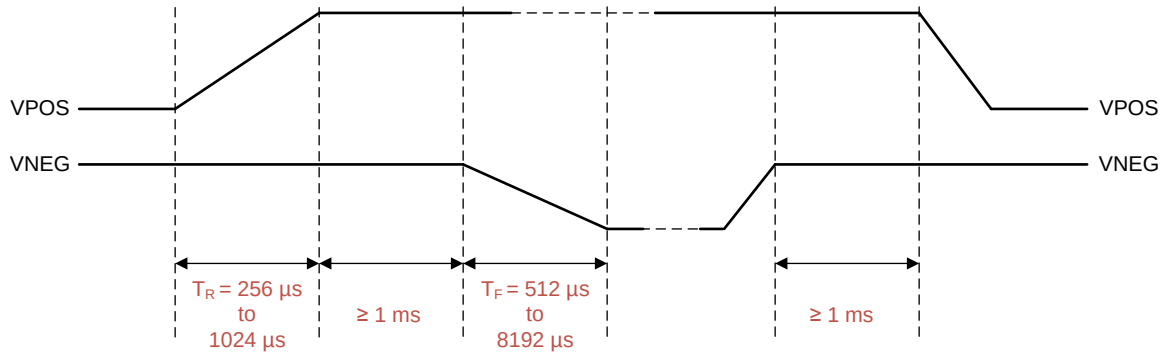


Figure 41. Auto Sequence Timing

7.3.3.3 Wake-up Mode

If wake-up mode is selected the LM36272 allows on/off control of both VPOS and VNEG with only one external pin (LCM_EN2). Any combination of VPOS or VNEG can be turned on based on the state of bits VPOS_EN and VNEG_EN in register 0x09. In these modes the internal shutdown timing of the VPOS and VNEG blocks is modified to allow for lower quiescent current in standby mode, therefore reducing the average current consumption during a sequence of on/off events.

There are two wake-up modes available on the LM36272: wake1 and wake2.

7.3.3.3.1 Wake1 Mode

In wake1 mode the LM36272 passes V_{IN} through to the LCM boost output and the enabled VPOS, VNEG outputs. Due to the impedance of the LCM boost, the VPOS LDO and the VNEG charge pump, the respective outputs are regulated close to V_{IN} only at very light load current and droop below V_{IN} as the load increases.

7.3.3.3.2 Wake2 Mode

In wake2 mode the LM36272 regulates the LCM boost output as well as the enabled VPOS and VNEG outputs to their programmed voltage.

7.3.3.4 Active Discharge

An optional active discharge is available for the VPOS and VNEG output rails. An internal switch resistance for this discharge function is implemented on each output rail. The VPOS active discharge function is enabled with register 0x09 bit[4] and the VNEG active discharge with register 0x09 bit[3].

7.3.3.5 LCM Bias Protection and Faults

The LCM bias block of the LM36272 provides three protection mechanisms in order to prevent damage to the device. Note that none of these have any effect on backlight operation.

7.3.3.5.1 LCM Overvoltage (OVP) Protection

The LM36272 provides OVP that monitors the LCM bias boost output voltage (V_{LCM_OUT}) and protects LCM_OUT and LCM_SW from exceeding safe operating voltages. The OVP threshold is set to 7.8 V (typical). If an LCM bias overvoltage condition is detected, the LCM_OVP flag, register 0x0F bit[5], is set. Once the OVP condition is removed, the flag can be cleared with an I^2C read back of the register. An LCM OVP condition does not cause the LCM bias to shut down; it is a report-only flag.

7.3.3.5.2 VPOS Short-Circuit Protection

If the current at VPOS exceeds 180 mA (typical), the LM36272 sets the VPOS_SHORT flag, register 0x0F bit[3]. A readback of register 0x0F is required to clear the flag. The outcome of a VPOS_SHORT detection depends on the configuration of the bias short-circuit mode option, register 0x0A bits[7:6]. The options are report-only flag, shutdown VPOS/VNEG, and shutdown VPOS/VNEG and backlight. To prevent narrow spikes from falsely triggering a VPOS short-circuit condition, the LM36272 provides four programmable VPOS short-circuit filter options: 100 µs, 500 µs, 1 ms, and 2 ms. These are selected in register 0x0B bits[3:2].

7.3.3.5.3 VNEG Short-Circuit Protection

If the voltage at VNEG rises (towards GND) to above 84% of its programmed value (typical), the LM36272 sets the VNEG_SHORT flag, register 0x0F bit[2]. A readback of register 0x0F is required to clear the flag. The outcome of a VNEG_SHORT detection depends on the configuration of the bias short-circuit mode option, register 0x0A bits[7:6]. The options are report-only flag, shut down VPOS/VNEG, and shut down VPOS/VNEG and backlight. To prevent narrow spikes from falsely triggering a VNEG short circuit condition, the LM36272 provides four programmable VNEG short circuit filter options: 100 µs, 500 µs, 1 ms, and 2 ms. These are selected in register 0x0B bits[1:0].

7.3.4 Software Reset

Bit[7] (SWR_RESET) of the Enable Register (0x08) is a software reset bit. Writing a 1 to this bit resets all I^2C register values to their default values. Once the LM36272 has finished resetting all registers, it auto-clears the SWR_RESET bit.

7.3.5 HWEN Input

The HWEN pin is a global hardware enable for the LM36272. This pin must be pulled to logic HIGH to enable the device and the I^2C-compatible interface. There is a 300-kΩ internal resistor between HWEN and GND. When this pin is at logic LOW, the LM36272 is placed in shutdown, the I^2C-compatible interface is disabled, and the internal registers are reset to their default state. TI recommends that V_{IN} has risen above 2.7 V before setting HWEN HIGH.

7.3.6 Thermal Shutdown (TSD)

The LM36272 has TSD protection which shuts down the backlight boost, all backlight current sinks, LCM bias boost, inverting charge pump, and the LDO when the die temperature reaches or exceeds 140°C (typical). The I^2C interface remains active during a TSD event. If a TSD fault occurs the TSD fault is set (register 0x0F bit[6]). The fault is cleared by an I^2C read of register 0x0F or by toggling the HWEN pin.

7.4 Device Functional Modes

7.4.1 Modes of Operation

Shutdown: The LM36272 is in shutdown when the HWEN pin is low.

Standby: After the HWEN pin is set high the LM36272 goes into standby mode. In standby mode, I^2C writes are allowed but references, bias currents, the oscillator, LCM powers, and backlight are all disabled to keep the quiescent supply current low (2 µA typical).

Normal mode: Both main blocks of the LM36272 are independently controlled. For enabling each of the blocks in all available modes, see Table 1 and Table 8.

7.5 Programming

7.5.1 I²C-Compatible Serial Bus Interface

7.5.1.1 Interface Bus Overview

The I²C-compatible synchronous serial interface provides access to the programmable functions and registers on the device. This protocol uses a two-wire interface for bidirectional communications between the devices connected to the bus. The two interface lines are the Serial Data Line (SDA) and the Serial Clock Line (SCL). These lines must be connected to a positive supply via a pullup resistor and remain HIGH even when the bus is idle.

Every device on the bus is assigned a unique address and acts as either a Master or a Slave, depending whether it generates or receives the serial clock (SCL).

7.5.1.2 Data Transactions

One data bit is transferred during each clock pulse. Data is sampled during the high state of the SCL. Consequently, throughout the clock's high period, the data remains stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data is sent during the low SCL state. This protocol permits a single data line to transfer both command/control information and data using the synchronous serial clock.

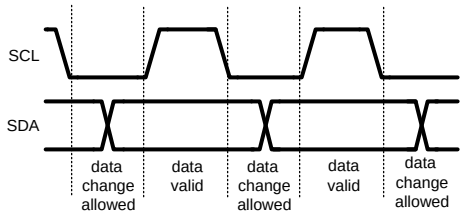


Figure 42. Data Validity

Each data transaction is composed of a start condition, a number of byte transfers (set by the software), and a stop condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an acknowledge signal must follow. The following sections provide further details of this process.

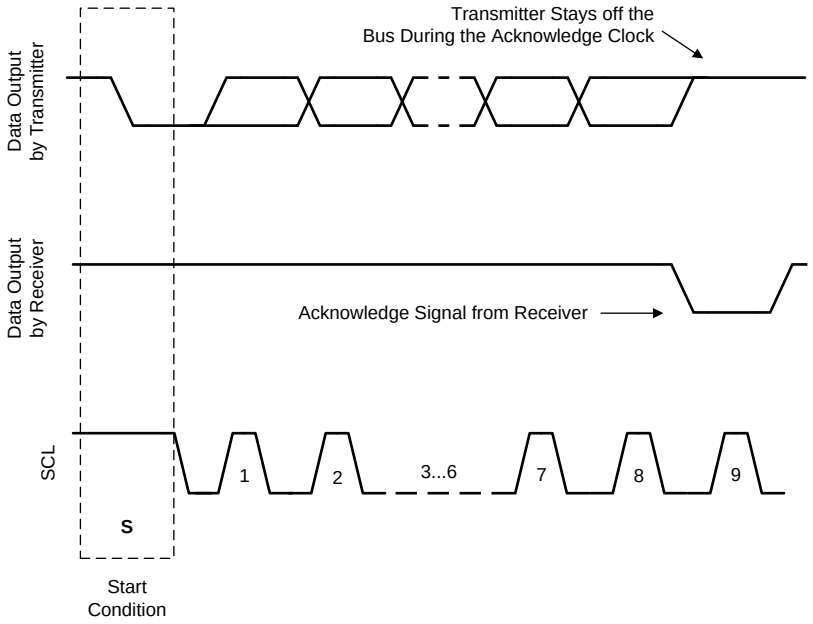


Figure 43. Acknowledge Signal

Programming (continued)

The Master device on the bus always generates the start and stop conditions (control codes). After a Start Condition is generated, the bus is considered busy, and it retains this status until a certain time after a stop condition is generated. A high-to-low transition of the data line (SDA) while the clock (SCL) is high indicates a start condition. A low-to-high transition of the SDA line while the SCL is high indicates a stop condition.

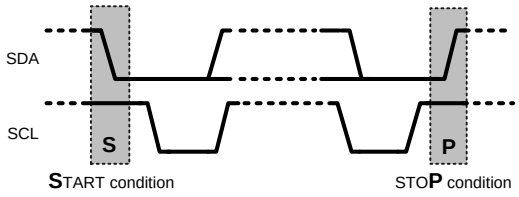


Figure 44. Start and Stop Conditions

In addition to the first start condition, a repeated start condition can be generated in the middle of a transaction. This allows another device to be accessed, or a register read cycle.

7.5.1.3 Acknowledge Cycle

The acknowledge cycle consists of two signals: the acknowledge clock pulse the master sends with each byte transferred, and the acknowledge signal sent by the receiving device.

The master generates the acknowledge clock pulse on the ninth clock pulse of the byte transfer. The transmitter releases the SDA line (permits it to go high) to allow the receiver to send the acknowledge signal. The receiver must pull down the SDA line during the acknowledge clock pulse and ensure that SDA remains low during the high period of the clock pulse, thus signaling the correct reception of the last data byte and its readiness to receive the next byte.

7.5.1.4 Acknowledge After Every Byte Rule

The master generates an acknowledge clock pulse after each byte transfer. The receiver sends an acknowledge signal after every byte received.

There is one exception to the *acknowledge after every byte* rule. When the master is the receiver, it must indicate to the transmitter an end of data by not-acknowledging (*negative acknowledge*) the last byte clocked out of the slave. This *negative acknowledge* still includes the acknowledge clock pulse (generated by the master), but the SDA line is not pulled down.

7.5.1.5 Addressing Transfer Formats

Each device on the bus has a unique slave address. The LM36272 operates as a slave device with the 7-bit address. If an 8-bit address is used for programming, the 8th bit is 1 for read and 0 for write. The 7-bit address for the device is 0x11.

Before any data is transmitted, the master transmits the address of the slave being addressed. The slave device sends an acknowledge signal on the SDA line, once it recognizes its address. The slave address is the first seven bits after a Start Condition. The direction of the data transfer (R/W) depends on the bit sent after the slave address — the eighth bit.

When the slave address is sent, each device in the system compares this slave address with its own. If there is a match, the device considers itself addressed and sends an acknowledge signal. Depending upon the state of the R/W bit (1: read, 0: write), the device acts as a transmitter or a receiver.

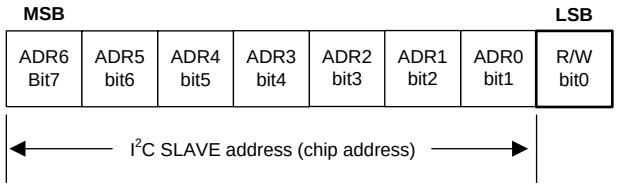


Figure 45. I²C Device Address

Programming (continued)

Control Register Write Cycle

- Master device generates start condition.
- Master device sends slave address (7 bits) and the data direction bit (r/w = 0).
- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8 bits).
- Slave sends acknowledge signal.
- Master sends data byte to be written to the addressed register.
- Slave sends acknowledge signal.
- If master sends further data bytes the control register address is incremented by one after acknowledge signal.
- Write cycle ends when the master creates stop condition.

Control Register Read Cycle

- Master device generates a start condition.
- Master device sends slave address (7 bits) and the data direction bit (r/w = 0).
- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8 bits).
- Slave sends acknowledge signal
- Master device generates repeated start condition.
- Master sends the slave address (7 bits) and the data direction bit (r/w = 1).
- Slave sends acknowledge signal if the slave address is correct.
- Slave sends data byte from addressed register.
- If the master device sends acknowledge signal, the control register address is incremented by one. Slave device sends data byte from addressed register.
- Read cycle ends when the master does not generate acknowledge signal after data byte and generates stop condition.

Table 9. I^2C Data Read/Write(1)

	ADDRESS MODE
Data Read	<Start Condition> <Slave Address><r/w =0>[Ack] <Register Addr>[Ack] <Repeated Start Condition> <Slave Address><r/w = 1>[Ack] [Register Data]<Ack or NAck> ...additional reads from subsequent register address possible <Stop Condition>
Data Write	<Start Condition> <Slave Address><r/w = 0>[Ack] <Register Addr>[Ack] <Register Data>[Ack] ...additional writes to subsequent register address possible <Stop Condition>

(1) < > = Data from master, [ ] = Data from slave

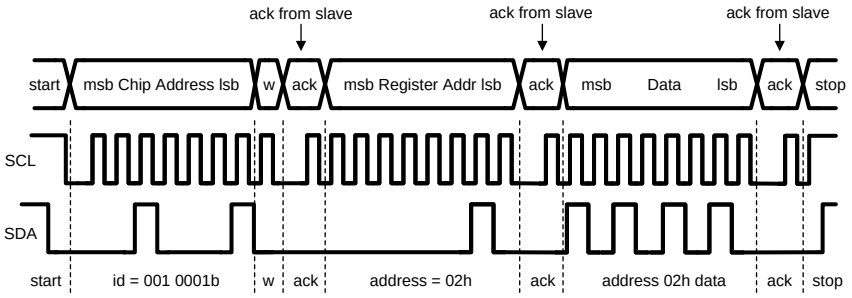


Figure 46. Register Write Format

When a READ function is to be accomplished, a WRITE function must precede the READ function, as show in the Read Cycle waveform.

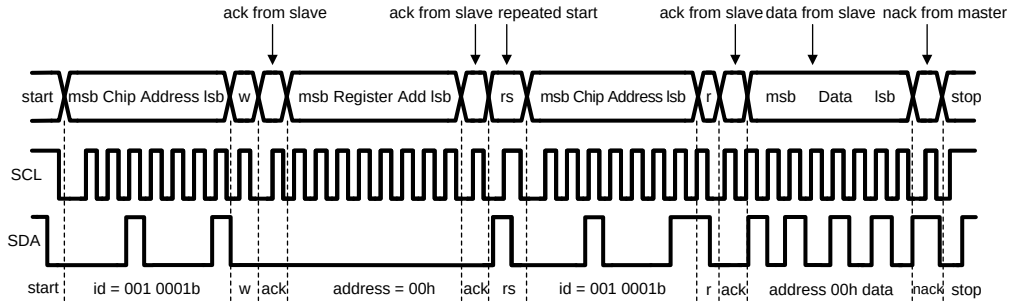


Figure 47. Register Read Format

NOTE

w = write (SDA = 0), r = read (SDA = 1), ack = acknowledge (SDA pulled down by either master or slave), rs = repeated start id = 7-bit chip address

7.5.1.6 Register Programming

For glitch-free operation, the following bits and/or registers must only be programmed while the LED Enable bits are 0 (Register 0x08, Bit [1:0] = 0) and/or Backlight Enable bit is 0 (Register 0x08, Bit[4] = 0):

1. Register 0x02 Bit[0] (PWM Enable)
2. Register 0x02 Bits[1] (PWM Ramp)
3. Register 0x02 Bit[2] (PWM Config)
4. Register 0x02 Bits[3] (LED Current Mapping)
5. Register 0x03 Bit[1:0] (PWM Hysteresis)
6. Register 0x03 Bit[2] (PWM Sample)
7. Register 0x03 Bit[6:3] (LED Current Ramp)
8. Register 0x10 Bit[0] (PWM HF Sample)
9. Register 0x10 Bit[1] (PWM Glitch Filter)
10. Register 0x10 Bit [4:3] (LED Feedback Enable)
11. Register 0x06 (auto frequency high threshold)
12. Register 0x07 (auto frequency low threshold)

7.6 Register Maps

Table 10. Register Default Values

I²C ADDRESS	REGISTER NAME	READ/WRITE	POWER ON/RESET VALUE	SECTION
0x01	Revision Register	R	0x01	Go
0x02	Backlight Configuration1 Register	R/W	0x28	Go
0x03	Backlight Configuration 2 Register	R/W	0x8D	Go
0x04	Backlight Brightness LSB Register	R/W	0x07	Go
0x05	Backlight Brightness MSB Register	R/W	0xFF	Go
0x06	Backlight Auto-Frequency Low Register	R/W	0x00	Go
0x07	Backlight Auto-Frequency High Register	R/W	0x00	Go
0x08	Backlight Enable Register	R/W	0x00	Go
0x09	Display Bias Configuration 1 Register	R/W	0x18	Go
0x0A	Display Bias Configuration 2 Register	R/W	0x11	Go
0x0B	Display Bias Configuration 3 Register	R/W	0x00	Go
0x0C	LCM Boost Bias Register	R/W	0x28	Go
0x0D	VPOS Bias Register	R/W	0x1E	Go
0x0E	VNEG Bias Register	R/W	0x1C	Go
0x0F	Flags Register	R	0x00	Go
0x10	Backlight Option 1 Register	R/W	0x06	Go
0x11	Backlight Option 2 Register	R/W	0x35	Go
0x12	PWM-to-Digital Code Readback LSB Register	R	0x00	Go
0x13	PWM-to-Digital Code Readback MSB Register	R	0x00	Go

7.6.1 Revision Register (Address = 0x01)[Reset = 0x01]

Figure 48. Revision Register

7	6	5	4	3	2	1	0
DEV_REV[6]	DEV_REV[5]	DEV_REV[4]	DEV_REV[3]	DEV_REV[1]	DEV_REV[0]	DEV_REV[1]	DEV_REV[0]
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 11. Revision Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	DEVICE REVISION	R	000000 or 000001	DEV_REVISION, A0 = 000000 A1 = 000001
1-0	VENDOR	R	01	VENDOR, Texas Instruments = 01

7.6.2 Backlight Configuration1 Register (Address = 0x02)[Reset = 0x28]

Figure 49. Backlight Configuration 1 Register

7	6	5	4	3	2	1	0
BL_OVP[2]	BL_OVP[1]	BL_OVP[0]	OVP_MODE	BLED_MAP	PWM_CONFIG	PWM_RAMP	PWM_ENABLE
R/W-0	R/W-0	R/W-1	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 12. Backlight Configuration 1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	BL_OVP	R/W	001	Backlight OVP 000: 17 V 001: 21 V 010: 25 V 011: 29 V 100 to 111 = 29 V
4	OVP_MODE	R/W	0	0: OVP is report only 1: OVP causes shutdown
3	BLED_MAP	R/W	1	0: Exponential 1: Linear
2	PWM_CONFIG	R/W	0	0: Active high 1: Active low
1	PWM_RAMP	R/W	0	0: No PWM ramp 1: LED current ramps with changes in duty cycle
0	PWM_ENABLE	R/W	0	0: PWM disabled 1: PWM enabled

7.6.3 Backlight Configuration 2 Register (Address = 0x03)[Reset = 0x8D]

Figure 50. Backlight Configuration 2 Register

7	6	5	4	3	2	1	0
BL BOOST FREQUENCY	LED CURRENT RAMP[3]	LED CURRENT RAMP[2]	LED CURRENT RAMP[1]	LED CURRENT RAMP[0]	PWM SAMPLE(1)	PWM HYST[1]	PWM HYST[0]
R/W-1	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

(1) (Note: register 0x10 bit[0] = 1 enables 24-MHz sample mode.)

Table 13. Backlight Configuration 2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BL BOOST FREQUENCY		1	Sets the backlight boost switch frequency 0: 500 kHz 1: 1 MHz (Default)
6-3	LED CURRENT RAMP	R/W	0001	Controls backlight LED ramping time. The transient time is a constant time that the backlight takes to transition from an existing programmed code to a new programmed code. 0000: 0 µs 0001: 500 µs 0010: 750 µs 0011: 1 ms 0100: 2 ms 0101: 5 ms 0110: 10 ms 0111: 20 ms 1000: 50 ms 1001: 100 ms 1010: 250 ms 1011: 800 ms 1100: 1 s 1101: 2 s 1110: 4 s 1111: 8 s
2	PWM SAMPLE	R/W	1	Sets PWM sampling frequency 0: 1 MHz 1: 4 MHz (Default0 Note: register 0x10 bit[0] = 1 enables 24-MHz sample mode
1-0	PWM HYST	R/W	01	Sets the minimum change in PWM input duty cycle that results in a change of backlight LED brightness level PWM Sample Frequency = 1 MHz or 4 MHz: 00: 1 bit 01: 2 bits 10: 4 bits 11: 6 bits PWM Sample Frequency = 24 MHz: 00: 0 01: 1 bit 10: 2 bits 11: 3 bits

7.6.4 Backlight Brightness LSB Register (Address = 0x04)[Reset = 0x07]

Figure 51. Backlight Brightness LSB Register

7	6	5	4	3	2	1	0
NOT USED					BRT[2]	BRT[1]	BRT[0]
					R/W-1	R/W-1	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 14. Backlight Brightness LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	NOT USED			
2-0	BRT	R/W	111	11-bit brightness code LSBs

7.6.5 Backlight Brightness MSB Register (Address = 0x05)[Reset = 0xFF]

Figure 52. Backlight Brightness MSB Register

7	6	5	4	3	2	1	0
BRT[10]	BRT[9]	BRT[8]	BRT[7]	BRT[6]	BRT[5]	BRT[4]	BRT[3]
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 15. Backlight Brightness MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BRT	R/W	11111111	11-bit brightness code MSBs

7.6.6 Backlight Auto-Frequency Low Threshold Register (Address = 0x06)[Reset = 0x00]

Figure 53. Backlight Auto-Frequency Low Threshold Register

7	6	5	4	3	2	1	0
AFLT[7]	AFLT[6]	AFLT[5]	AFLT[4]	AFLT[3]	AFLT[2]	AFLT[1]	AFLT[0]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 16. Backlight Auto-Frequency Low Threshold Field Descriptions

Bit	Field	Type	Reset	Description
7-0	AFLT	R/W	00000000	Compared against 8 MSB's of Brightness Code (register 0x05)

7.6.7 Backlight Auto-Frequency High Threshold Register (Address = 0x07)[Reset = 0x00]

Figure 54. Backlight Auto-Frequency High Threshold Register

7	6	5	4	3	2	1	0
AFHT[7]	AFHT[6]	AFHT[5]	AFHT[4]	AFHT[3]	AFHT[2]	AFHT[1]	AFHT[0]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 17. Backlight Auto-Frequency High Threshold Field Descriptions

Bit	Field	Type	Reset	Description
7-0	AFHT	R/W	00000000	Compared against 8 MSB's of Brightness Code (register 0x05)

7.6.8 Backlight Enable Register (Address = 0x08)[Reset = 0x00]

Figure 55. Backlight Enable Register

7	6	5	4	3	2	1	0
SOFTWARE_RESET	NOT USED		BL_EN	Reserved		LED2_EN	LED1_EN
R/W-0			R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 18. Backlight Enable Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SOFTWARE_RESET	R/W	0	0 = No reset 1 = Device reset (automatically returns to 0 after reset)
6-5	NOT USED			
4	BL_EN	R/W	0	0 = BL disabled (Default) 1 = BL enabled
3	Reserved	R/W	0	Must be written to 0
2	Reserved	R/W	0	Must be written to 0
1	LED2_EN	R/W	0	0 = Current sink 2 disabled 1 = Current sink 2 enabled
0	LED1_EN	R/W	0	0 = Current sink 1 disabled 1 = Current sink 1 enabled

7.6.9 Bias Configuration 1 Register (Address = 0x09)[Reset = 0x18]

Figure 56. Bias Configuration 1 Register

7	6	5	4	3	2	1	0
LCM_EN[2]	LCM_EN[1]	LCM_EN[0]	VPOS_DISCH	VNEG_DISCH	VPOS_EN	VNEG_EN	EXT_EN
R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 19. Bias Configuration 1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	LCM_EN	R/W	000	000 = Bias supply off (I^2C and external) 100 = Normal mode 101 = Auto sequence 110 = Wake1 111 = Wake2
4	VPOS_DISCH	R/W	1	0 = No pulldown on VPOS 1 = Pulldown on VPOS when in shutdown
3	VNEG_DISCH	R/W	1	0 = No pulldown on VNEG 1 = Pulldown on VNEG when in shutdown
2	VPOS_EN	R/W	0	0 = VPOS disabled 1 = VPOS enabled
1	VNEG_EN	R/W	0	0 = VNEG disabled 1 = VNEG enabled
0	EXT_EN	R/W	0	Activates external enables (LCM_EN1 and LCM_EN2) 0 = External enables are disabled. VPOS and VNEG can only be enabled via bit VPOS_EN and VNEG_EN, respectively. (Default) 1 = External enables are enabled. VPOS and VNEG can only be enabled via pin LCM_EN1 and LCM_EN2, respectively.

7.6.10 Bias Configuration 2 register (Address = 0x0A)[Reset = 0x11]

Figure 57. Bias Configuration 2 Register

7	6	5	4	3	2	1	0
BIAS_SHORT _MODE[1]	BIAS_SHORT _MODE[0]	VPOS _RAMP[1]	VPOS _RAMP[0]	VNEG _RAMP[3]	VNEG _RAMP[2]	VNEG _RAMP[1]	VNEG _RAMP[0]
R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 20. Bias Configuration 2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	BIAS_SHORT_MODE	R/W	00	0X = Flag only 10 = Flag + shutdown VPOS/VNEG 11 = Flag + shutdown VPOS/VNEG/Backlight
5:4	VPOS_RAMP	R/W	01	VPOS ramp time, low to high: 00 = 256 µs 01 = 512 µs 10 = 768 µs 11 = 1024 µs
3:0	VNEG_RAMP	R/W	0001	VNEG ramp time, high to low: 0000 = 512 µs 0001 = 1024 µs 0010 = 1536 µs 0011 = 2048 µs 0100 = 2560 µs 0101 = 3072 µs 0110 = 3584 µs 0111 = 4096 µs 1000 = 4608 µs 1001 = 5120 µs 1010 = 5632 µs 1011 = 6144 µs 1100 = 6656 µs 1101 = 7168 µs 1110 = 7680 µs 111 = 8192 µs

7.6.11 Bias Configuration 3 Register (Address = 0x0B)[Reset = 0x00]

Figure 58. Bias Configuration 3 Register

7	6	5	4	3	2	1	0
NOT USED				VPOS_SC _FILT[1]	VPOS_SC _FILT[0]	VNEG_SC _FILT[1]	VNEG_SC _FILT[0]
				R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21. Bias Configuration 3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	NOT USED			
5:4	VPOS_SC_FILT	R/W	00	VPOS short circuit filter timer 00 = 2 ms 01 = 1 ms 10 = 500 µs 11 = 100 µs
1:0	VNEG_SC_FILT	R/W	00	VNEG short circuit filter timer 00 = 2 ms 01 = 1 ms 10 = 500 µs 11 = 100 µs

7.6.12 LCM Boost Bias Register (Address = 0x0C)[Reset = 0x28]

Figure 59. LCM Boost Bias Register

7	6	5	4	3	2	1	0
NOT USED		LCM_OUT[5]	LCM_OUT[4]	LCM_OUT[3]	LCM_OUT[2]	LCM_OUT[1]	LCM_OUT[0]
		R/W-1	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 22. LCM Boost Bias Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	NOT USED			
5-0	LCM_OUT	R/W	101000	LCM_OUT voltage (50-mV steps): LCM_OUT = 4 V + (Code × 50 mV) 000000 = 4 V 000001 = 4.55V : 101000 = 6 V (Default) : 111111 = 7.15 V

7.6.13 VPOS Bias Register (Address = 0x0D)[Reset = 0x1E]

Figure 60. VPOS Bias Register

7	6	5	4	3	2	1	0
NOT USED		VPOS[5]	VPOS[4]	VPOS[3]	VPOS[2]	VPOS[1]	VPOS[0]
		R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 23. VPOS Bias Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	NOT USED			
5-0	VPOS	R/W	011110	VPOS voltage (50-mV steps): VPOS = 4 V + (Code × 50 mV), 6.5 V max 000000 = 4 V 000001 = 4.05 V : 011110 = 5.5 V (Default) : 110010 = 6.5 V 110011 to 111111 map to 6.5 V

7.6.14 VNEG Bias Register (Address = 0x0E)[Reset = 0x1C]

Figure 61. VNEG Bias Register

7	6	5	4	3	2	1	0
NOT USED		VNEG[5]	VNEG[4]	VNEG[3]	VNEG[2]	VNEG[1]	VNEG[0]
		R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 24. VNEG Bias Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	NOT USED			
5-0	VNEG	R/W	011100	VNEG voltage (–50-mV steps): VNEG = -4 V - (Code × 50 mV), -6.5 V min 000000 = –4 V 000000 = –4.05 V : 011100 = -5.4 V (Default) : 110010 = –6.5 V 110011 to 111111 map to –6.5 V

7.6.15 Flags Register (Address = 0x0F)[Reset = 0x00]

Figure 62. Flags Register

7	6	5	4	3	2	1	0
NOT USED	TSD	LCM_OVP	NOT USED	VPOS_SHORT	VNEG_SHORT	BL_OVP	BL_OCP
	R-0	R-0		R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 25. Flags Register Field Descriptions

Bit	Field	Type	Reset	Description
7	NOT USED			
6	TSD	R	0	0 = Normal operation 1 = Thermal shutdown triggered (die temperature > 140°C)
5	LCM_OVP	R	0	0 = Normal operation 1 = V_{LCM_OUT} > 7.8 V
4	NOT USED			
3	VPOS_SHORT	R	0	0 = Normal operation 1 = VPOS output has hit the overcurrent threshold
2	VNEG_SHORT	R	0	0 = Normal operation 1 = V_{VNEG} > 0.84 × V_{VNEG_target}
1	BL_OVP	R	0	0 = Normal operation 1 = Backlight boost output > OVP threshold
0	BL_OCP	R	0	0 = Normal operation 1 = Backlight boost switch current > OCP threshold

7.6.16 Option 1 Register (Address = 0x10)[Reset = 0x06]

Figure 63. Option 1 Register

7	6	5	4	3	2	1	0
NOT USED	Reserved		LED2_FB	LED1_FB	PWM_FILT[1]	PWM_ FILT[0]	PWM_24MHZ_ SAMPLE
RW-0	RW-0	RW-0	RW-0	RW-0	RW-1	RW-1	RW-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 26. Option 1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	NOT USED			
6	Reserved	R/W	0	Must be written to 0
5	Reserved	R/W	0	Must be written to 0
4	LED2_FEEDBACK_DISABLE	R/W	0	0 = Feedback enabled 1 = Feedback disabled
3	LED1_FEEDBACK_DISABLE	R/W	0	0 = Feedback enabled 1 = Feedback disabled
2:1	PWM_FILT	R/W	11	PWM Glitch Filter 00 = No filter 01 = 100 ns 10 = 150 ns 11 = 200 ns
0	PWM_24MHz_SAMPLE	R/W	0	0 = Low-frequency options (see 0x03 bit[2]) 1 = 24-MHz PWM sample frequency

7.6.17 Option 2 Register (Address = 0x11)[Reset = 0x35]

Figure 64. Option 2 Register

7	6	5	4	3	2	1	0
BL_L SELECT[1]	BL_L SELECT[0]	BL_SEL_P[1]	BL_SEL_P[0]	BL_SEL_I[1]	BL_SEL_I[0]	BL_CURRENT _LIMIT[1]	BL_CURRENT _LIMIT[0]
RW-0	RW-0	RW-1	RW-1	RW-0	RW-1	RW-0	RW-1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 27. Option 2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	BACKLIGHT_BOOST_L_SELECT	RW	00	00 = 4.7 µH 01 = 10 µH 10 = 15 µH 11 = 15 µH
5-4	BACKLIGHT_SEL_P	RW	11	These bits must be written to 11 (default values) to ensure backlight boost stability with recommended external components for all LED configurations
3-2	BACKLIGHT_SEL_I	RW	01	These bits must be written to 01 (default values) to ensure backlight boost stability with recommended external components for all LED configurations
1-0	BACKLIGHT_BOOST_CURRENT_ LIMIT	RW	01	00 = 0.9 A 01 = 1.2 A 10 = 1.5 A 11 = 1.8 A

7.6.18 PWM-to-Digital Code Readback LSB Register (Address = 0x12)[Reset = 0x00]

Figure 65. PWM-to-Digital Code Readback LSB Register

7	6	5	4	3	2	1	0
PWM_TO_DIG[7]	PWM_TO_DIG[6]	PWM_TO_DIG[5]	PWM_TO_DIG[4]	PWM_TO_DIG[3]	PWM_TO_DIG[2]	PWM_TO_DIG[1]	PWM_TO_DIG[0]
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 28. PWM-to-Digital Code Readback LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PWM_TO_DIG	R	00000000	11-bit PWM-to-digital conversion code LSBs

7.6.19 PWM-to-Digital Code Readback MSB Register (Address = 0x13)[Reset = 0x00]

Figure 66. PWM-to-Digital Code Readback MSB Register

7	6	5	4	3	2	1	0
RESERVED					PWM_TO_DIG[10]	PWM_TO_DIG[9]	PWM_TO_DIG[8]
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 29. PWM-to-Digital Code Readback MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	00000	Reserved
2-0	PWM_TO_DIG	R	000	11-bit PWM-to-digital conversion code MSBs

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM36272 integrates an LCD backlight driver and LCM positive and negative bias voltages into a single device. The backlight boost converter generates the high voltage required for the LEDs. The device can drive one or two LED strings with up to eight white LEDs per string. Positive and negative bias voltages are post-regulated from the LCM bias boost output voltage. The LM36272 offers high performance, is highly configurable, and can support multiple LED configurations as well as independent control of the bias outputs.

8.2 Typical Application

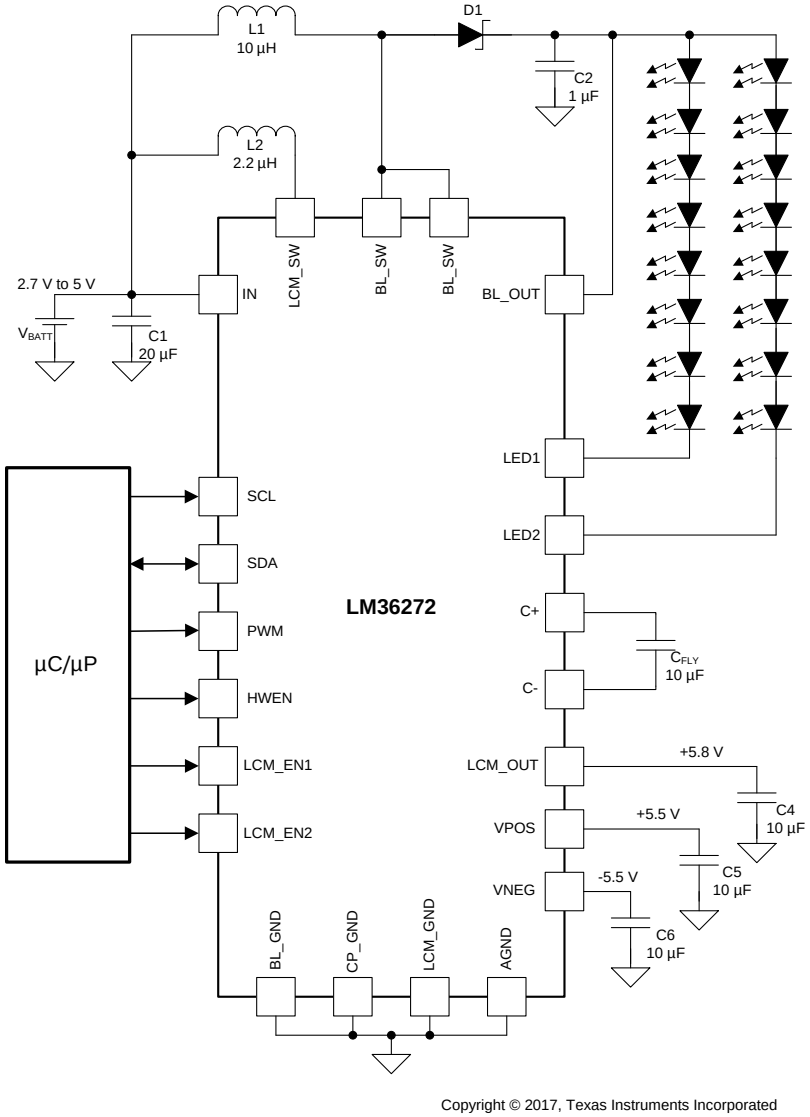


Figure 67. LM36272 Typical Application

Typical Application (continued)

8.2.1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range (V_{IN})	2.7 V to 4.5 V (single Li-Ion cell battery)
LED parallel/series configuration	2 parallel, 6 series
LED maximum forward voltage (V_f)	3.35 V
Backlight LED current	maximum 30 mA / string
Backlight boost maximum voltage	29 V
Backlight boost SW frequency	1 MHZ, 500 kHz, 250 kHz (auto-frequency option)
Backlight boost inductor	10-µH, 1.5-A saturation current
Backlight boost Schottky diode	NSR0530P2T5G
LCM boost output voltage	5.8 V
VPOS output voltage	5.5 V
VNEG output voltage	–5.5 V
LCM boost inductor	2.2-µH, 1.5-A saturation current

The number of LED strings, number of series LEDs, and minimum input voltage are needed in order to calculate the peak input current. This information guides the designer to make the appropriate backlight boost inductor selection for the application. The LM36272 backlight boost converter output voltage (V_{OUT}) is calculated as follows: number of series LEDs × V_f + 0.31 V. The LM36272 boost converter output current (I_{OUT}) is calculated as follows: number of parallel LED strings × 30 mA. The LM36272 peak input current is calculated using Equation 5.

8.2.2 Detailed Design Procedure

8.2.2.1 Component Selection

Table 30 shows examples of external components for the LM36272. Boost converter output capacitors can be replaced with dual output capacitors of lower capacitance as long as the minimum effective capacitance requirement is met. DC bias effect of the ceramic capacitors must be taken into consideration when choosing the output capacitors. This is especially true for the high output-voltage backlight-boost converter.

Table 30. Recommended External Components

DESIGNATOR	DESCRIPTION	VALUE	EXAMPLE
C1, C4, C5, C6, C_{FLY}	Ceramic capacitor	10 µF, 10 V	C1608X5R0J106M
C2	Ceramic capacitor	1 µF, 35 V	C2012X7R1H105K125AB
L1	Inductor	4.7 µH, 1.94 A	VLF504012MT-4R7M
L1	Inductor	10 µH, 1.44 A	VLF504015MT-100M
L1	Inductor	15 µH, 1.25 A	VLF504015MT-150M
L2	Inductor	2.2 µH, 1.5 A	DFE201612P-2R2M
D1	Schottky diode	30 V, 500 mA	NSR0530P2T5G

8.2.2.1.1 Inductor Selection

The LM36272 backlight boost requires a typical inductance in the range of 4.7 µH to 15 µH. To ensure boost stability the Backlight Boost L Select bit (register 0x11 bits [7:6]) must be selected depending on the value of inductance chosen. Use the 4.7-µH setting with a 6.8-µH inductor.

The LCM boost is internally compensated for a typical inductance in the range of 1 µH to 2.2 µH. If the LCM boost output setting is greater than 6.3 V a 2.2-µH inductor must be used.

There are two main considerations when choosing an inductor: the inductor RMS current rating must be greater than the RMS inductor current for the application, and the inductor saturation current must be greater than the peak inductor current for the application. Different saturation current rating specifications are followed by different manufacturers so attention must be given to details. Saturation current ratings are typically specified at 25°C. However, ratings at the maximum ambient temperature of the application should be requested from the manufacturer. The saturation current must be greater than the sum of the maximum load current and the worst-case average-to-peak inductor current. When the boost device is boosting ($V_{OUT} > V_{IN}$) the inductor is one of the largest area of efficiency loss in the circuit. Therefore, choosing an inductor with the lowest possible series resistance is important, especially for an LCM bias converter. For proper inductor operation and circuit performance, ensure that the inductor saturation and the peak current limit setting of the LM36272 are greater than I_{PEAK} in Equation 5:

$$I_{PEAK} = \frac{I_{LOAD}}{\eta} \times \frac{V_{OUT}}{V_{IN}} + \Delta I_{LOAD} \text{ where } \Delta I_{LOAD} = \frac{V_{IN} \times (V_{OUT} - V_{IN} \times \eta)}{2 \times f_{SW} \times L \times V_{OUT}} \quad (5)$$

See detailed information in *Understanding Boost Power Stages in Switch Mode Power Supplies* http://focus.ti.com/lit/an/slva061/slva061.pdf. *Power Stage Designer™ Tools* can be used for the boost calculation: http://www.ti.com/tool/powerstage-designer.

Also, the peak current calculated in Equation 5 is different from the peak inductor current setting (I_{SAT}). The NMOS switch current limit setting (I_{CL_MIN}) must be greater than I_{PEAK} from Equation 5.

8.2.2.1.2 Boost Output Capacitor Selection

At least an 1-µF capacitor is recommended for the backlight boost converter output capacitor. A high-quality ceramic type X5R or X7R is recommended. Voltage rating must be greater than the maximum output voltage that is used. The effective output capacitance must always remain higher than 0.4 µF for stable operation.

Table 31 lists possible backlight output capacitors that can be used with the LM36272. Figure 68 shows the DC bias of the four TDK capacitors. The useful voltage range is determined from the effective output voltage range for a given capacitor as determined by Equation 6:

$$\text{DC Voltage Derating} \geq \frac{0.4\ \mu F}{(1 - \text{Tol}) \times (1 - \text{Temp\_co})} \quad (6)$$

Table 31. Recommended Backlight Output Capacitors

PART NUMBER	MANUFACTURER	CASE SIZE	VOLTAGE RATING (V)	NOMINAL CAPACITANCE (µF)	TOLERANCE (%)	TEMPERATURE COEFFICIENT (%)	RECOMMENDED MAX OUTPUT VOLTAGE (FOR SINGLE CAPACITOR)
C2012X5R1H105K085AB	TDK	0805	50	1	±10	±15	22
C2012X5R1H225K085AB	TDK	0805	50	2.2	±10	±15	24
C1608X5R1V225K080AC	TDK	0603	35	2.2	±10	±15	12
C1608X5R1H105K080AB	TDK	0603	50	1	±10	±15	15

For example, with a 10% tolerance, and a 15% temperature coefficient, the DC voltage derating must be ≥ 0.4 / (0.9 × 0.85) = 0.523 µF. For the C1608X5R1H225K080AB (0603, 50-V) device, the useful voltage range occurs up to the point where the DC bias derating falls below 0.523 µF, or around 12 V. For configurations where V_{OUT} is > 15 V, two of these capacitors can be paralleled, or a larger capacitor such as the C2012X5R1H105K085AB must be used.

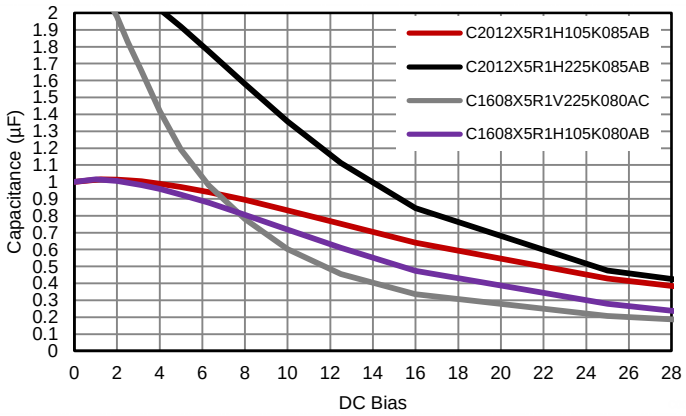


Figure 68. DC Bias Derating for 0805 Case Size and 0603 Case Size 35-V and 50-V Ceramic Capacitors

For the LCM bias boost output a high-quality 10-µF ceramic type X5R or X7R capacitor is recommended. Voltage rating must be greater than the maximum output voltage that is used.

8.2.2.1.3 Input Capacitor Selection

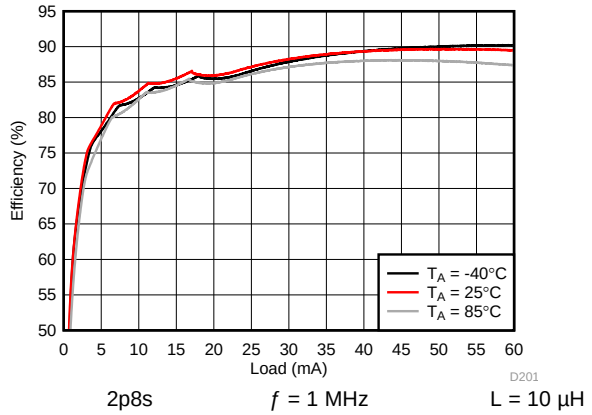
Choosing the correct size and type of input capacitor helps minimize the voltage ripple caused by the switching of the LM36272 boost converters and reduce noise on the input pin that can feed through and disrupt internal analog signals. For the LM36272 a 10-µF ceramic input capacitor works well. It is important to place the input capacitor as close to the input (IN) pin as possible. This reduces the series resistance and inductance that can inject noise into the device due to the input switching currents.

8.2.3 Application Curves

8.2.3.1 Backlight Curves

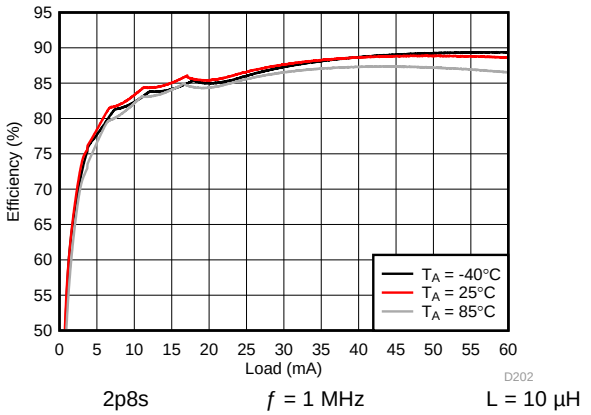
Ambient temperature is 25°C and V_{IN} is 3.7 V unless otherwise noted. Backlight system efficiency is defined as PLED / PIN, where PLED is actual power consumed in backlight LEDs. External components are from Table 30.

8.2.3.1.1 Two LED Strings



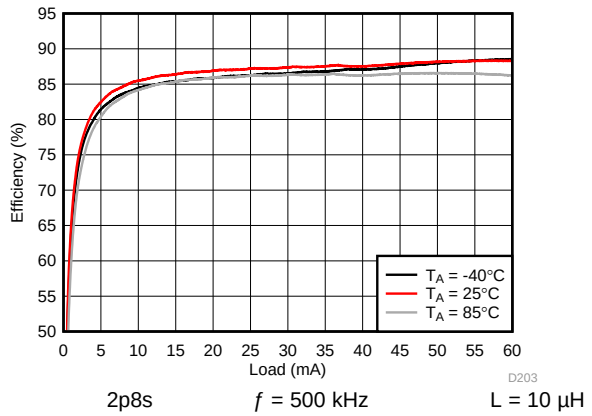
2p8s f = 1 MHz L = 10 µH

Figure 69. Backlight Boost Efficiency



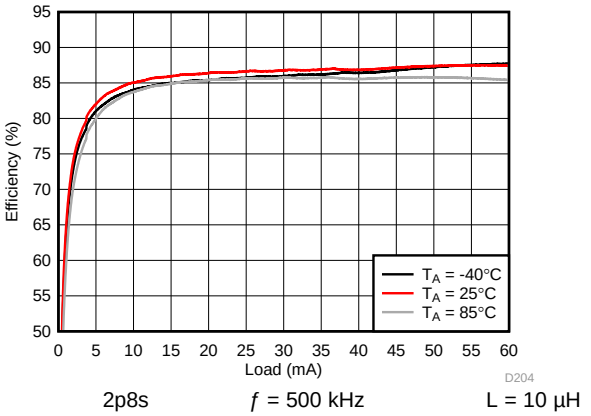
2p8s f = 1 MHz L = 10 µH

Figure 70. Backlight System Efficiency



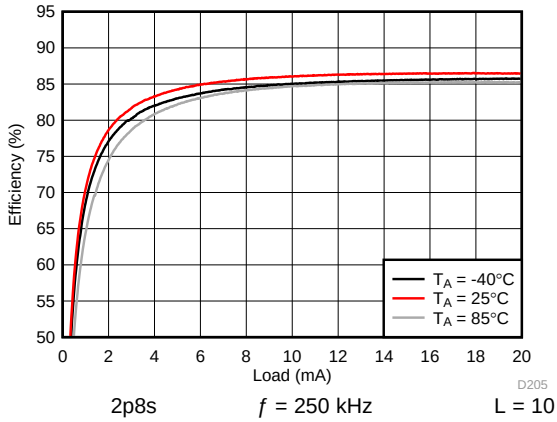
2p8s f = 500 kHz L = 10 µH

Figure 71. Backlight Boost Efficiency



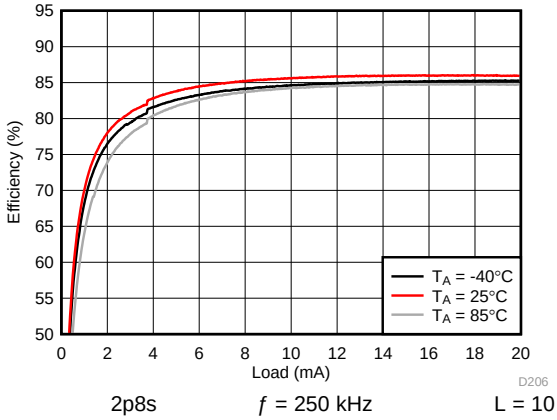
2p8s f = 500 kHz L = 10 µH

Figure 72. Backlight System Efficiency



2p8s f = 250 kHz L = 10 µH

Figure 73. Backlight Boost Efficiency



2p8s f = 250 kHz L = 10 µH

Figure 74. Backlight System Efficiency

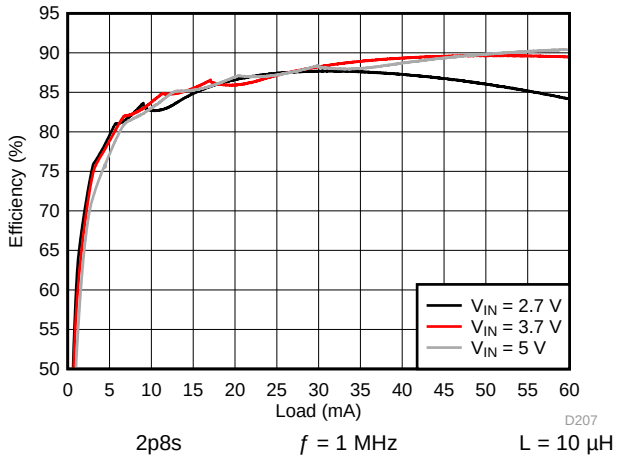


Figure 75. Backlight Boost Efficiency

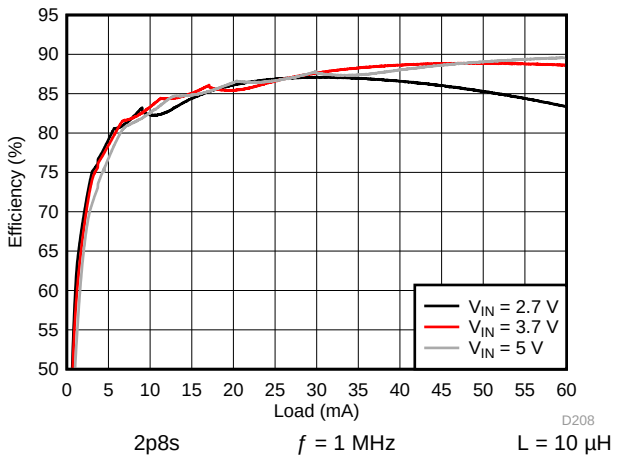


Figure 76. Backlight System Efficiency

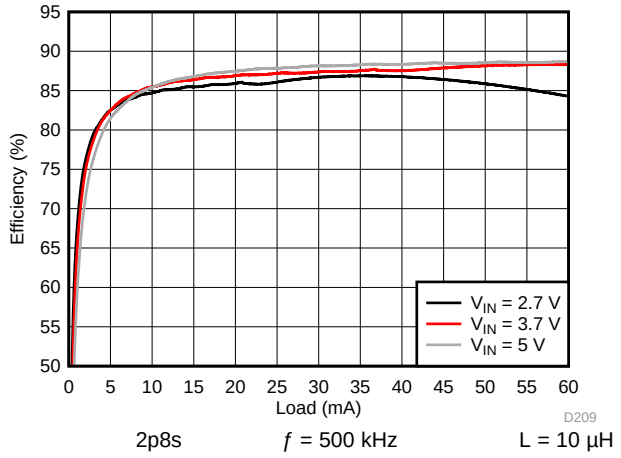


Figure 77. Backlight Boost Efficiency

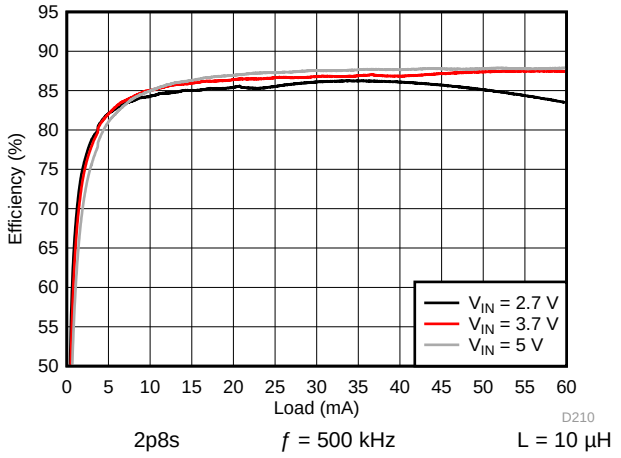


Figure 78. Backlight System Efficiency

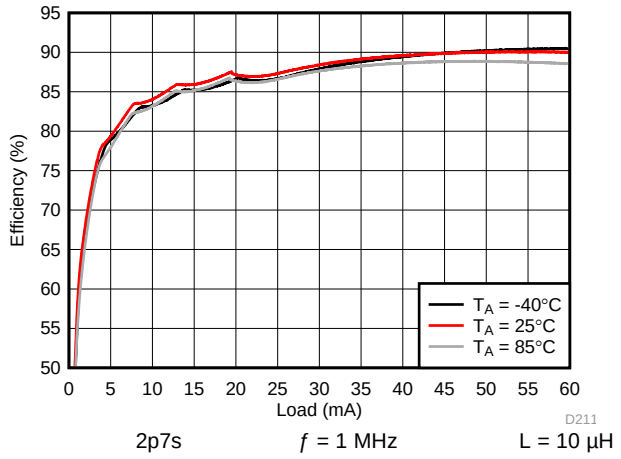


Figure 79. Backlight Boost Efficiency

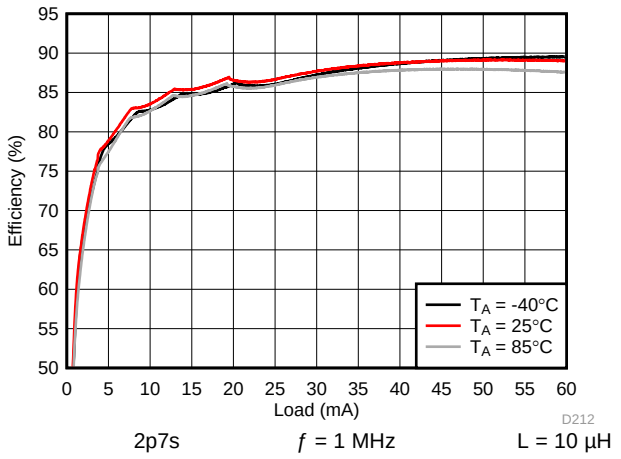


Figure 80. Backlight System Efficiency

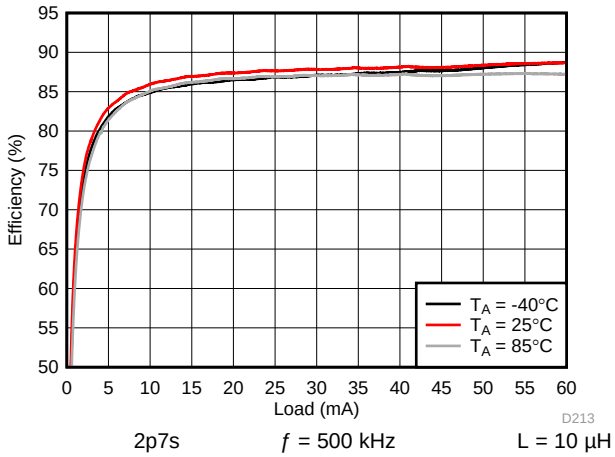


Figure 81. Backlight Boost Efficiency

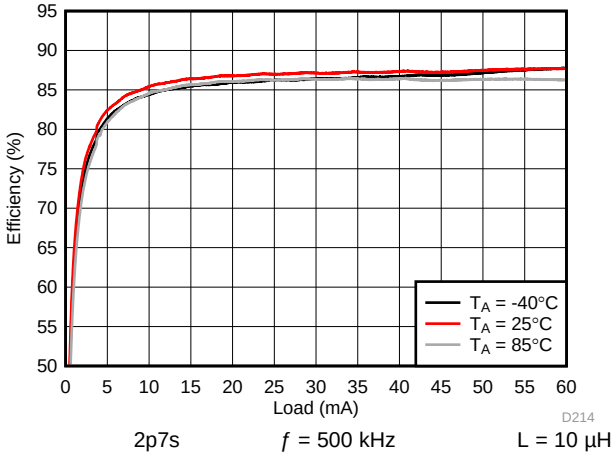


Figure 82. Backlight System Efficiency

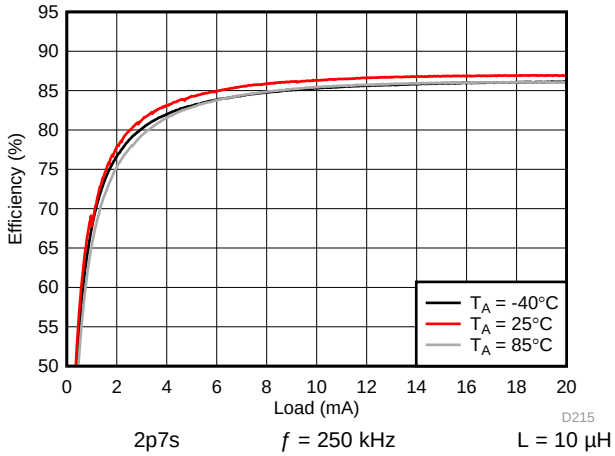


Figure 83. Backlight Boost Efficiency

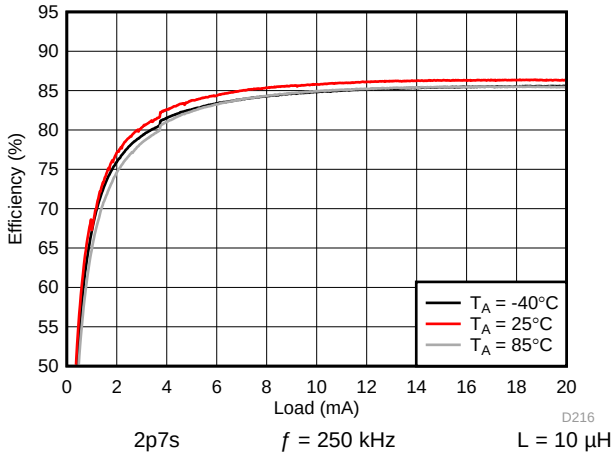


Figure 84. Backlight System Efficiency

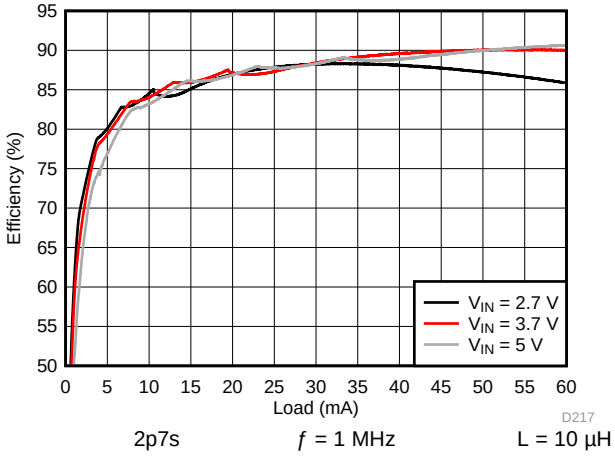


Figure 85. Backlight Boost Efficiency

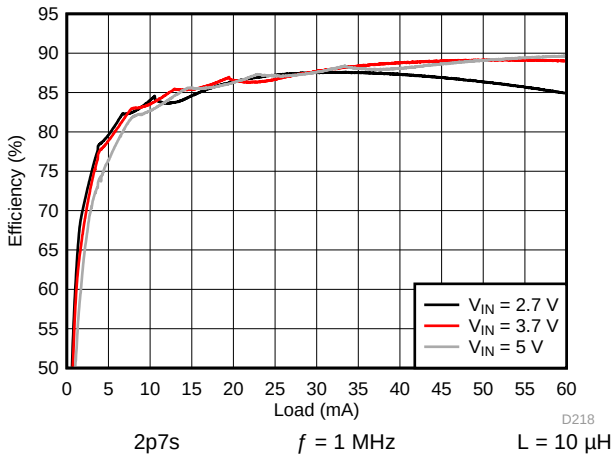
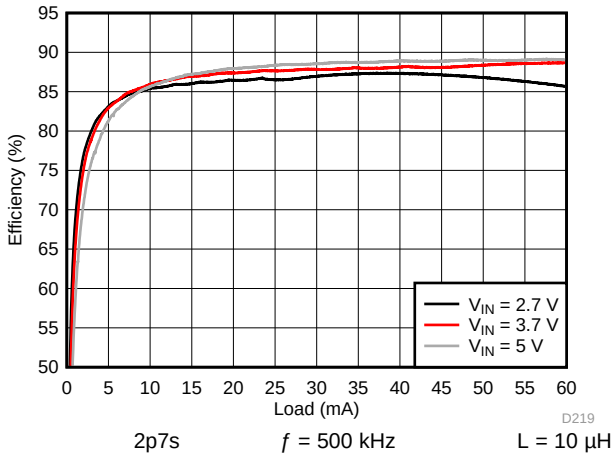
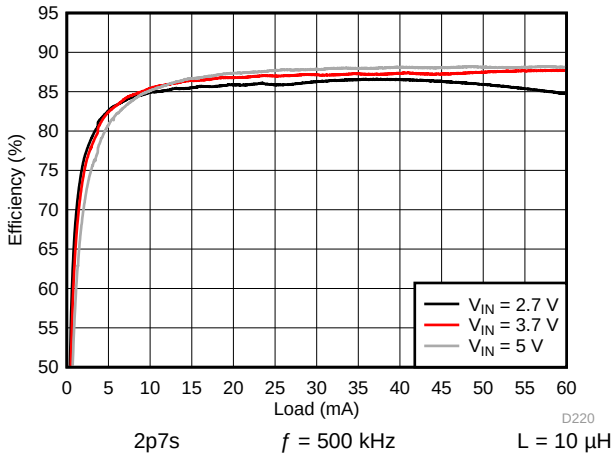


Figure 86. Backlight System Efficiency



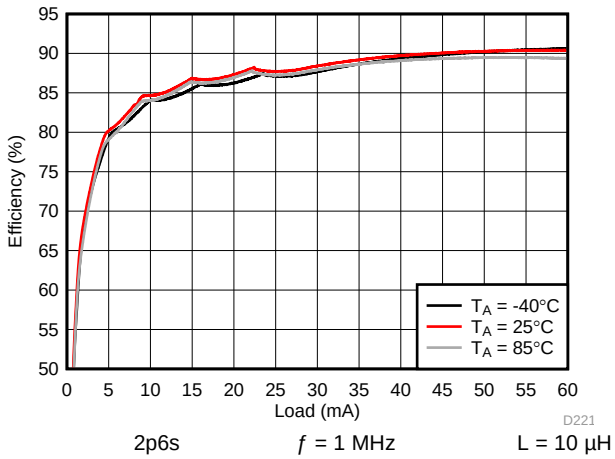
2p7s f = 500 kHz L = 10 µH

Figure 87. Backlight Boost Efficiency



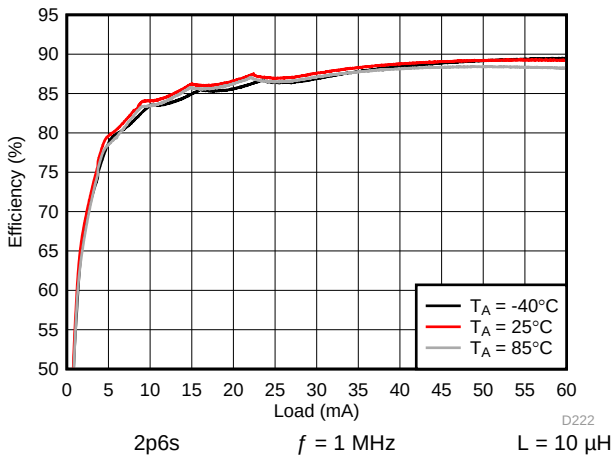
2p7s f = 500 kHz L = 10 µH

Figure 88. Backlight System Efficiency



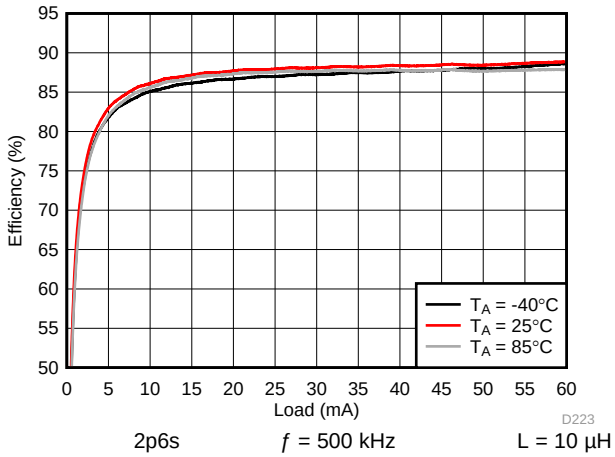
2p6s f = 1 MHz L = 10 µH

Figure 89. Backlight Boost Efficiency



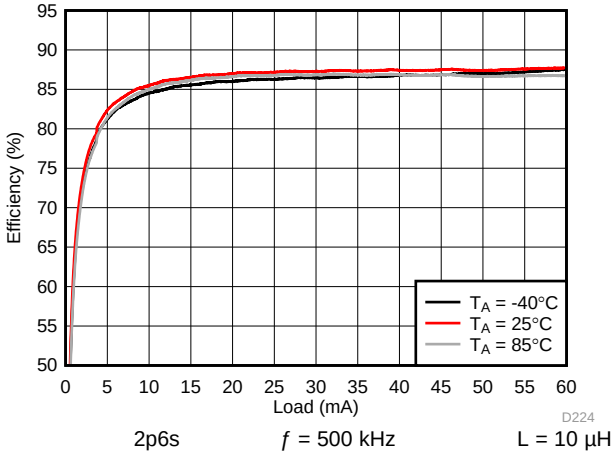
2p6s f = 1 MHz L = 10 µH

Figure 90. Backlight System Efficiency



2p6s f = 500 kHz L = 10 µH

Figure 91. Backlight Boost Efficiency



2p6s f = 500 kHz L = 10 µH

Figure 92. Backlight System Efficiency

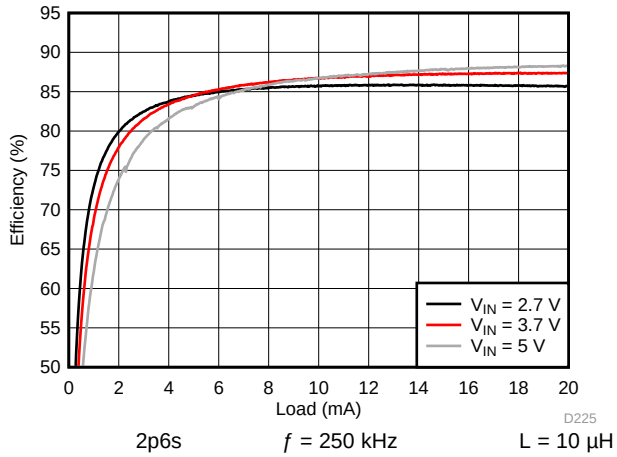


Figure 93. Backlight Boost Efficiency

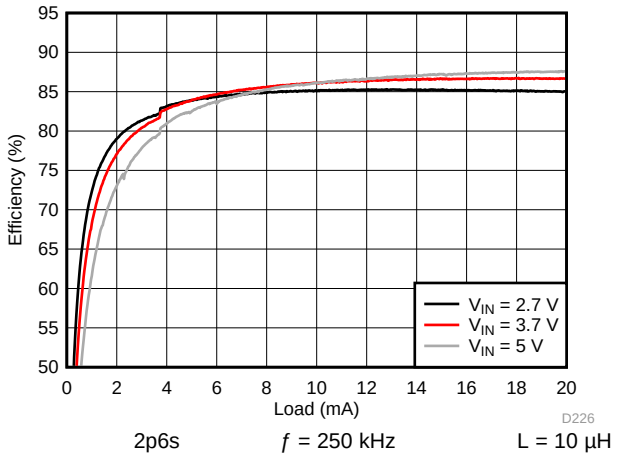


Figure 94. Backlight System Efficiency

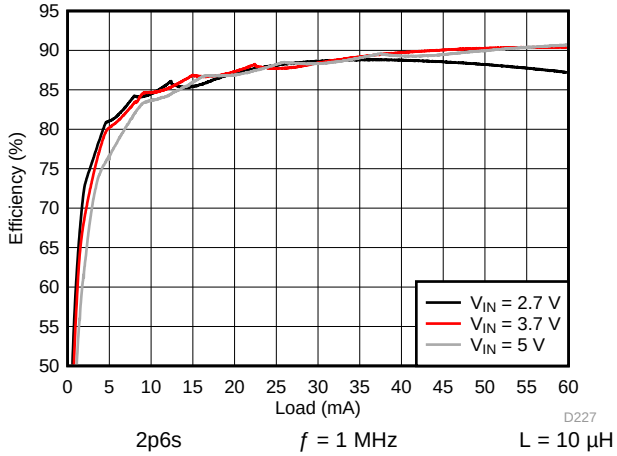


Figure 95. Backlight Boost Efficiency

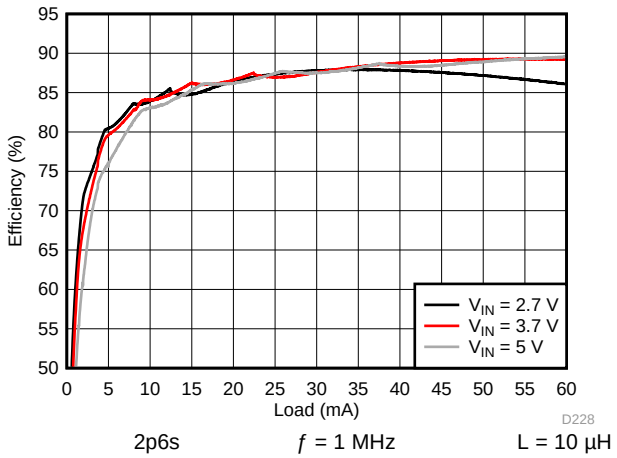


Figure 96. Backlight System Efficiency

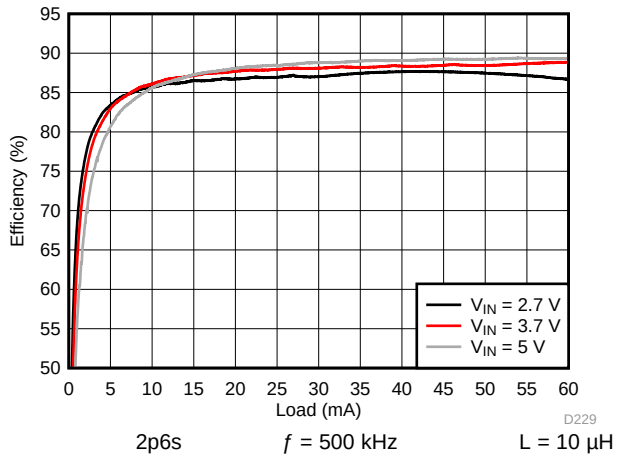


Figure 97. Backlight Boost Efficiency

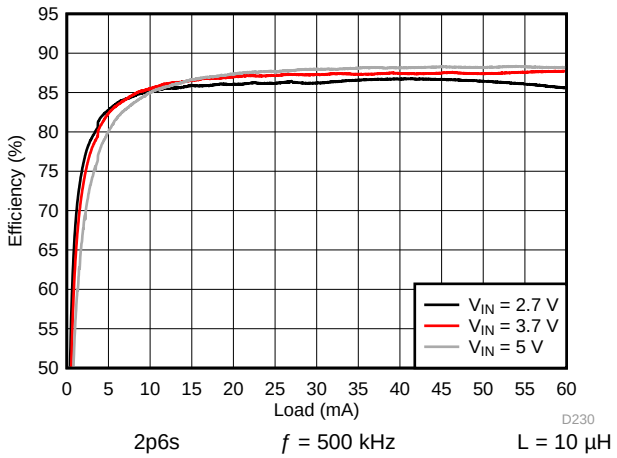


Figure 98. Backlight System Efficiency

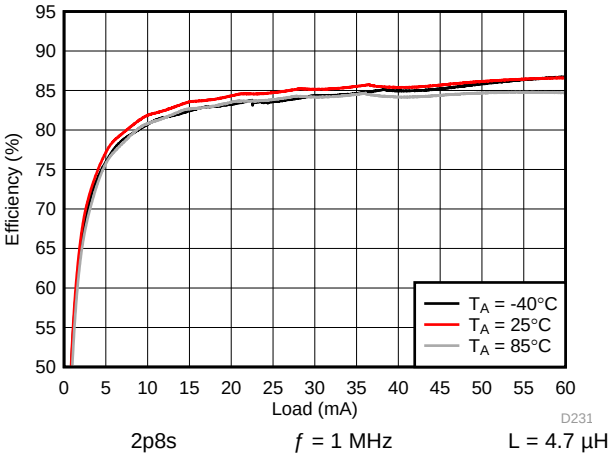


Figure 99. Backlight Boost Efficiency

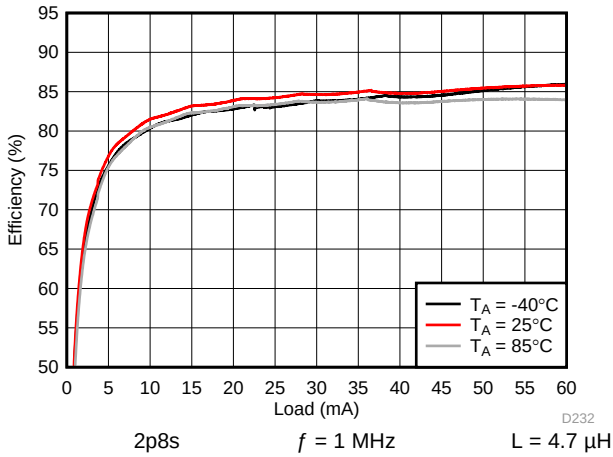


Figure 100. Backlight System Efficiency

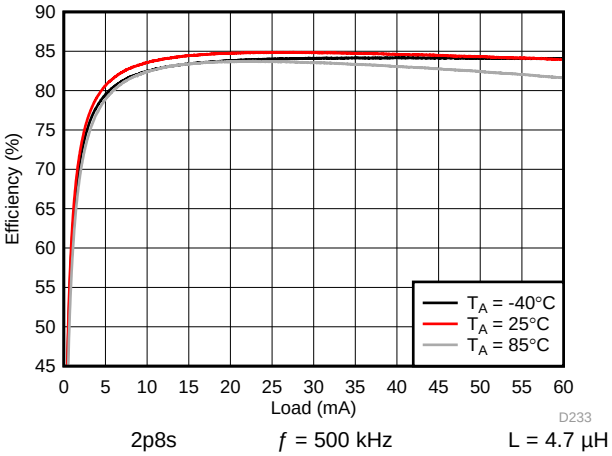


Figure 101. Backlight Boost Efficiency

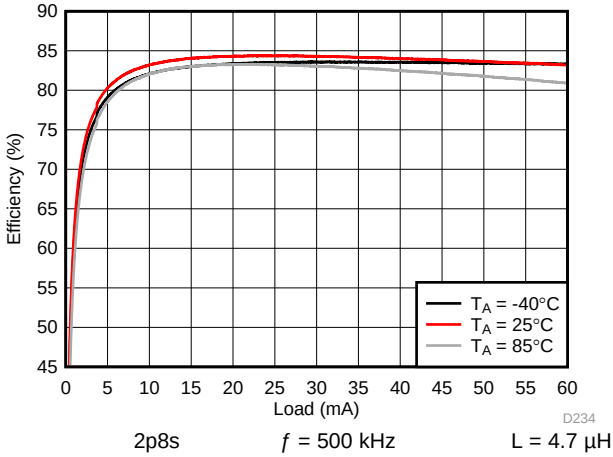


Figure 102. Backlight System Efficiency

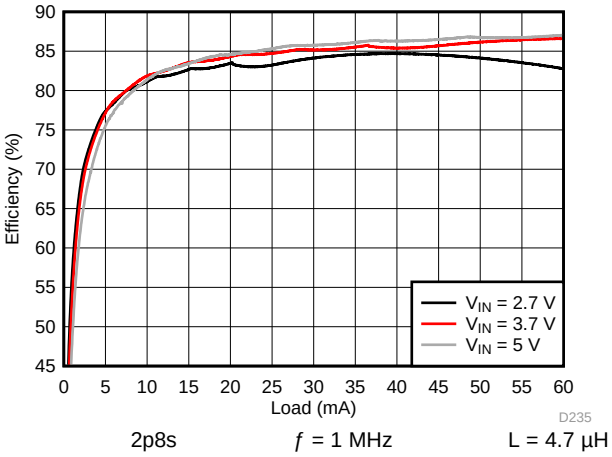


Figure 103. Backlight Boost Efficiency

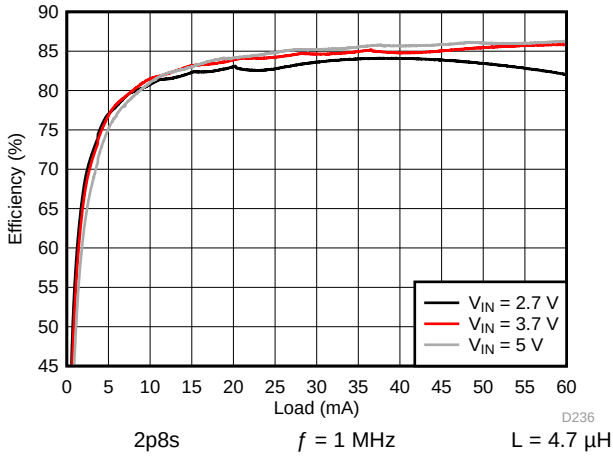


Figure 104. Backlight System Efficiency

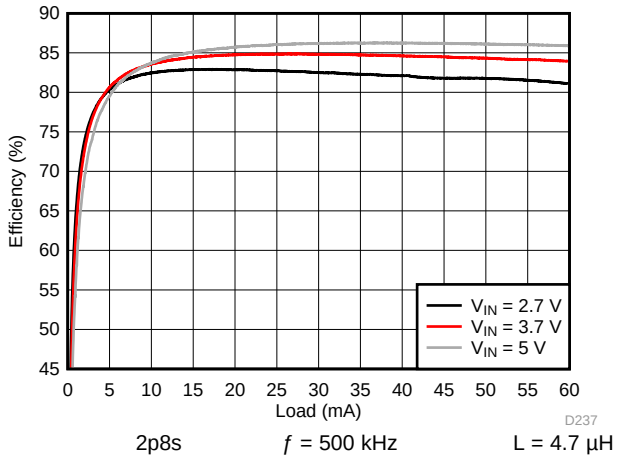


Figure 105. Backlight Boost Efficiency

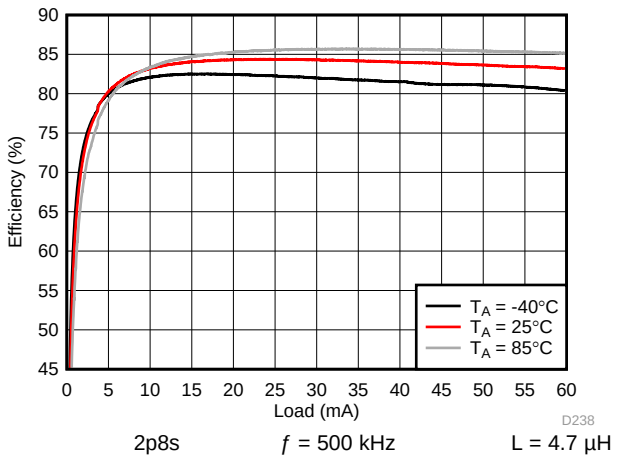


Figure 106. Backlight System Efficiency

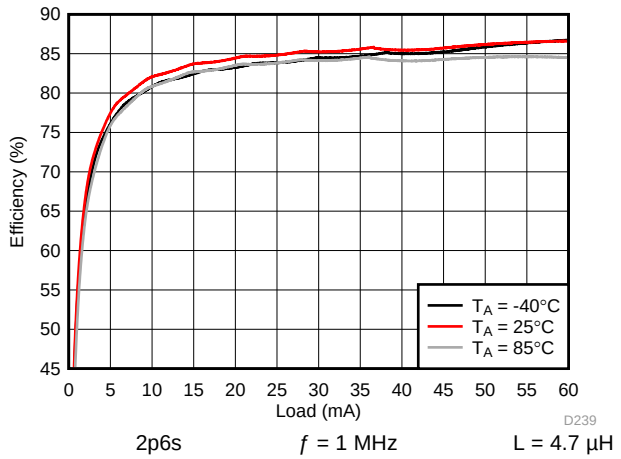


Figure 107. Backlight Boost Efficiency

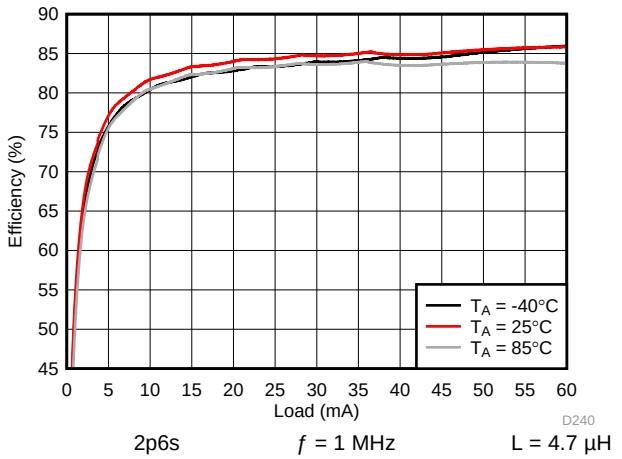


Figure 108. Backlight System Efficiency

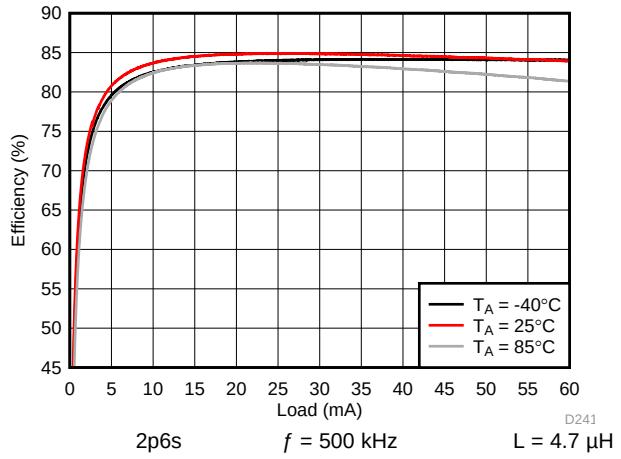


Figure 109. Backlight Boost Efficiency

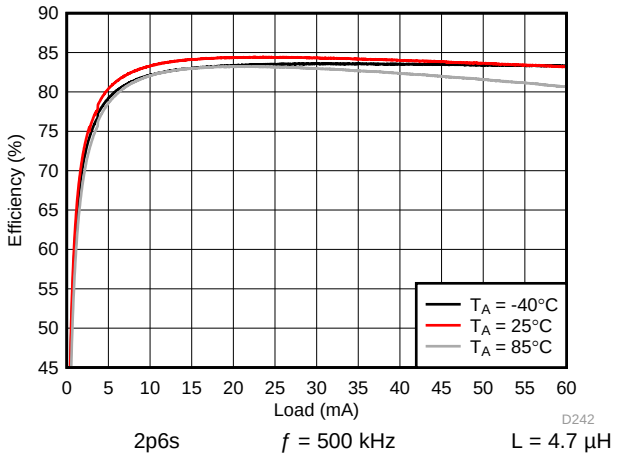


Figure 110. Backlight System Efficiency

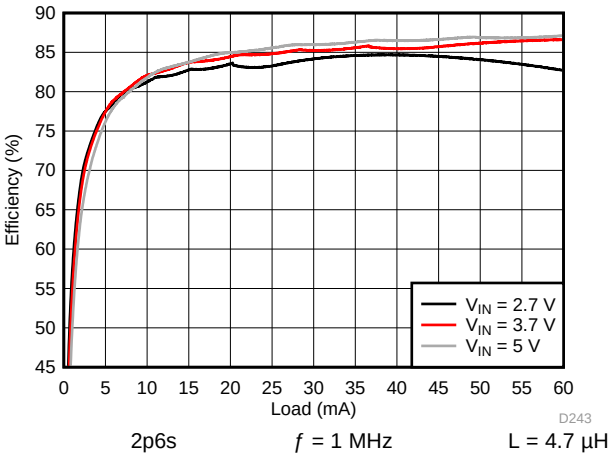


Figure 111. Backlight Boost Efficiency

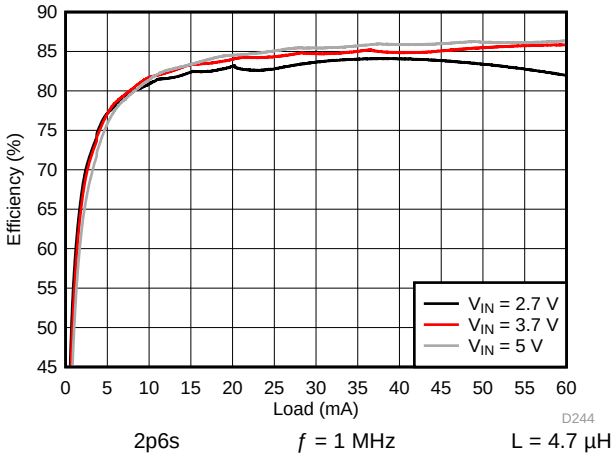


Figure 112. Backlight System Efficiency

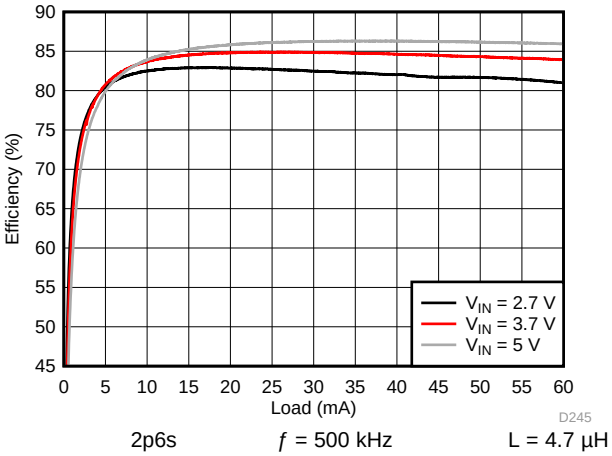


Figure 113. Backlight Boost Efficiency

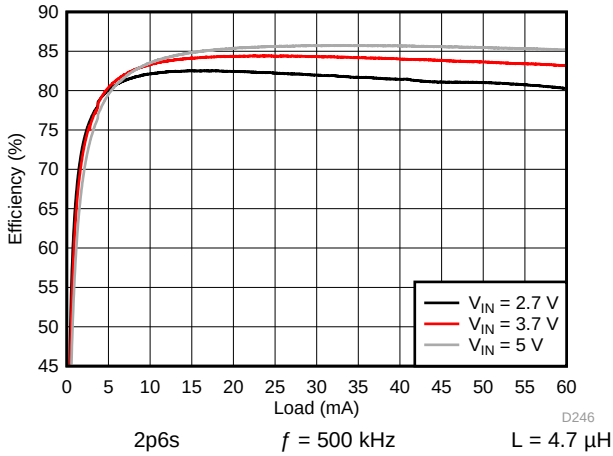
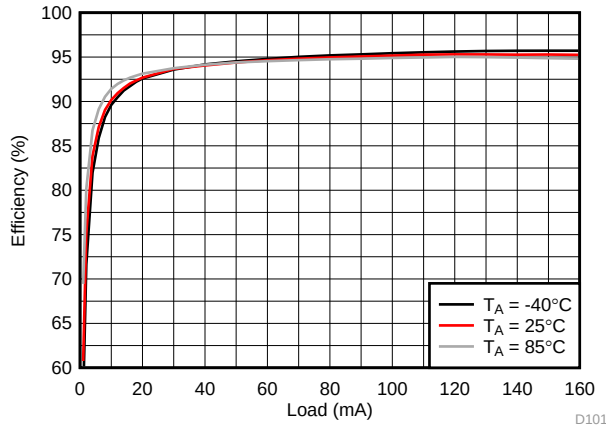


Figure 114. Backlight System Efficiency

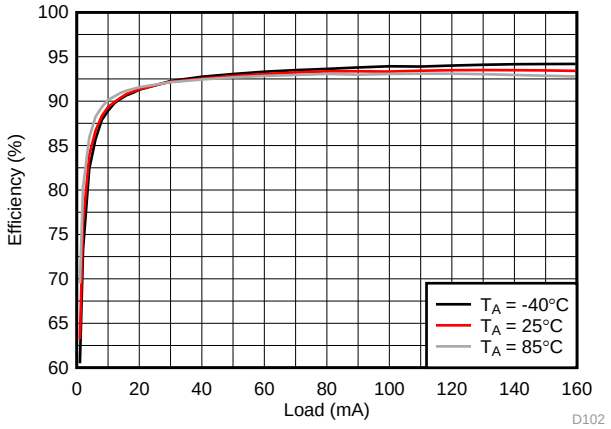
8.2.3.2 LCM Bias Curves

Ambient temperature is 25°C and V_{IN} is 3.7 V unless otherwise noted. VPOS, VNEG and VPOS/VNEG efficiency is defined as POUT / PIN, where POUT is actual power consumed in VPOS, VNEG and (VPOS + VNEG) outputs, respectively. External components are from Table 30.



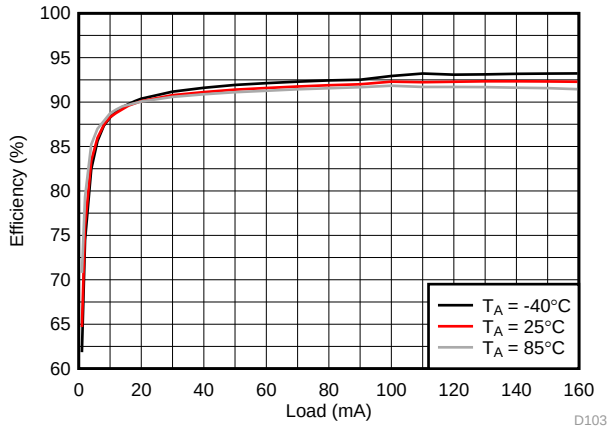
V_{LCM_OUT} = 4.3 V

Figure 115. LCM Boost Efficiency



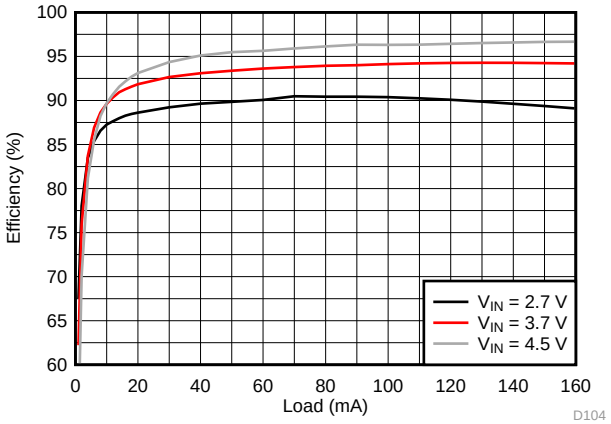
V_{LCM_OUT} = 5.3 V

Figure 116. LCM Boost Efficiency



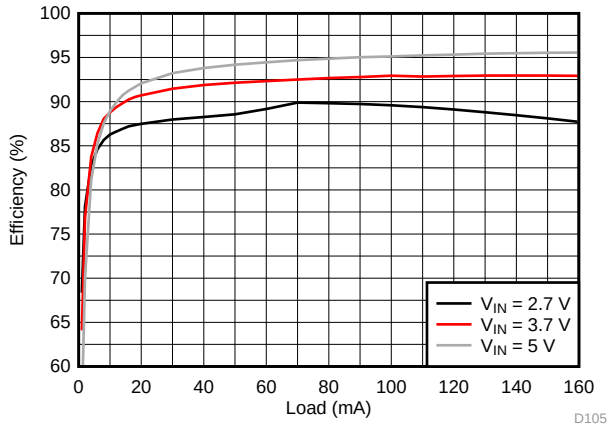
V_{LCM_OUT} = 6.3 V

Figure 117. LCM Boost Efficiency



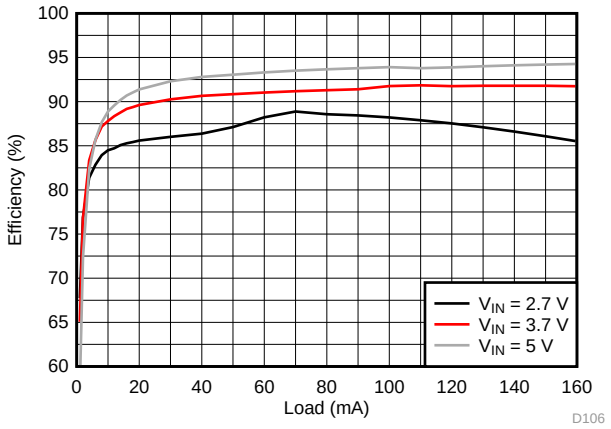
V_{LCM_OUT} = 4.8 V

Figure 118. LCM Boost Efficiency



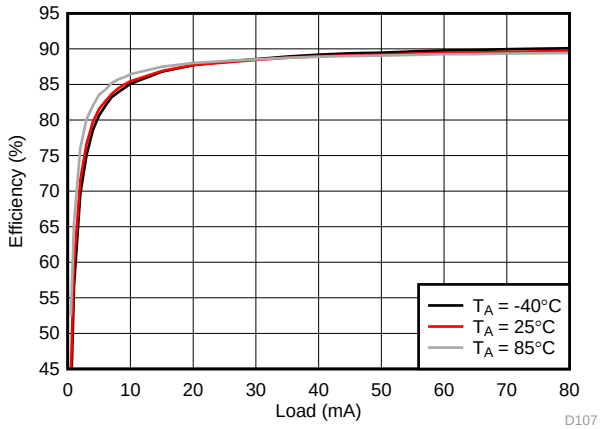
V_{LCM_OUT} = 5.8 V

Figure 119. LCM Boost Efficiency



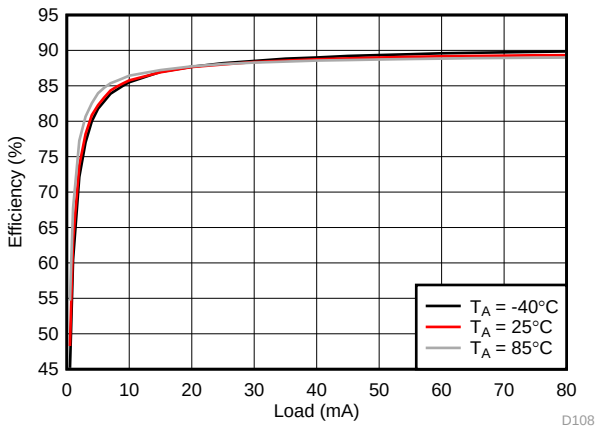
V_{LCM_OUT} = 6.8 V

Figure 120. LCM Boost Efficiency



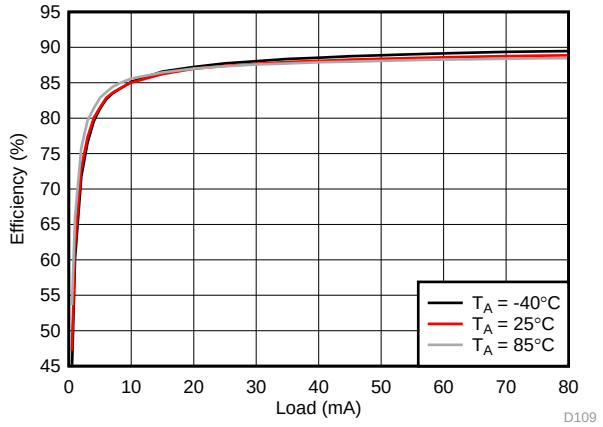
V_{VPOS} = 4 V V_{LCM_OUT} = 4.3 V

Figure 121. VPOS Efficiency



V_{VPOS} = 5 V V_{LCM_OUT} = 5.3 V

Figure 122. VPOS Efficiency



V_{VPOS} = 6 V V_{LCM_OUT} = 6.3 V

Figure 123. VPOS Efficiency

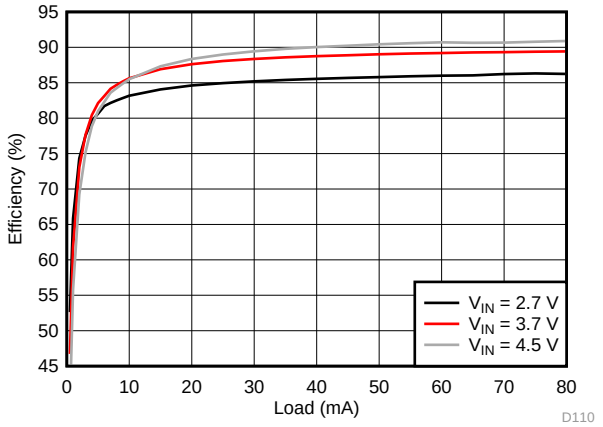
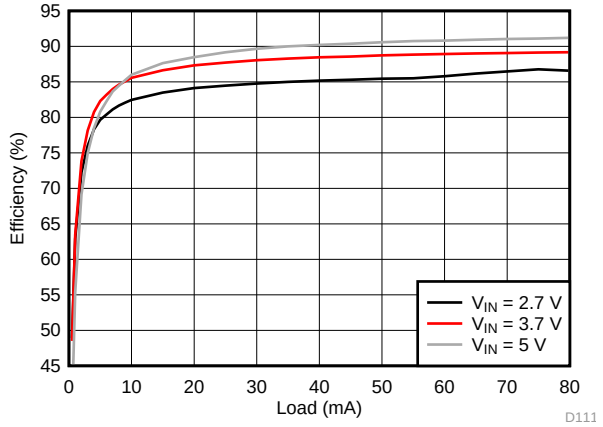
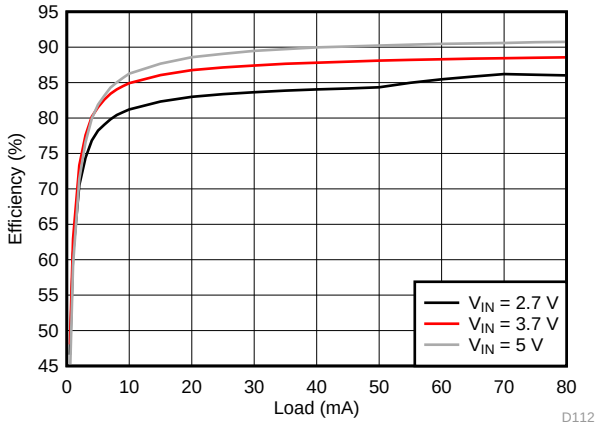


Figure 124. VPOS Efficiency



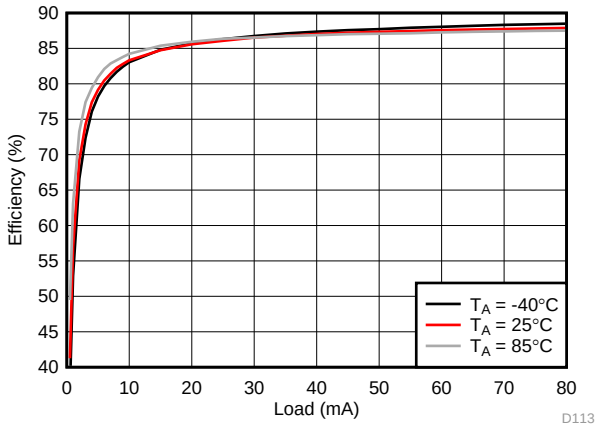
V_{VPOS} = 6 V V_{LCM_OUT} = 6.3 V

Figure 125. VPOS Efficiency



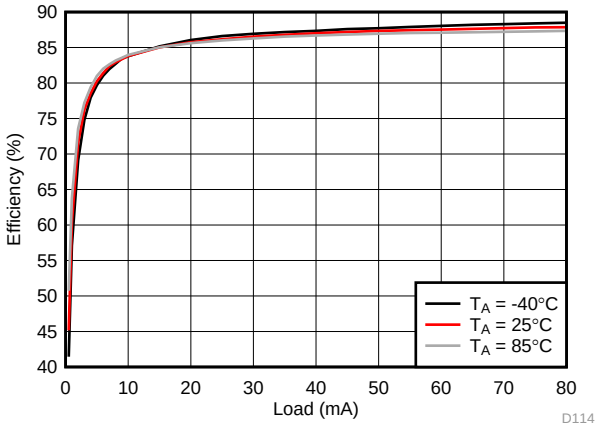
V_{VPOS} = 6.5 V V_{LCM_OUT} = 6.8 V

Figure 126. VPOS Efficiency



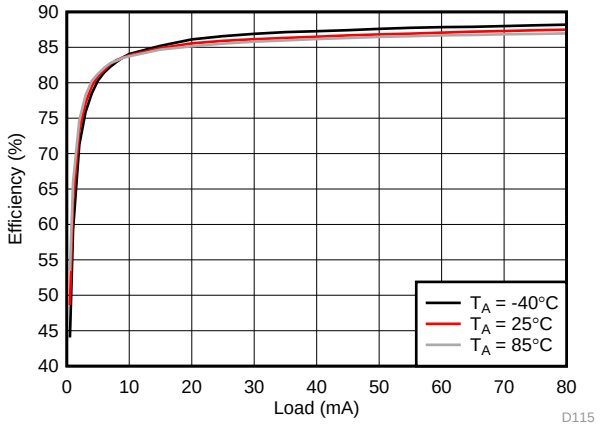
V_{VNEG} = -4 V V_{LCM_OUT} = 4.3 V

Figure 127. VNEG Efficiency



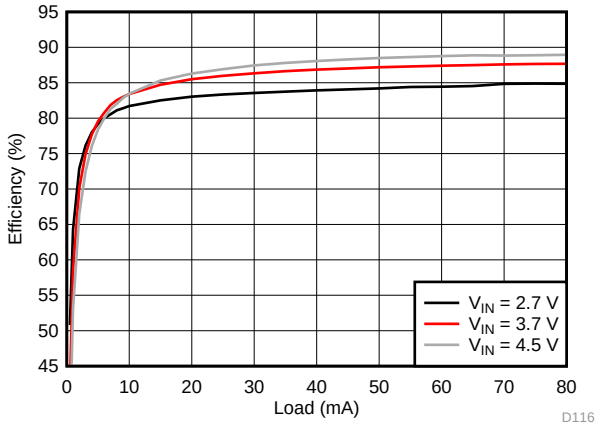
V_{VNEG} = -5 V V_{LCM_OUT} = 5.3 V

Figure 128. VNEG Efficiency



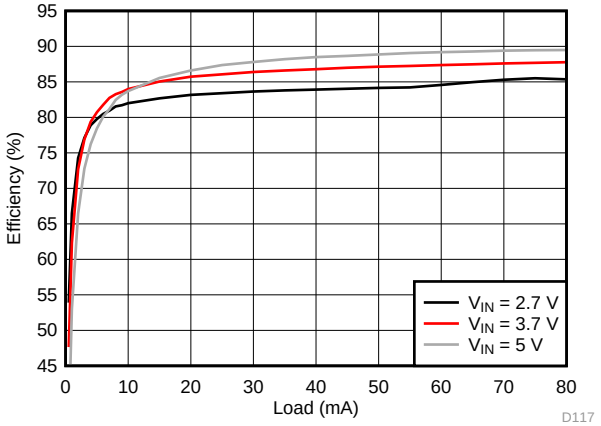
V_{VNEG} = -6 V V_{LCM_OUT} = 6.3 V

Figure 129. VNEG Efficiency



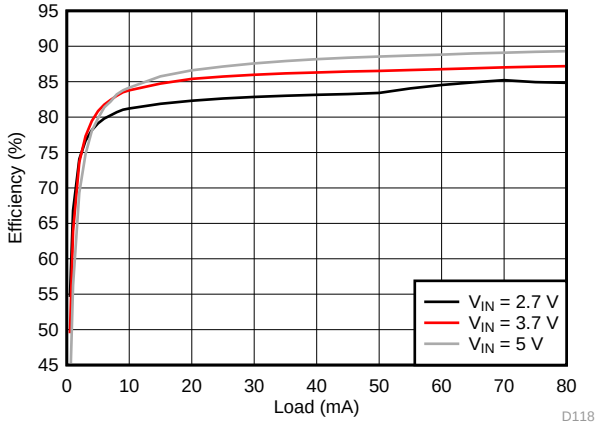
V_{VNEG} = –4.5 V V_{LCM_OUT} = 4.8 V

Figure 130. VNEG Efficiency



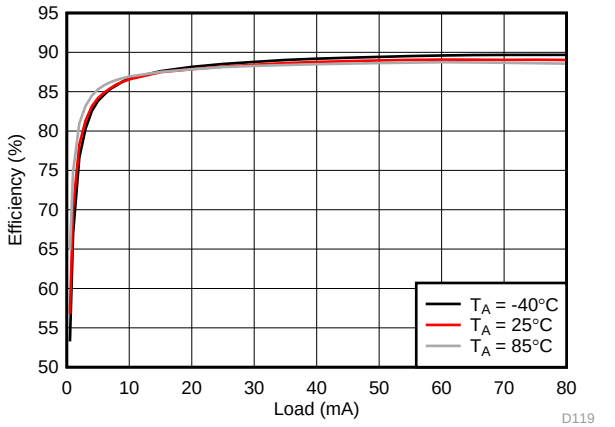
V_{VNEG} = –5.5 V V_{LCM_OUT} = 5.8 V

Figure 131. VNEG Efficiency



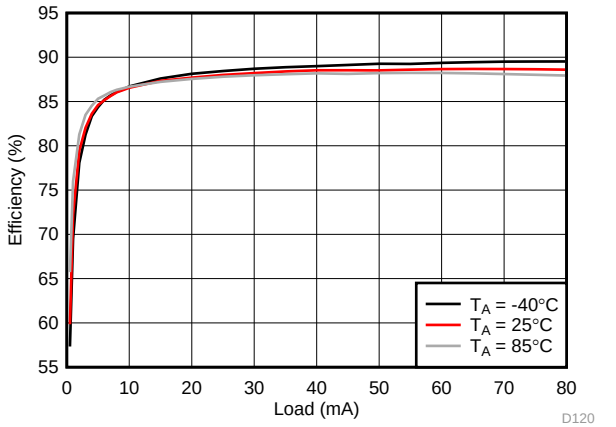
V_{VNEG} = –6.5 V V_{LCM_OUT} = 6.8 V

Figure 132. VNEG Efficiency



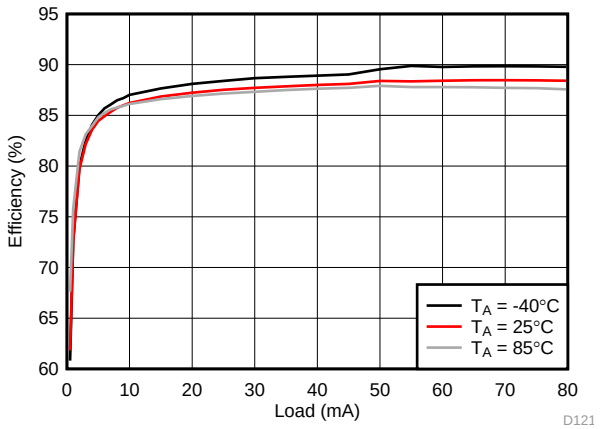
V_{VPOS} = 4 V V_{VNEG} = –4 V V_{LCM_OUT} = 4.3 V

Figure 133. VPOS/VNEG Efficiency



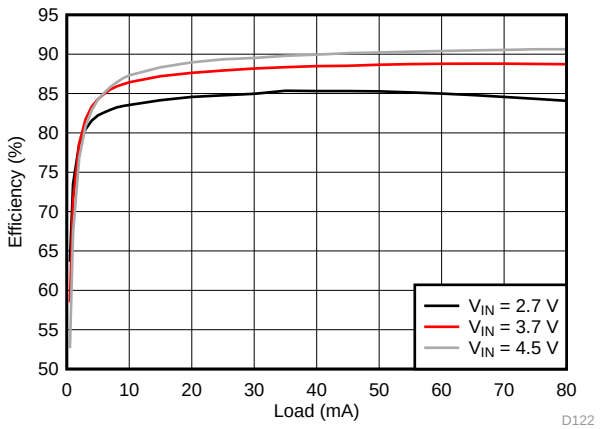
V_{VPOS} = 5 V V_{VNEG} = –5 V V_{LCM_OUT} = 5.3 V

Figure 134. VPOS/VNEG Efficiency



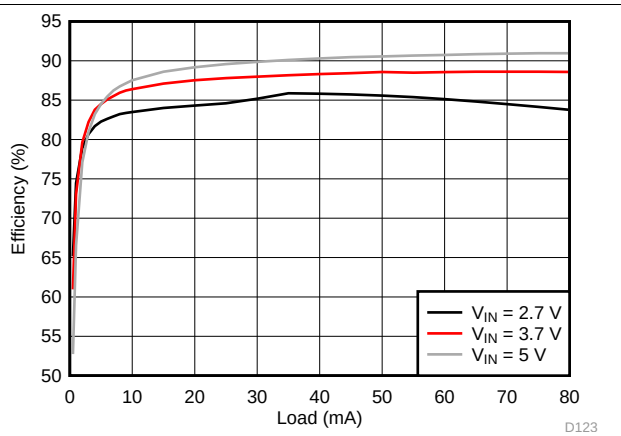
V_{VPOS} = 6 V V_{VNEG} = –6 V V_{LCM_OUT} = 6.3 V

Figure 135. VPOS/VNEG Efficiency



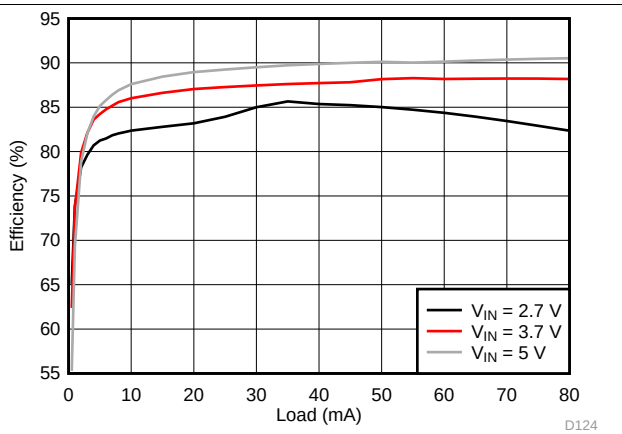
V_{VPOS} = 4.5 V V_{VNEG} = –4.5 V V_{LCM_OUT} = 4.8 V

Figure 136. VPOS/VNEG Efficiency



V_{VPOS} = 5.5 V V_{VNEG} = –5.5 V V_{LCM_OUT} = 5.8 V

Figure 137. VPOS/VNEG Efficiency



V_{VPOS} = 6.5 V V_{VNEG} = –6.5 V V_{LCM_OUT} = 6.8 V

Figure 138. VPOS/VNEG Efficiency

9 Power Supply Recommendations

The LM36272 is designed to operate from an input voltage supply range from 2.7 V to 5 V. This input supply must be well regulated and capable to supply the required input current. If the input supply is located far from the LM36272 additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

10 Layout

10.1 Layout Guidelines

- Place the boost converter output capacitors as close to the output voltage and GND pins as possible.
- Minimize the boost converter switching loops by placing the input capacitors and inductors close to GND and switch pins.
- If possible, route the switching loops on top layer only. For best efficiency, try to minimize copper on the switch node to minimize switch pin parasitic capacitance while preserving adequate routing width.
- VIN input voltage pin must be bypassed to ground with a low-ESR bypass capacitor. Place the capacitor as close as possible to VIN pin.
- Place the output capacitor of the LDO as close to the output pins as possible. Also place the charge pump flying capacitor and output capacitor close to their respective pins.
- Route the internal pins on the second layer. Use offset micro vias to go from top layer to mid-layer1. Avoid routing the signal traces directly under the switching loops of the boost converters.

10.2 Layout Example

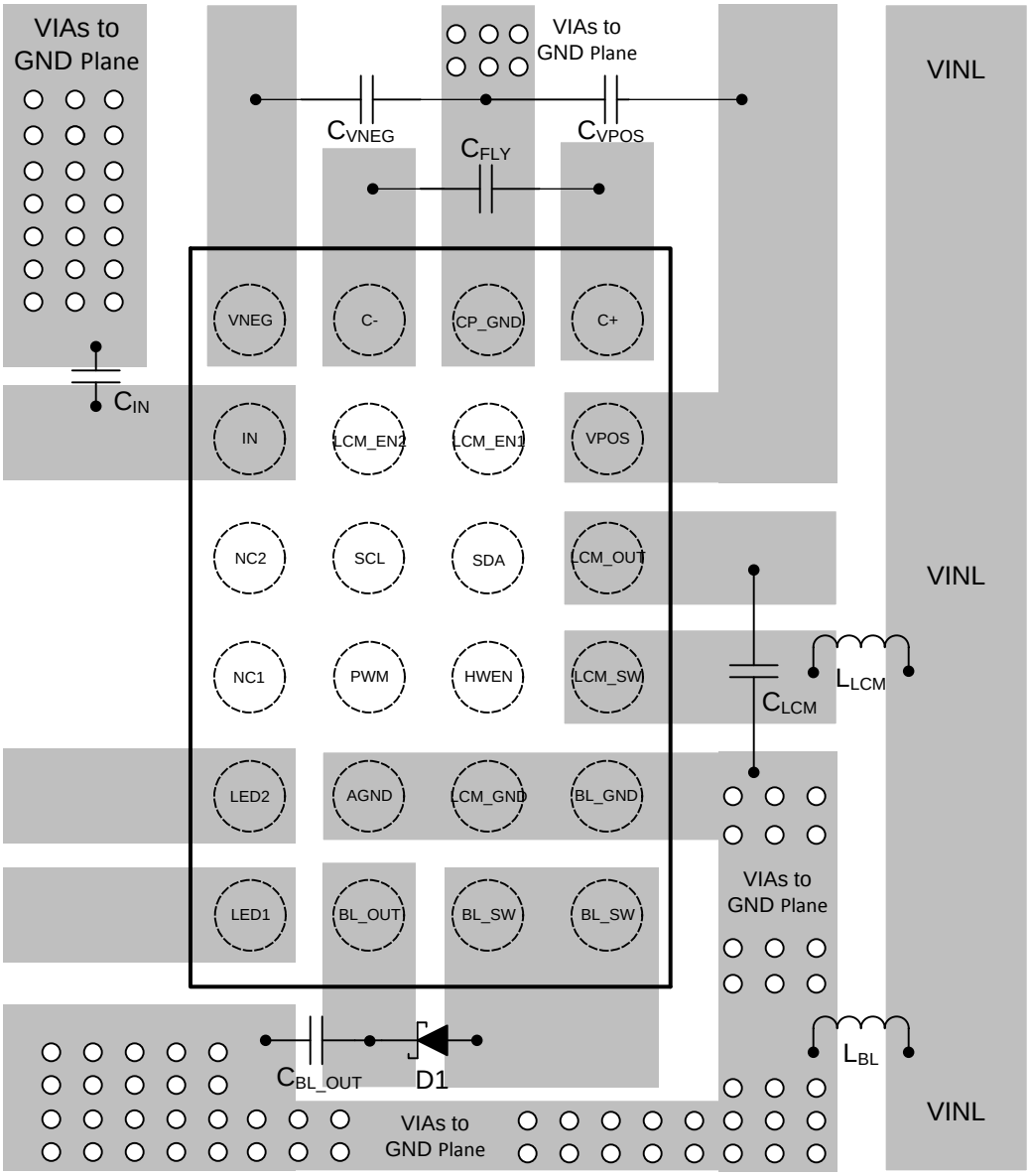


Figure 139. LM36272 Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.1.2 Development Support

Power Stage Designer™ tools can be used for the boost calculation: http://www.ti.com/tool/powerstage-designer

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- *AN-1112 DSBGA Wafer Level Chip Scale Package*
- *Understanding Boost Power Stages in Switch Mode Power Supplies*

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

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All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM36272YFFR	ACTIVE	DSBGA	YFF	24	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	LM36272	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

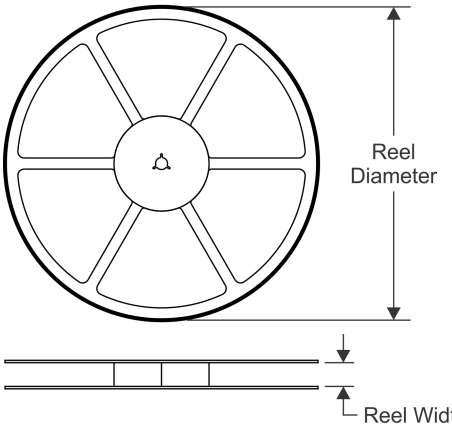
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

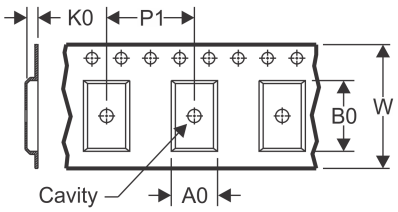
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

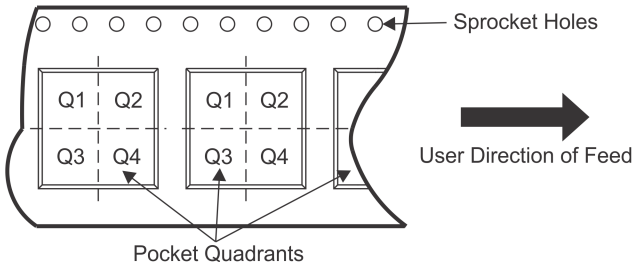


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

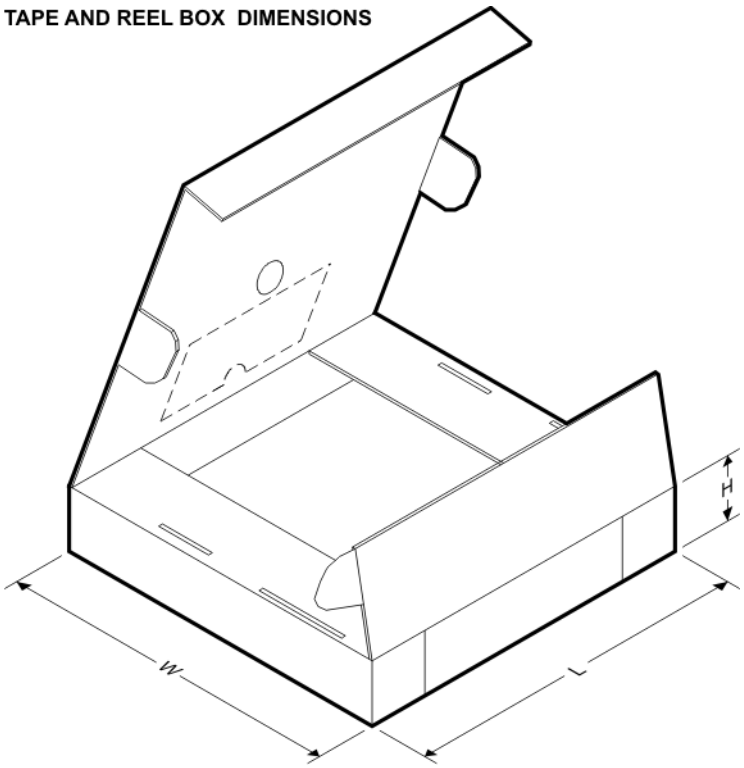
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM36272YFFR	DSBGA	YFF	24	3000	180.0	8.4	1.72	2.51	0.69	4.0	8.0	Q1

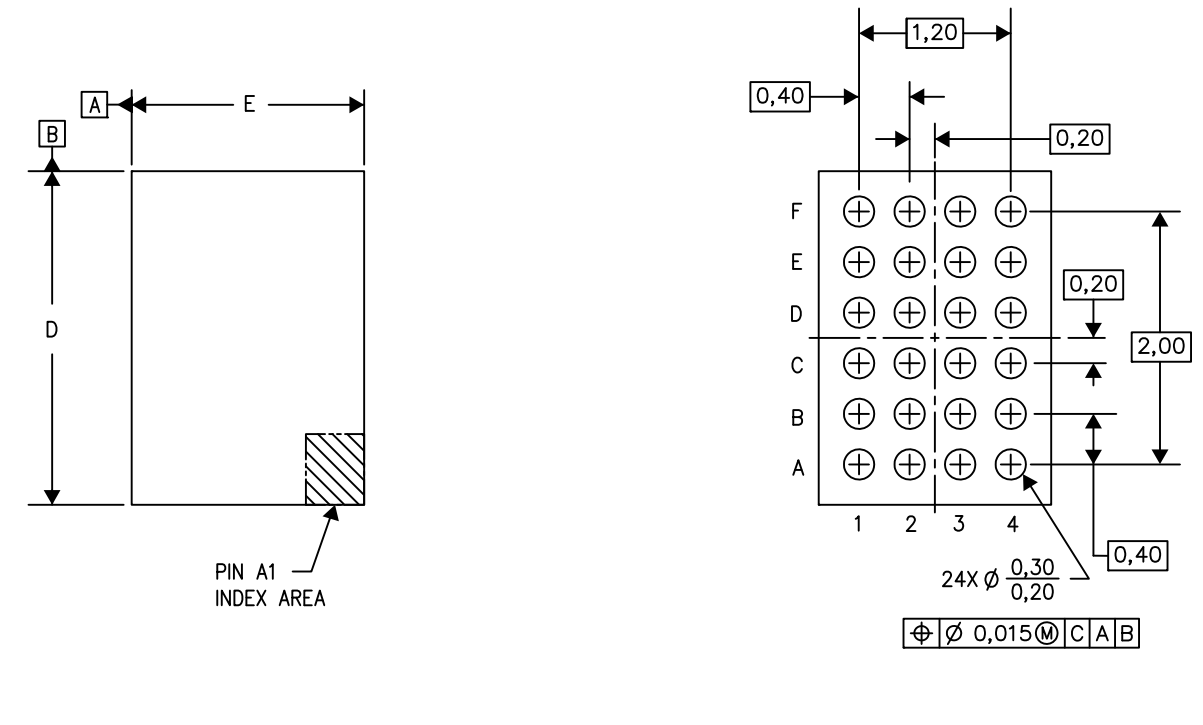
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM36272YFFR	DSBGA	YFF	24	3000	182.0	182.0	20.0

YFF (R–XBGA–N24) DIE–SIZE BALL GRID ARRAY



D: Max = 2.44 mm, Min = 2.38 mm

E: Max = 1.671 mm, Min = 1.61 mm

4207625–29/AO 12/13

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

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