DS26C32AT/DS26C32AM Quad Differential Line Receiver

Check for Samples: DS26C32AM, DS26C32AT

FEATURES

- **CMOS Design for Low Power**
- **±0.2V Sensitivity over Input Common Mode Voltage Range**
- **Typical Propagation Delays: 19 ns**
- **Typical Input hysteresis: 60 mV**
- **Inputs Won't Load Line When V_{CC} = 0V**
- **Meets the Requirements of EIA Standard RS-422**
- **TRI-STATE Outputs for Connection to System Buses**
- **Available in Surface Mount**
- **Mil-Std-883C Compliant**

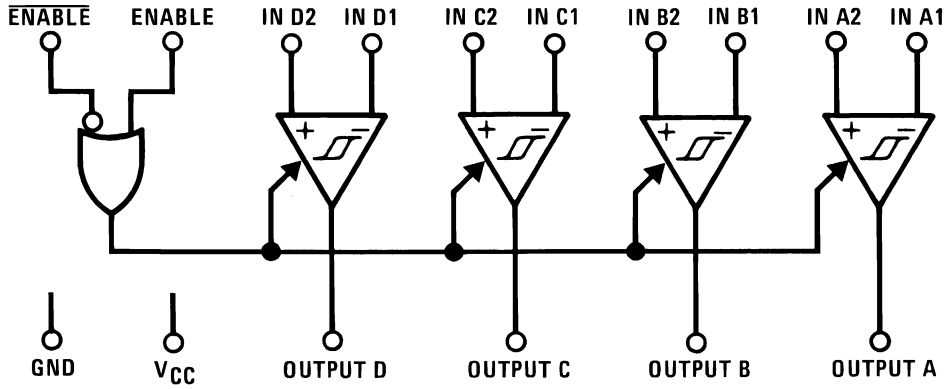
DESCRIPTION

The DS26C32A is a quad differential line receiver designed to meet the RS-422, RS-423, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission, while retaining the low power characteristics of CMOS.

The DS26C32A has an input sensitivity of 200 mV over the common mode input voltage range of ±7V. The DS26C32A features internal pull-up and pull-down resistors which prevent output oscillation on unused channels.

The DS26C32A provides an enable and disable function common to all four receivers. It also features TRI-STATE outputs with 6 mA source and sink capability. This product is pin compatible with the DS26LS32A and the AM26LS32.

Logic Diagram



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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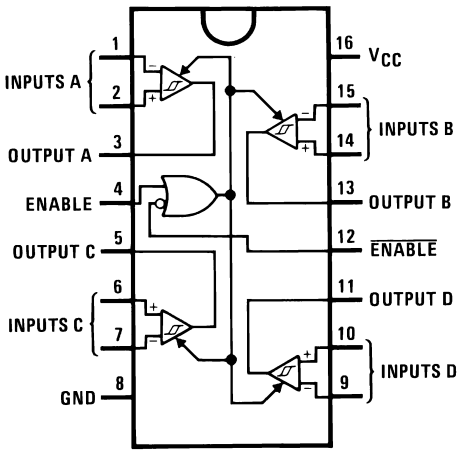
Connection Diagrams

Top View



For Complete Military Product Specifications, refer to the appropriate SMD or MDS.

Figure 1. PDIP Package
See Package Number D0016A or NFG0016E
See Package Number NAJ0020A, NFE0016A or NAD0016A

Top View

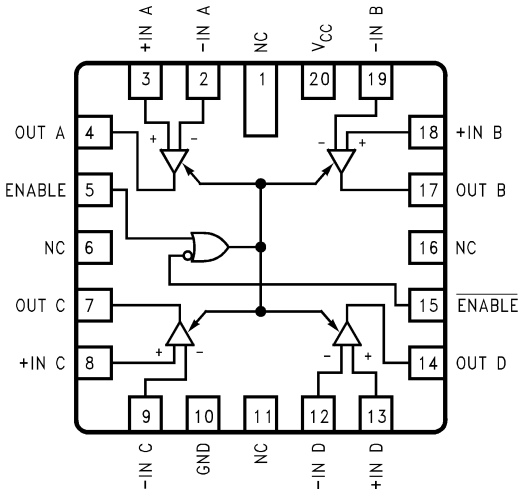


Figure 2. 20-Lead Ceramic Leadless Chip Carrier
LCCC Package

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings(1)(2)(3)

Supply Voltage (V_{CC})	7V
Common Mode Range (V_{CM})	±14V
Differential Input Voltage (V_{DIFF})	±14V
Enable Input Voltage (V_{IN})	7V
Storage Temperature Range (T_{STG})	−65°C to +150°C
Lead Temperature (Soldering 4 sec.)	260°C
Maximum Power Dissipation at 25°C (4)	
Ceramic NFE0016A Package	2308 mW
Plastic NFG0016E Package	1645 mW
SOIC D0016A Package	1190 mW
Ceramic NAJ0020A Package	2108 mW
Ceramic NAD0016A Package	1215 mW
Maximum Current Per Output	±25 mA
This device does not meet 2000V ESD rating.(5)	

(1) Absolute Maximum Ratings are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.
(2) Unless otherwise specified, all voltages are referenced to ground.
(3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications
(4) Ratings apply to ambient temperature at 25°C. Above this temperature derate N Package 13.16 mW/°C, J Package 15.38 mW/°C, M Package 9.52 mW/°C, E Package 12.04 mW/°C, and W package 6.94 mW/°C.
(5) ESD Rating: HBM (1.5 kΩ, 100 pF) Inputs ≥2000V All other pins ≥1000V EIAJ (0Ω, 200 pF) ≥350V

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.50	5.50	V
Operating Temperature Range (T_A)			
DS26C32AT	−40	+85	°C
DS26C32AM	−55	+125	°C
Enable Input Rise or Fall Times		500	ns

DC Electrical Characteristics

V_{CC} = 5V ±10% (unless otherwise specified)(1)

Parameter		Test Conditions		Min	Typ	Max	Units
V_{TH}	Minimum Differential Input Voltage	$V_{OUT} = V_{OH}$ or V_{OL} $-7V < V_{CM} < +7V$		−200	35	+200	mV
R_{IN}	Input Resistance	V_{IN} = −7V, +7V (Other Input = GND)	DS26C32AT	5.0	6.8	10	kΩ
			DS26C32AM	4.5	6.8	11	kΩ
I_{IN}	Input Current	V_{IN} = +10V, Other Input = GND	DS26C32AT		+1.1	+1.5	mA
			DS26C32AM		+1.1	+1.8	mA
		V_{IN} = −10V, Other Input = GND	DS26C32AT		−2.0	−2.5	mA
			DS26C32AM		−2.0	−2.7	mA
V_{OH}	Minimum High Level Output Voltage	V_{CC} = Min, V_{DIFF} = +1V		3.8	4.2		V
		I_{OUT} = −6.0 mA					
V_{OL}	Maximum Low Level Output Voltage	V_{CC} = Max, V_{DIFF} = −1V			0.2	0.3	V
		I_{OUT} = 6.0 mA					
V_{IH}	Minimum Enable High Input Level Voltage			2.0			V
V_{IL}	Maximum Enable Low Input Level Voltage					0.8	V

(1) Absolute Maximum Ratings are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

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DC Electrical Characteristics (continued)

V_{CC} = 5V ±10% (unless otherwise specified)(1)

Parameter		Test Conditions		Min	Typ	Max	Units
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT} = V_{CC} or GND, $\overline{ENABLE}$ = V_{IL}, $\overline{ENABLE}$ = V_{IH}			±0.5	±5.0	µA
I_I	Maximum Enable Input Current	V_{IN} = V_{CC} or GND				±1.0	µA
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max,	DS26C32AT		16	23	mA
		V_{DIF} = +1V	DS26C32AM		16	25	mA
V_{HYST}	Input Hysteresis	V_{CM} = 0V			60		mV

AC Electrical Characteristics

V_{CC} = 5V ±10% (1)

Parameter		Test Conditions	Min	Typ	Max		Units
					DS26C32AT	DS26C32AM	
t_{PLH}, t_{PHL}	Propagation Delay Input to Output	C_L = 50 pF V_{DIFF} = 2.5V V_{CM} = 0V	10	19	30	35	ns
t_{RISE}, t_{FALL}	Output Rise and Fall Times	C_L = 50 pF V_{DIFF} = 2.5V V_{CM} = 0V		4	9	9	ns
t_{PLZ}, t_{PHZ}	Propagation Delay ENABLE to Output	C_L = 50 pF R_L = 1000Ω V_{DIFF} = 2.5V		13	22	29	ns
t_{PZL}, t_{PZH}	Propagation Delay ENABLE to Output	C_L = 50 pF R_L = 1000Ω V_{DIFF} = 2.5V		13	23	29	ns

(1) Unless otherwise specified, Min/Max limits apply over recommended operating conditions. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Comparison Table of Switching Characteristics into "LS-Type" Load

(Figure 6, Figure 7, and Figure 8) (1)

Parameter		Test Conditions	DS26C32A	DS26LS32A	Units
			Typ	Typ	
t_{PLH}	Input to Output	C_L = 15 pF	17	23	ns
t_{PHL}			19	23	ns
t_{LZ}	ENABLE to Output	C_L = 5 pF	13	15	ns
t_{HZ}			12	20	ns
t_{ZL}	ENABLE to Output	C_L = 15 pF	13	14	ns
t_{ZH}			13	15	ns

(1) This table is provided for comparison purposes only. The values in this table for the DS26C32A reflect the performance of the device, but are not tested.

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TEST AND SWITCHING WAVEFORMS

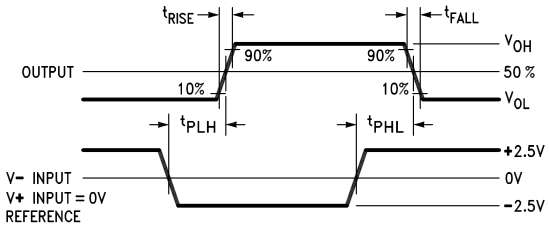
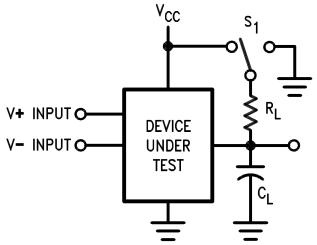


Figure 3. Propagation Delay



C_L includes load and test jig capacitance.
$S_1 = V_{CC}$ for t_{PZL}, and t_{PLZ} measurements.
S_1 = Gnd for t_{PZH} and t_{PHZ} measurements.

Figure 4. Test Circuit for TRI-STATE Output Tests

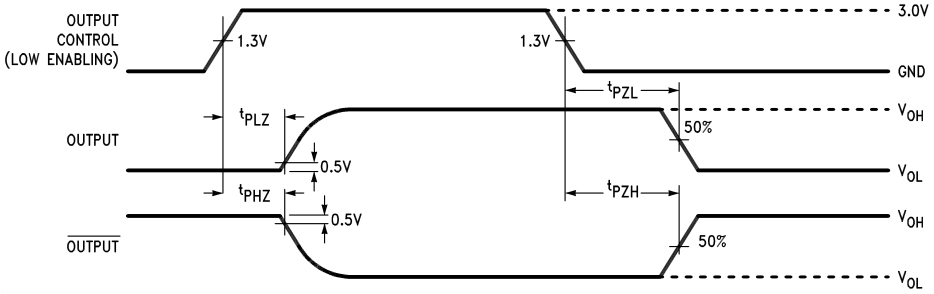


Figure 5. TRI-STATE Output Enable and Disable Waveforms

AC Test Circuit and Switching Time Waveforms

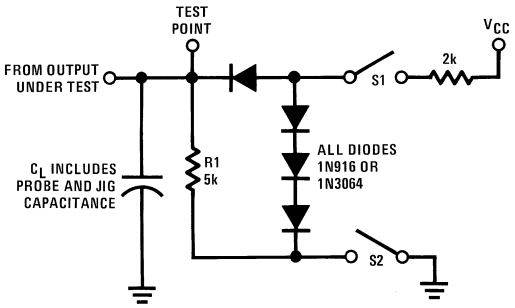


Figure 6. Load Test Circuit for TRI-STATE Outputs for "LS-Type" Load

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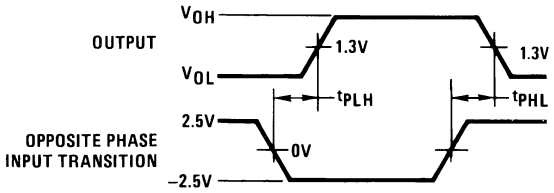
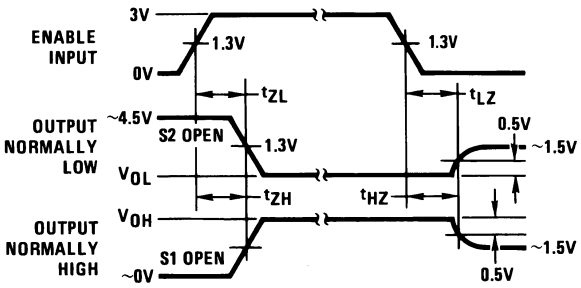


Figure 7. Propagation Delay for "LS-Type" Load



(1) Diagram shown for $\overline{\text{ENABLE}}$ low.

(2) S1 and S2 of load circuit are closed except where shown.

(3) Pulse generator for all pulses: Rate ≤ 1.0 MHz; Z_O = 50Ω; t_r ≤ 15 ns; t_f ≤ 6.0 ns.

Figure 8. Enable and Disable Times for "LS-Type" Load

Truth Table(1)

ENABLE	$\overline{\text{ENABLE}}$	Input	Output
L	H	X	Z
All Other Combinations of Enable Inputs		$V_{ID} \geq V_{TH}$ (Max)	H
		$V_{ID} \leq V_{TH}$ (Min)	L
		Open	H

(1) Z = TRI-STATE

TYPICAL APPLICATIONS

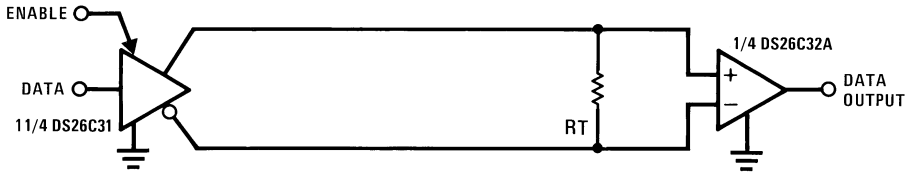


Figure 9. Two-Wire Balanced Systems, RS-422

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Typical Performance Characteristics

Differential Propagation Delay vs Temperature

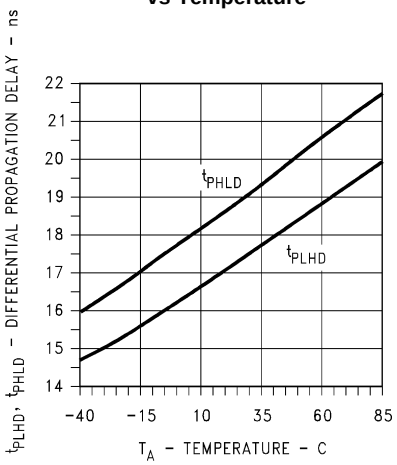

Figure 10.

Differential Propagation Delay vs Power Supply Voltage

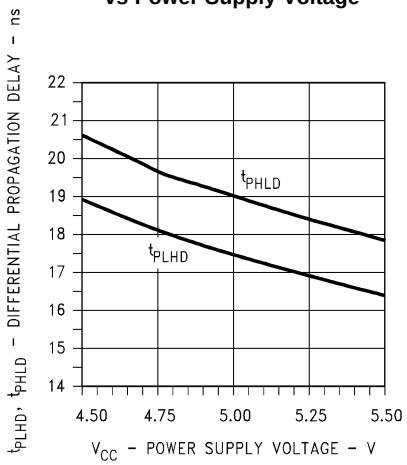

Figure 11.

Differential Skew vs Temperature

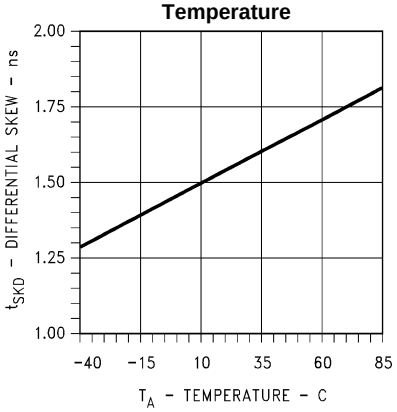

Figure 12.

Differential Skew vs Power Supply Voltage

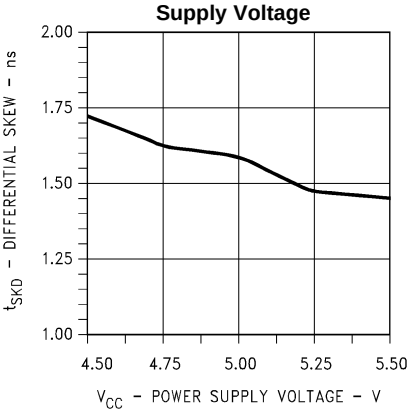

Figure 13.

Output High Voltage vs Output High Current

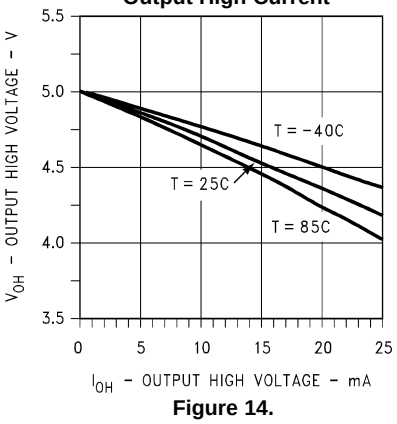

Figure 14.

Output High Voltage vs Output High Current

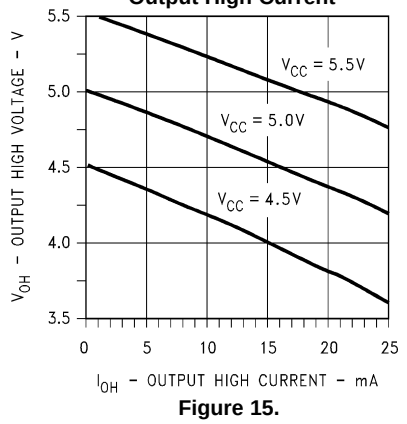

Figure 15.

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Typical Performance Characteristics (continued)

Output Low Voltage vs Output Low Current

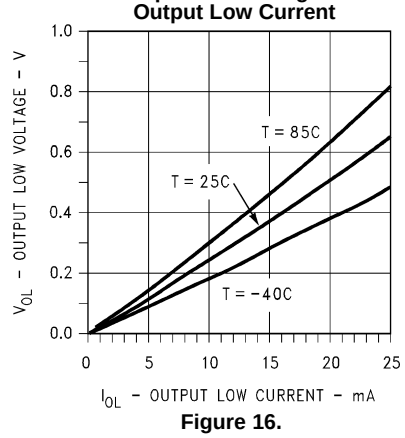

Figure 16.

Output Low Voltage vs Output Low Current

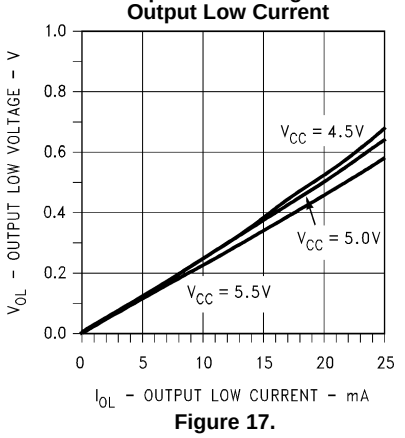

Figure 17.

Input Resistance vs Input Voltage

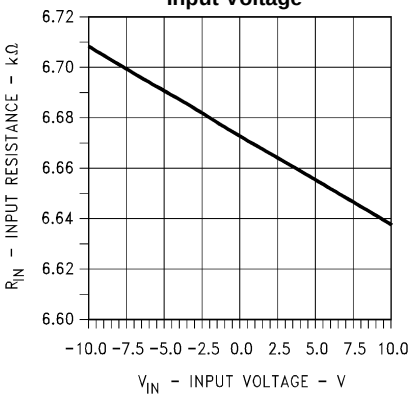

Figure 18.

Input Current vs Power Supply Voltage

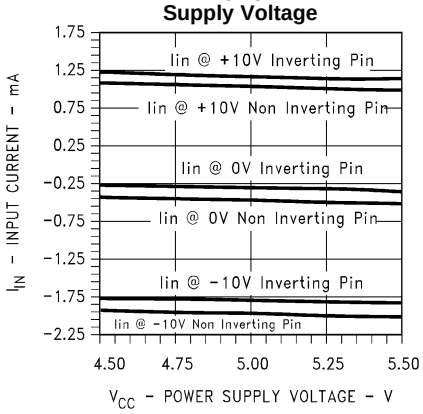

Figure 19.

Hysteresis & Differential Transition Voltage vs Temperature

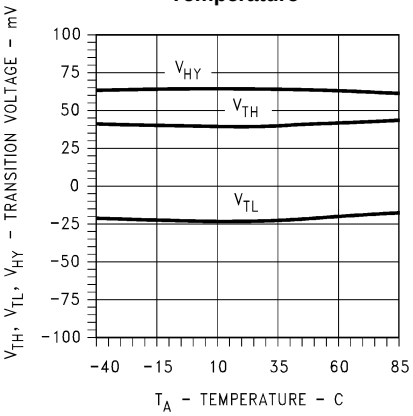

Figure 20.

Hysteresis & Differential Transition Voltage vs Power Supply Voltage

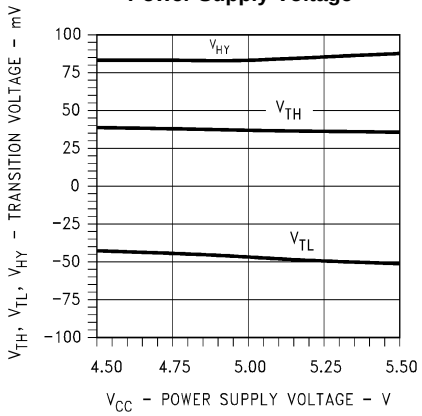

Figure 21.

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Typical Performance Characteristics (continued)

Supply Current vs Temperature

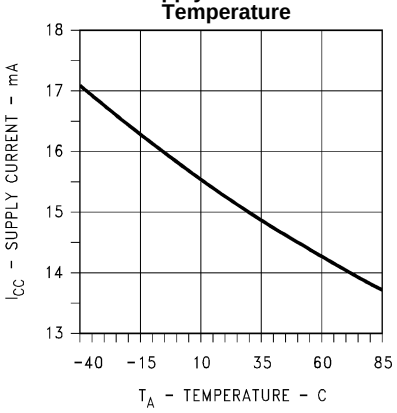

Figure 22.

Disabled Supply Current vs Power Supply Voltage

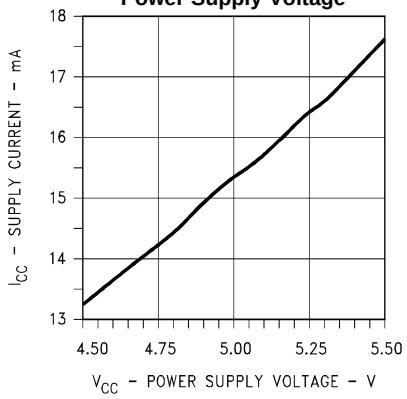

Figure 23.

Supply Current vs Data Rate

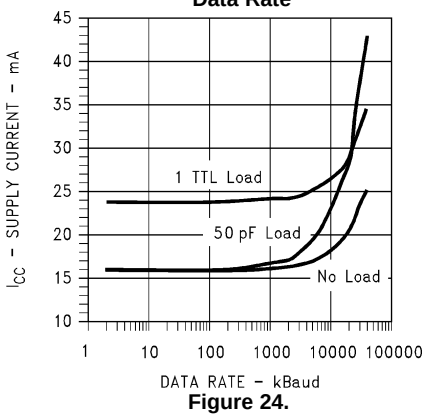

Figure 24.

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	9

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS26C32ATM	LIFEBUY	SOIC	D	16	48	TBD	Call TI	Call TI	-40 to 85	DS26C32ATM	
DS26C32ATM/NOPB	ACTIVE	SOIC	D	16	48	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS26C32ATM	Samples
DS26C32ATMX	LIFEBUY	SOIC	D	16	2500	TBD	Call TI	Call TI	-40 to 85	DS26C32ATM	
DS26C32ATMX/NOPB	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS26C32ATM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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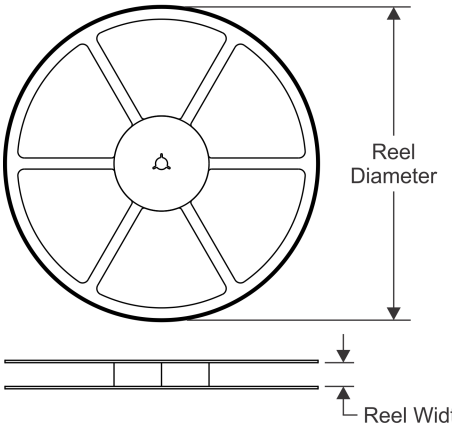
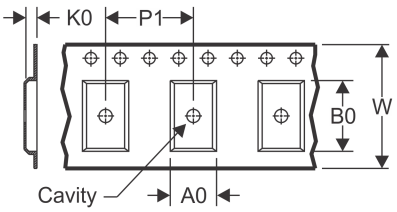
TAPE AND REEL INFORMATION

REEL DIMENSIONS

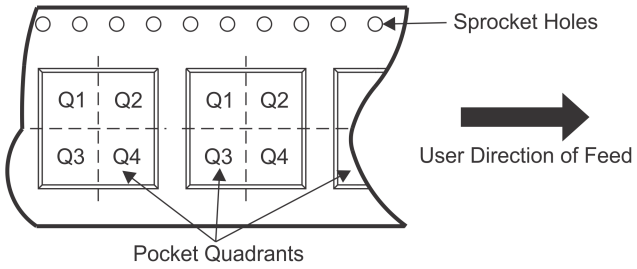


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

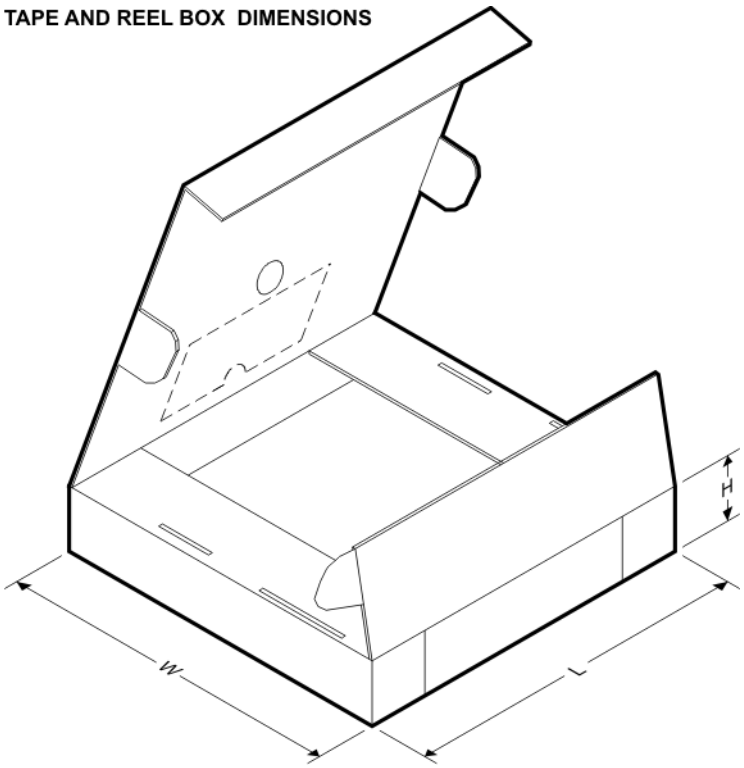
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS26C32ATMX	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1
DS26C32ATMX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1

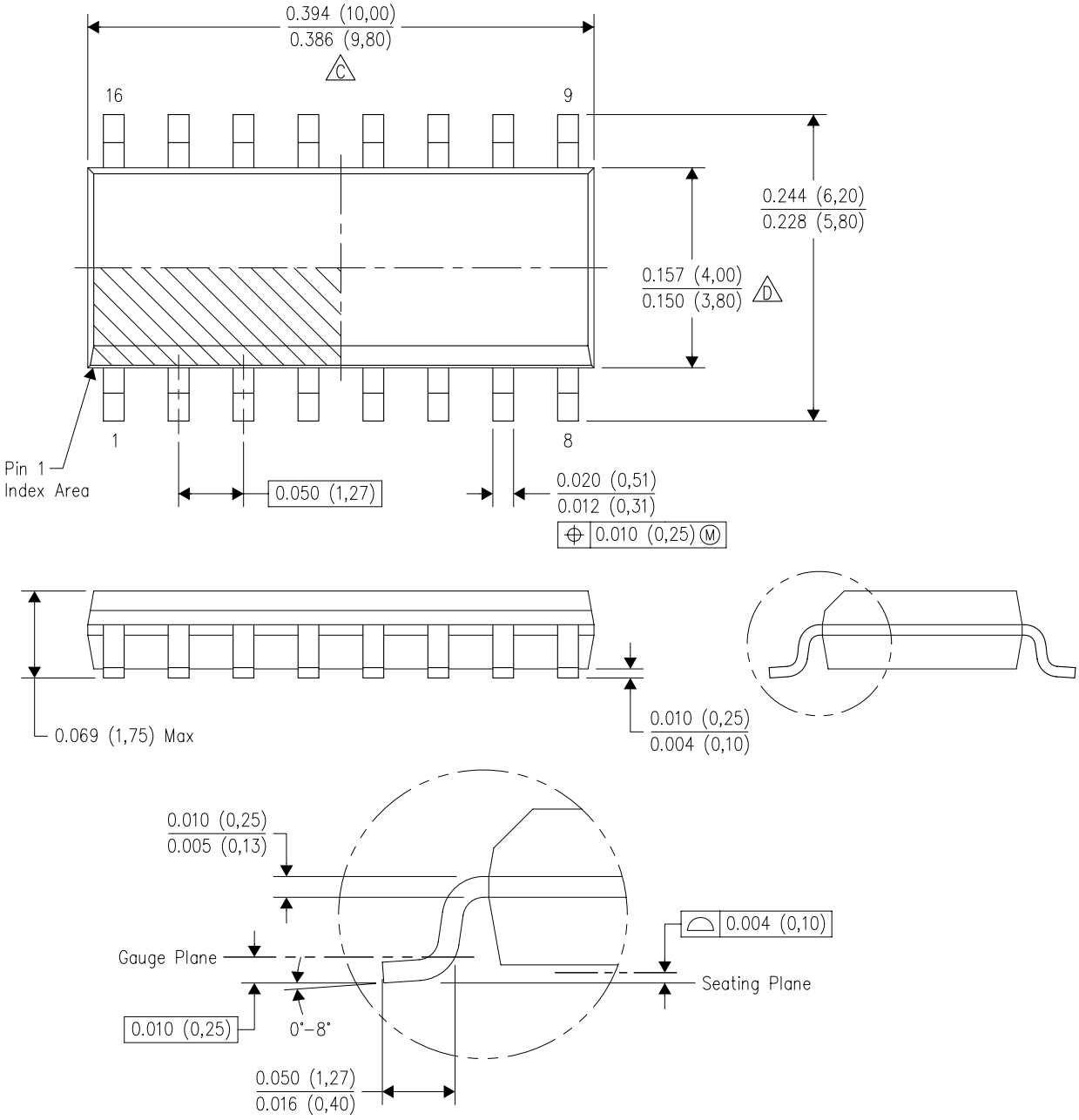
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS26C32ATMX	SOIC	D	16	2500	367.0	367.0	35.0
DS26C32ATMX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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