# LED Driver with Average-Mode Constant Current Control

Halogen Free

## General Description

The FP7176 is an average current mode control LED driver IC operating in a constant off-time mode. FP7176 does not produce a peak-to-average error, and therefore greatly improves accuracy, line and load regulation of the LED current without any need for loop compensation or high-side current sensing. The output LED current accuracy is ±2%.

The FP7176 can be powered from an 8.0 - 450V supply. A PWM dimming input is provided that accepts an external control TTL compatible signal. The output current can be programmed by an internal 277mV reference, or controlled externally through a 0 - 1.5V dimming input.

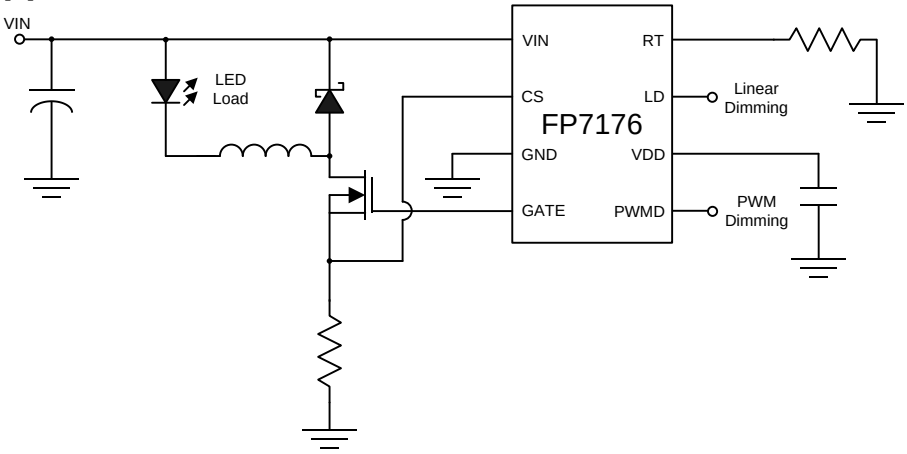
## Features

- Fast average current control
- Internal 8 to 450V linear regulator
- Programmable constant off-time switching
- Linear and PWM dimming capability
- Output short circuit protection with skip mode
- Requires few external components for operation

## Applications

- DC/DC or AC/DC LED driver applications
- LED street lighting
- Back lighting of flat panel displays
- General purpose constant current source
- Signage and decorative LED lighting
- Chargers

## Typical Application Circuit

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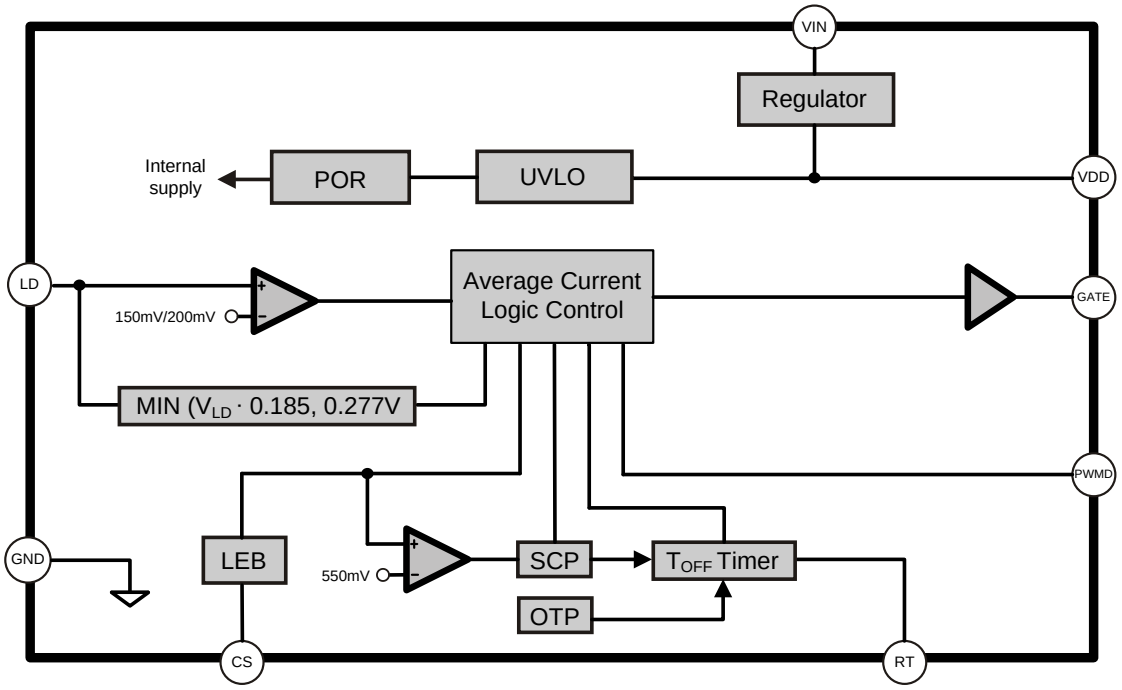
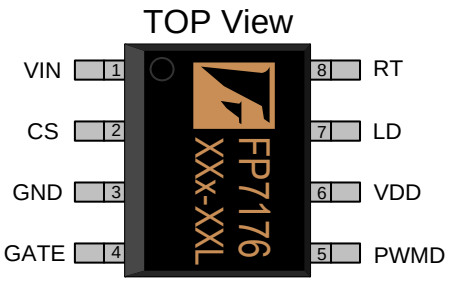
## Function Block Diagram




## Pin Descriptions

### SOP-8L




| Name | No. | I / O | Description |
|---|---|---|---|
| VIN | 1 | | This pin is the input of an 8 - 450V linear regulator. |
| CS | 2 | I | This pin is the current sense pin used to sense the FET current by means of an external sense resistor. |
| GND | 3 | P | Ground return for all internal circuitry. |
| GATE | 4 | O | This pin is the output GATE driver for an external N-channel power MOSFET. |
| PWMD | 5 | I | This is the PWM dimming input of the IC. |
| VDD | 6 | I | This is the power supply pin for all internal circuits. |
| LD | 7 | I | This pin is the linear dimming input of the IC. |
| RT | 8 | I | A resistor connected between this pin and GND programs the GATE off-time. |

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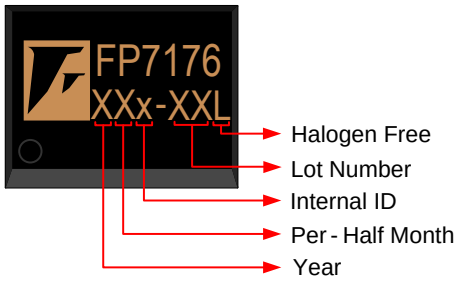
# Marking Information




**Halogen Free**: Halogen free product indicator

**Lot Number**: Wafer lot number's last two digits

For Example → Lot : 123456 → XXx-56L

**Internal ID**: Internal Identification Code

**Per-Half Month**: Production period indicator in half month time unit

For Example : A → First Half Month of January
B → Second Half Month of January
C → First Half Month of February
D → Second Half Month of February

**Year**: Production year's last digit

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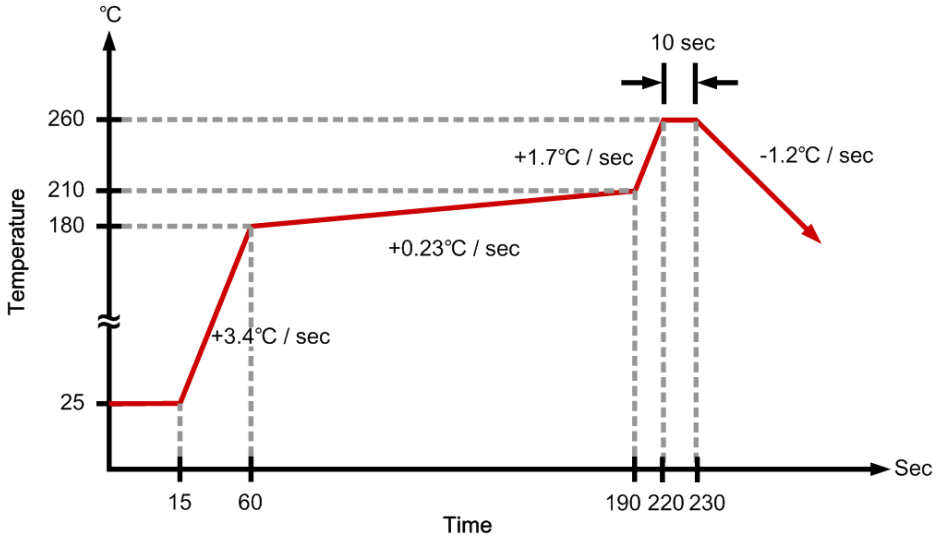
## Ordering Information

| Part Number | Operating Temperature | Package | MOQ | Description |
|---|---|---|---|---|
| FP7176DR-G1 | -25°C ~ +85°C | SOP-8L | 2500 EA | Tape & Reel |

## Absolute Maximum Ratings

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Power Supply Voltage | $V_{IN}$ | $V_{IN}$ to GND | | | 470 | V |
| | $V_{DD}$ | $V_{DD}$ to GND | | | 8 | V |
| CS, LD, PWMD, GATE, RT | | | -0.3 | | $V_{DD}$-0.3V | V |
| Allowable Power Dissipation | $P_D$ | SOP-8L $T_A \leqq +25°C$ | | | 630 | mW |
| Junction to Ambient Thermal Resistance | $\theta_{JA}$ | | | 128 | | °C / W |
| Operating Temperature | | | -25 | | +125 | °C |
| Storage Temperature | $T_S$ | SOP-8L | -40 | | +150 | °C |
| SOP-8L Lead Temperature | | (soldering, 10 sec) | | | +260 | °C |

## IR Re-flow Soldering Curve

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## Recommended Operating Conditions

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{IN}$ | | 8 | | 450 | V |
| Operating Temperature | | | -25 | | 125 | °C |

## DC Electrical Characteristics ($V_{IN}$=12V,$T_A$ = 25°C, unless otherwise noted)

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Internal Regulator** | | | | | | |
| Internally regulated voltage | $V_{DD}$ | VIN = 8V, $I_{DD(ext)}$= 0, 500pF at GATE; RT = 226kΩ, PWMD = VDD | 7.25 | 7.5 | 7.75 | V |
| Line regulation of VDD | $\Delta V_{DD,line}$ | VIN = 8 – 450V, $I_{DD(ext)}$=0, 500pF at GATE; RT = 226kΩ, PWMD = VDD | 0 | - | 1.0 | V |
| Load regulation of $V_{DD}$ | $\Delta V_{DD,load}$ | $I_{DD(ext)}$ = 0 – 0.6mA, 500pF at GATE; RT = 226kΩ, PWMD = VDD | 0 | | 100 | mV |
| $V_{DD}$ undervoltage lockout threshold | UVLO | $V_{DD}$ rising | 5.75 | 6 | 6.25 | V |
| $V_{DD}$ undervoltage lockout hysteresis | ΔUVLO | $V_{DD}$ falling | | 500 | | mV |
| Maximum input current | $I_{IN,MAX}$ | VIN = 8V, $I_{DD(ext)}$= 0, 500pF at GATE; RT = 226kΩ, PWMD = VDD | | 0.8 | | mA |
| **PWM Dimming** | | | | | | |
| Pin PWMD input low voltage | $V_{EN(lo)}$ | $V_{IN}$ = 8 - 450V | | | 0.9 | V |
| Pin PWMD input high voltage | $V_{EN(hi)}$ | $V_{IN}$ = 8 - 450V | 1.8 | | | V |
| **Average Current Sense Logic** | | | | | | |
| Current sense reference voltage | $V_{CS}$ | | 271 | | 283 | mV |
| LD-to-CS voltage ratio | $A_{V(LD)}$ | | 0.182 | | 0.188 | |
| LD-to-CS voltage offset | $AV_{LD\ (OFFSET)}$ | Offset = $V_{CS} – A_{V(LD)} \cdot V_{LD}$ $V_{LD}$=1.2V | 0 | | 15 | mV |
| CS threshold temp regulation | | | | | 5 | mV |
| LD input voltage, shutdown | $V_{LD(OFF)}$ | | | 150 | | mV |
| LD input voltage, enable | $\Delta V_{LD(OFF)}$ | | | 200 | | mV |
| Current sense blanking interval | $T_{BLANK}$ | | 150 | | 320 | ns |
| Minimum on-time | $T_{ON(min)}$ | CS=$V_{CS}$ + 30mV | | | 1000 | ns |
| **Short Circuit Protection** | | | | | | |
| Hiccup threshold voltage | $V_{CS}$ | | 495 | 550 | 605 | mV |
| Current limit delay CS - GATE | $T_{DELAY}$ | CS=$V_{CS}$ + 30mV | | | 150 | ns |
| Short circuit hiccup time | $T_{HICCUP}$ | | 450 | 550 | 650 | us |
| Minimum on-time (short circuit) | $T_{ON(min)}$ | CS=$V_{DD}$ | | | 600 | ns |

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| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **$T_{OFF}$ Timer** | | | | | | |
| Off time | $T_{OFF}$ | $R_T$ = 1.00MΩ | 32 | 40 | 48 | us |
| | | $R_T$ = 226kΩ | 8 | 10 | 12 | |
| **GATE Driver** | | | | | | |
| GATE sourcing current | $I_{SOURCE}$ | $V_{GATE}$ = 0V, $V_{DD}$ = 7.5V | 165 | | | mA |
| GATE sinking current | $I_{SINK}$ | $V_{GATE}$ = $V_{DD}$, $V_{DD}$ = 7.5V | 165 | | | mA |
| GATE output rise time | $t_{RISE}$ | $C_{GATE}$ = 500pF, $V_{DD}$ = 7.5V | | 30 | 50 | ns |
| GATE output fall time | $t_{FALL}$ | $C_{GATE}$ = 500pF, $V_{DD}$ = 7.5V | | 30 | 50 | ns |

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# Function Description

### Input Voltage Regulator

The FP7176 can be powered directly from its VIN pin and can work from 8.5 - 450VDC at its VIN pin. When a voltage is applied at the VIN pin, the FP7176 maintains a constant 7.5V at the VDD pin. This voltage is used to power the IC and any external resistor dividers needed to control the IC. The VDD pin must be bypassed by a low ESR capacitor to provide a low impedance path for the high frequency current of the output GATE driver.

The FP7176 can also be operated by supplying a voltage at the VDD pin greater than the internally regulated voltage. This will turn off the internal linear regulator of the IC and the FP7176 will operate directly off the voltage supplied at the VDD pin. Please note that this external voltage at the VDD pin should not exceed 8.5V.

Although the VIN pin of the FP7176 is rated up to 450V, the actual maximum voltage that can be applied is limited by the power dissipation in the IC. For example, if an 8-pin SOIC (junction to ambient thermal resistance Rθ,j-a = 128°C/ W) FP7176 draws about $I_{IN}$ = 2.0mA from the VIN pin, and has a maximum allowable temperature rise of the junction temperature limited to about ΔT = 100°C, the maximum voltage at the VIN pin would be:

$$V_{IN(MAX)} = \frac{\Delta T}{R_{\theta,j\ a}} \times \frac{1}{I_{in}} = \frac{100^{o}C}{128^{o}C/W} \times \frac{1}{2mA} = 390V$$

In these cases, to operate the FP7176 from higher input voltages, a Zener diode can be added in series with the VIN pin to divert some of the power loss from the FP7176 to the Zener diode. In the above example, using a 100V Zener diode will allow the circuit to easily work up to 490V.The input current drawn from the VIN pin is represented by the following equation:

$$I_{IN} \approx 0.5mA + Q_G \times f_S$$

In the above equation, $f_S$ is the switching frequency and QG is the GATE charge of the external FET (which can be obtained from the datasheet of the FET).

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## OFF Timer

The timing resistor connected to RT determines the off-time of the gate driver, and it must be wired to GND. The equation governing the off-time of the GATE output is given by:

$$T_{OFF}(\mu s)=\frac{R_T(k\Omega)}{25}+0.3$$

within the range of $30k\Omega \leqq RT(k\Omega) \leqq 1M\Omega$

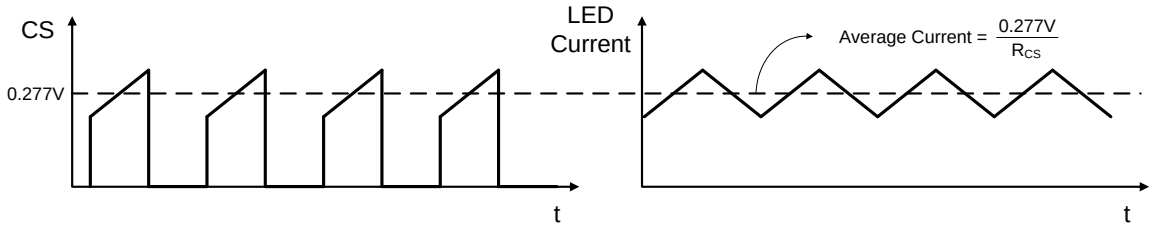
## Average Current Control

The LED current is detected using a sense resistor at the CS pin. The feedback operates in a fast open-loop mode. No compensation is required. When the voltage at the LD input $V_{LD} \geq 1.5V$, output current is programmed simply as:

$$I_{LED}(A)=\frac{0.277V}{R_{CS}(\Omega)}$$

Otherwise:

$$I_{LED}(A)=\frac{V_{LD}(V)\times 0.185}{R_{CS}(\Omega)}$$




The above equations are only valid for continuous conduction of the output inductor. It is a good practice to design the inductor such that the switching ripple current in it is 30~40% of its average peak-to-peak, full load, DC current. Hence, the recommended inductance can be calculated as:

$$L=\frac{V_{LED(MAX)}\times T_{OFF}}{0.4\times I_{LED}}$$

## GATE Output

The GATE output of the FP7176 is used to drive an external MOSFET. It is recommended that the gate charge QG of the external MOSFET be less than 25nC for switching frequencies ≤100kHz and less than 15nC for switching frequencies >100kHz.

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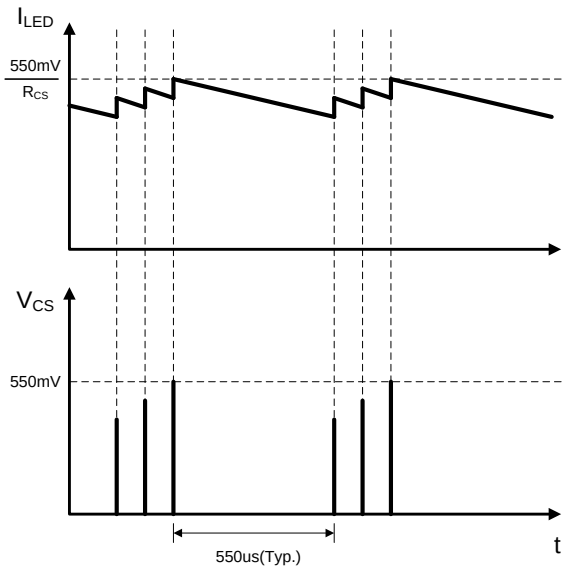
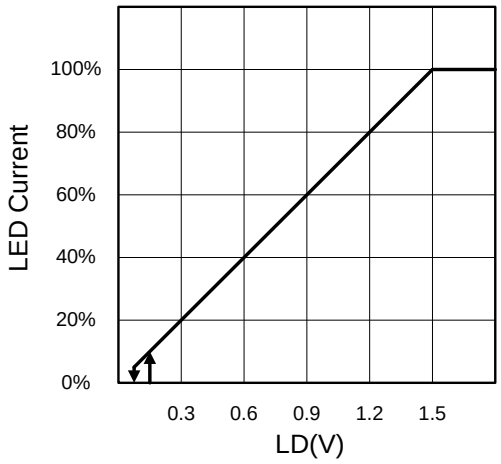
## Output Short Circuit Protection

The short circuit protection comparator trips when the voltage at CS exceeds 0.55V. When this occurs, the GATE off-time $T_{HICCUP}$ = 550μs is generated to prevent stair-casing of the inductor current and potentially its saturation due to insufficient output voltage.




## Linear Dimming

When the voltage at LD falls below 1.5V, the internal 277mV reference to the constant-current feedback becomes overridden by $V_{LD}$ • 0.185. As long as the current in the inductor remains continuous, the LED current is given by the equation above. However, when $V_{LD}$ falls below 150mV, the GATE output becomes disabled. The GATE signal recovers, when $V_{LD}$ exceeds 200mV. This is required in some applications to be able to shut the LED lamp off with the same signal input that controls the brightness.

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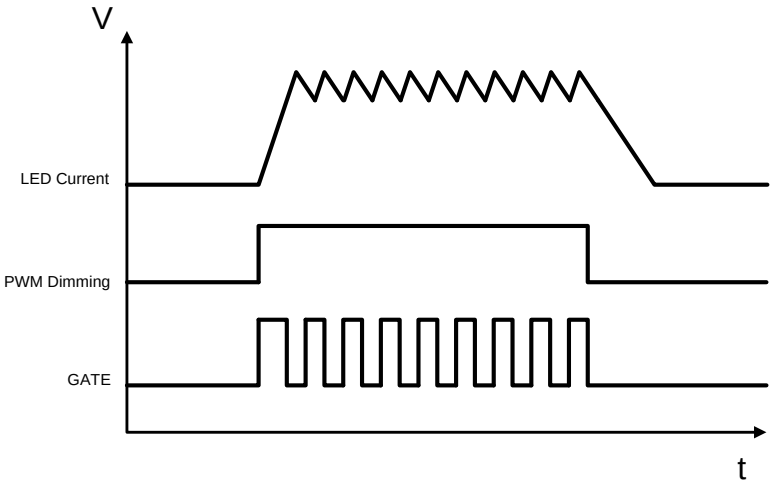
## PWM Dimming

Due to the fast open-loop response of the average-current control loop of the FP7176, its PWM dimming performance nearly matches that of the FP7171.




The rising and falling edges are limited by the current slew rate in the inductor. The first switching cycle is terminated upon reaching the 277mV (VLD • 0.185) level at CS. The circuit is further reaching its steady-state within 1 switching cycles regardless of the switching frequency.

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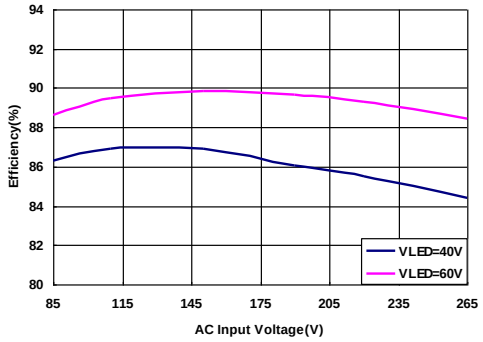
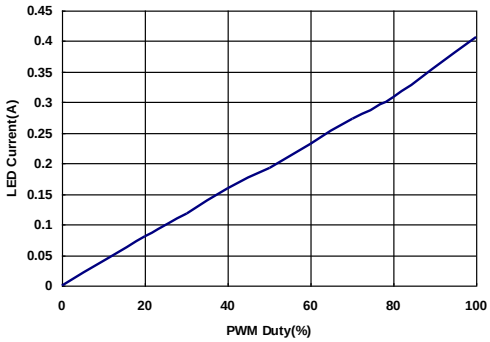
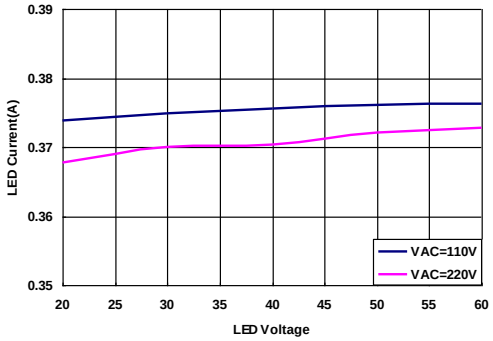
Efficiency



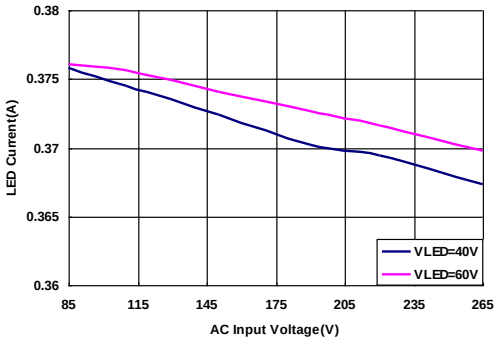

PWM Duty VS LED Current



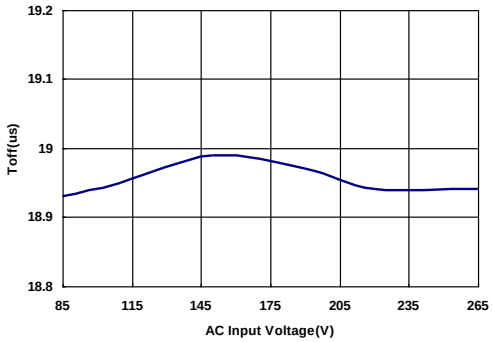

Load Regulation



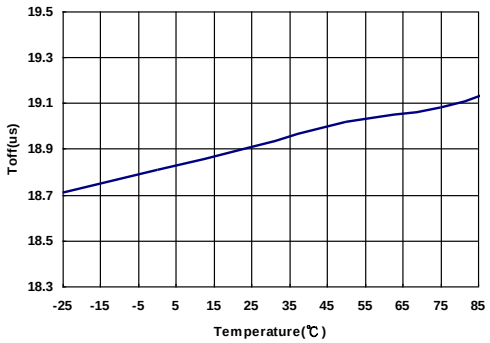

Line Regulation




AC Input Voltage VS Toff




Temperature VS Toff

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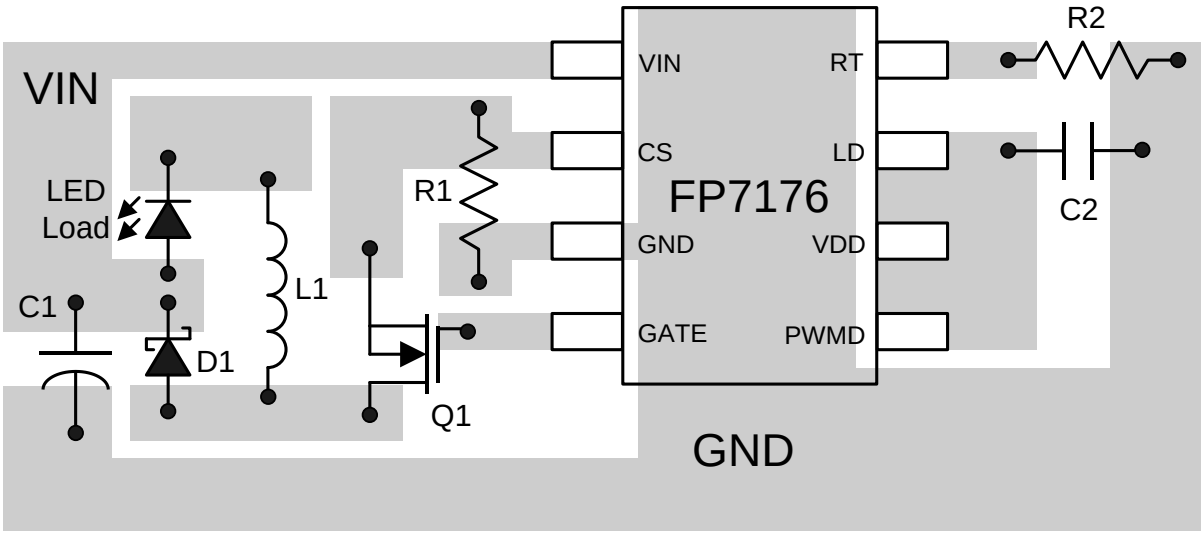


**Suggested Layout**

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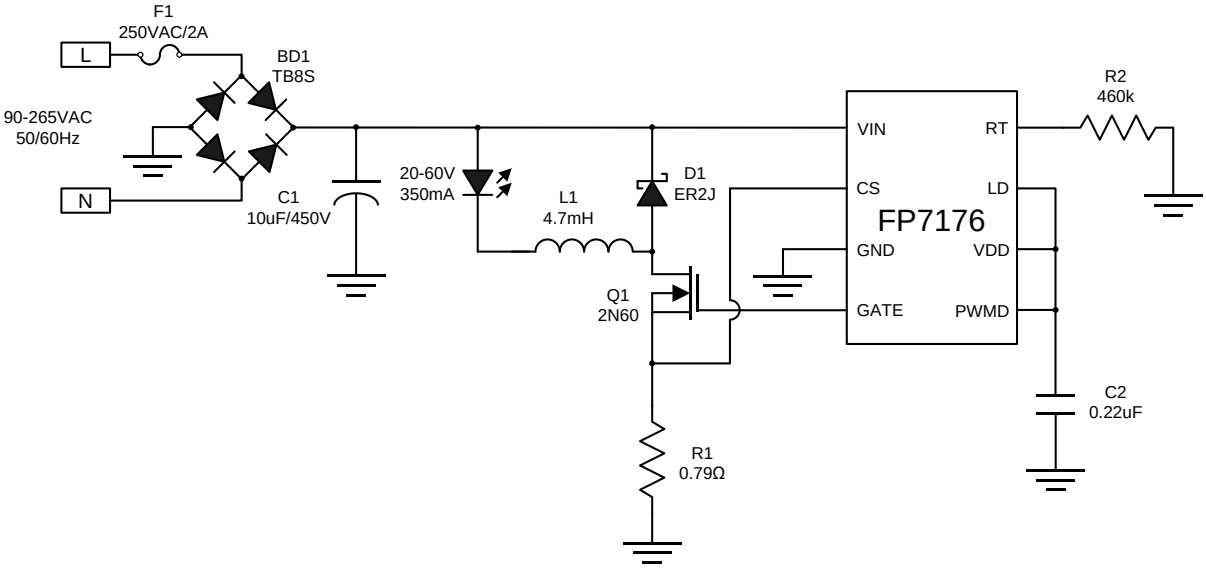
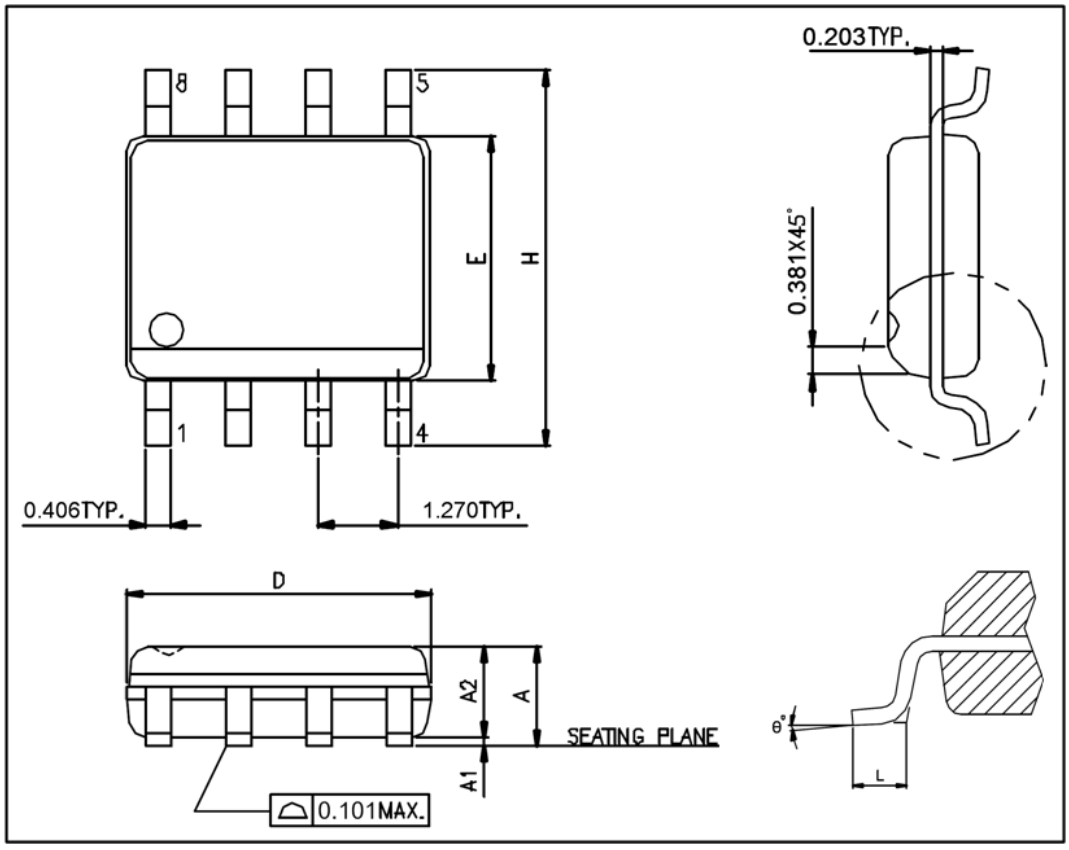
## Typical Application Circuit



# Package Outline

## SOP-8L




**UNIT: mm**

| Symbols | Min. (mm) | Max. (mm) |
|---|---|---|
| A | 1.346 | 1.752 |
| A1 | 0.101 | 0.254 |
| A2 | | 1.498 |
| D | 4.800 | 4.978 |
| E | 3.810 | 3.987 |
| H | 5.791 | 6.197 |
| L | 0.406 | 1.270 |
| θ° | 0° | 8° |

**Note:**

1. Package dimensions are in compliance with JEDEC Outline: MS-012 AA.
2. Dimension “D” does not include molding flash, protrusions or gate burrs.
3. Dimension “E” does not include inter-lead flash, or protrusions.

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