N-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

BV _{DSS}	R _{DS(ON)} Max	I _D T _A = +25°C
60V	2Ω @ $V_{GS} = 4V$	310mA
607	2.5Ω @ $V_{GS} = 2.5V$	295mA

Description

This new generation MOSFET has been designed to minimize the onstate resistance (R_{DS(ON)}) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

- **DC-DC Converters**
- **Power Management Functions**
- Battery Operated Systems and Solid-State Relays
- Drivers: Relays, Solenoids, Lamps, Hammers, Displays, Memories, Transistors, etc.

Features and Benefits

- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- **ESD Protected**
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- Qualified to AEC-Q101 Standards for High Reliability

Mechanical Data

- Case: X1-DFN1212-3
- Case Material: Molded Plastic. UL Flammability Classification
- Moisture Sensitivity: Level 1 per J-STD-020

Pin-Out Top View

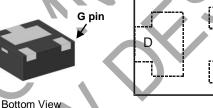
- Terminals: NiPdAu over Copper leadframe. Solderable per MIL-STD-202, Method 208 @4)
- Terminal Connections: See Diagram
- Weight: 0.005 grams (Approximate)

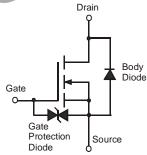




Top View







Equivalent Circuit

Ordering Information (Note 4)

Part Number	Compliance	Case	Packaging
DMN62D0LFD-7	Standard	X1-DFN1212-3	3,000/Tape & Reel
DMN62D0LFD-13	Standard	X1-DFN1212-3	10,000/Tape & Reel

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
- 2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information

K63

K63 = Product Type Marking Code YM = Date Code Marking Y = Year (ex: E = 2017)M = Month (ex: 9 = September)

Date Code Key

Year	2007	2008	2009	2010	2011	20	12	2013	2014	2015	2016	2017
Code	U	V	W	X	Υ	Z	7	Α	В	С	D	E
Month	Jan	Feb	Mar	Apr	May	Jun	Ju	ıl Au	g Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	0	N	D



NOT RECOMMENDED FOR NEW DESIGN **USE DMN62D1LFD**

DMN62D0LFD

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit	
Drain-Source Voltage		V _{DSS}	60	V
Gate-Source Voltage		V _{GSS}	±20	V
Continuous Drain Current (Note 5) V _{GS} = 4.0V	I _D	310 260	mA	
Pulsed Drain Current (Note 6) (10µs Pulse, Duty Cycle = 1%)	I _{DM}	1.0	Α	

Thermal Characteristics

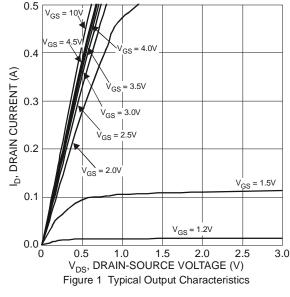
Characteristic	Symbol	Max	Unit
Power Dissipation (Note 5)	P_{D}	0.48	W
Thermal Resistance, Junction to Ambient @T _A = +25°C (Note 5)	$R_{ heta JA}$	265	°C/W
Operating and Storage Temperature Range	TJ, T _{STG}	-55 to +150	°C

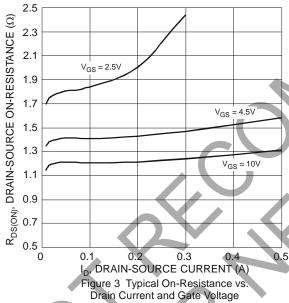
Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

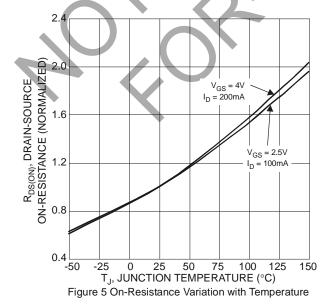
Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)		1				4
Drain-Source Breakdown Voltage	BV _{DSS}	60	—	(-)	V	V _{GS} = 0V, I _D = 250μA
Zero Gate Voltage Drain Current T _J = +25°C	I _{DSS}	74.	-	1.0	μA	V _{DS} = 60V, V _{GS} = 0V
		1-		±100	nA	$V_{GS} = \pm 5V$, $V_{DS} = 0V$
Gate-Source Leakage	I _{GSS}	_		±500	nA	$V_{GS} = \pm 10V, V_{DS} = 0V$
		_	-	±2.0	μA	$V_{GS} = \pm 15V, V_{DS} = 0V$
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	V _{GS(TH)}	0.6		1.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu A$
		-1	1.3	2		$V_{GS} = 4V, I_D = 100mA$
Static Drain-Source On-Resistance	D		1.4	2.5	Ω	$V_{GS} = 2.5V, I_D = 50mA$
Static Diain-Source On-Resistance	R _{DS} (ON)	→	1.8	3	Ω	$V_{GS} = 1.8V, I_D = 50mA$
		V -	2.4	_		$V_{GS} = 1.5V, I_D = 10mA$
Forward Transfer Admittance	Y _{fs}	_	1.8	_	S	$V_{DS} = 10V, I_D = 200mA$
Diode Forward Voltage	V _{SD}	_	0.8	1.3	V	V _{GS} = 0V, I _S = 115mA
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C _{iss}	_	31	_		051/1/ 01/
Output Capacitance	Coss	_	4.3	_	pF	$V_{DS} = 25V, V_{GS} = 0V,$ f = 1.0MHz
Reverse Transfer Capacitance	C _{rss}	_	3.0	_		1 - 1.00112
Gate Resistance	Rg	_	99	_	Ω	$V_{DS} = 0V$, $V_{GS} = 0V$, $f = 1MHz$
Total Gate Charge	Qg	_	0.5	_		V 45V V 40V
Gate-Source Charge	Q_{gs}	_	0.09	_	nC	$V_{GS} = 4.5V, V_{DS} = 10V,$ $I_{D} = 250 \text{mA}$
Gate-Drain Charge	Q _{gd}		0.07			ID = ZOUTIA
Turn-On Delay Time	t _{D(ON)}	_	2.6	_	ns	
Turn-On Rise Time	t _R	_	2.1	_	ns	$V_{GS} = 10V, V_{DS} = 30V,$
Turn-Off Delay Time	t _{D(OFF)}	_	18	_	ns	$R_L = 150\Omega$, $R_G = 25\Omega$, $I_D = 200$ mA
Turn-Off Fall Time	t _F	_	8.7	_	ns	710 – 20011IA

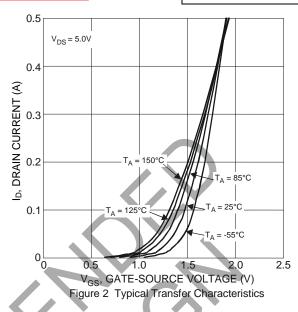
Notes:

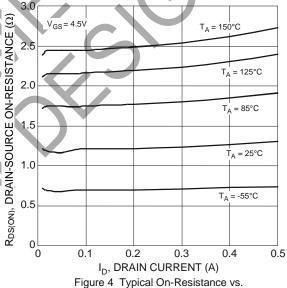
- 5. Device mounted on FR-4 PCB with minimum recommended pad layout, single sided.
- Repetitive rating, pulse width limited by junction temperature.
 Short duration pulse test used to minimize self-heating effect.
- 8. Guaranteed by design. Not subject to production testing.











Drain Current and Temperature

3.0 $R_{DS(ON)}$, DRAIN-SOURCE ON-RESISTANCE (Ω) 2.5 V_{GS} = 2.5V I_D = 100mA 2.0 $V_{GS} = 4V$ $I_{D} = 200 \text{mA}$ 1.5 1.0 0 -50 25 100 -25 50 75 125 T_{.I}, JUNCTION TEMPERATURE (°C)

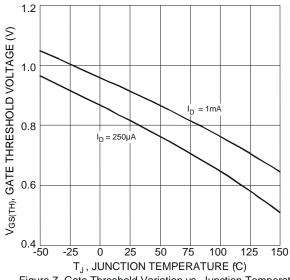
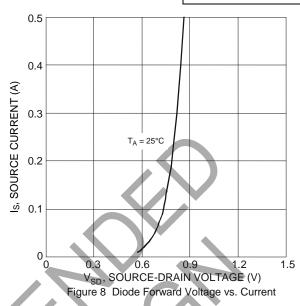
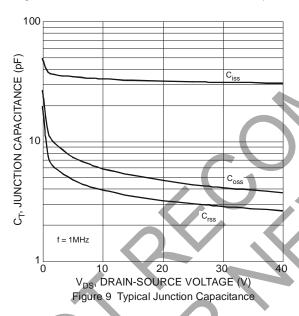
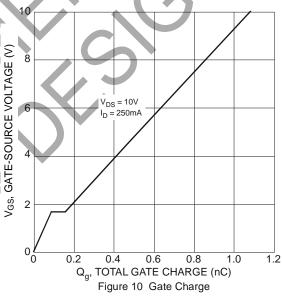


Figure 7 Gate Threshold Variation vs. Junction Temperature







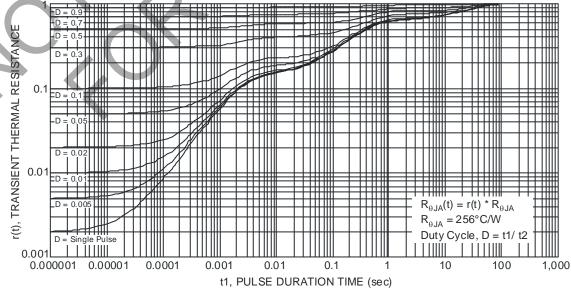


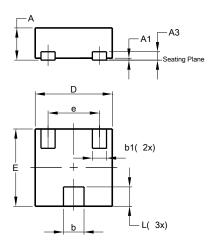
Figure 11 Transient Thermal Resistance



Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

X1-DFN1212-3

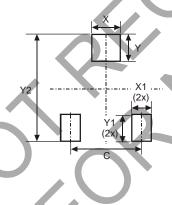


X1-DFN1212-3						
Dim	Min	Max	Typ			
Α	0.47	0.53	0.50			
A1	0	0.05	0.02			
A3	-	•	0.13			
b	0.27	0.37	0.32			
b1	0.17	0.27	0.22			
D	1.15	1.25	1.20			
Е	1.15	1.25	1.20			
е	-	-	0.80			
L	0.25	0.35	0.30			
All D	All Dimensions in mm					

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

X1-DFN1212-3



Dimensions	Value (in mm)
С	0.80
Х	0.42
X1	0.32
Υ	0.50
Y1	0.50
Y2	1.50



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DMN62D0LFD

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