











CSD25404Q3

SLPS570 - NOVEMBER 2015

CSD25404Q3 -20 V P-Channel NexFET™ Power MOSFET

Features

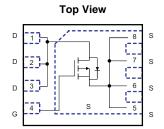
- Ultra-Low Qa and Qad
- Low Thermal Resistance
- Low R_{DS(on)}
- Halogen Free
- **RoHS Compliant**
- Pb Free Terminal Plating
- SON 3.3 mm x 3.3 mm Plastic Package

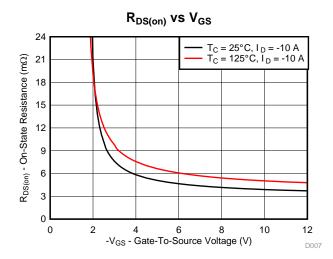
Applications

- **DC-DC Converters**
- **Battery Management**
- Load Switch
- **Battery Protection**

3 Description

This -20 V, 5.5 m Ω NexFETTM power MOSFET is designed to minimize losses in power conversion load management applications with a SON 3.3 mm x 3.3 mm package that offers an excellent thermal performance for the size of the device.





Product Summary

T _A = 25°	С	TYPICAL VA	UNIT	
V_{DS}	Drain-to-source voltage	-20	٧	
Q_g	Gate charge total (-4.5 V)	10.9		nC
Q_{gd}	Gate charge gate to drain	2.2		nC
		$V_{GS} = -1.8 \text{ V}$	40	mΩ
R _{DS(on)}	Drain-to-source on resistance	$V_{GS} = -2.5 \text{ V}$	10.1	mΩ
		$V_{GS} = -4.5 \text{ V}$	5.5	mΩ
V_{th}	Threshold voltage	-0.9		٧

Ordering Information⁽¹⁾

DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD25404Q3	2500	13-Inch Reel	SON 3.3 mm × 3.3	Tape and
CSD25404Q3T	250	7-Inch Reel	mm Plastic Package	Reel

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

T _A = 2	5°C	VALUE	UNIT
V_{DS}	Drain-to-source voltage	-20	٧
V_{GS}	Gate-to-source voltage	±12	٧
	Continuous drain current, T _C = 25°C	-104	
I_D	Continuous drain current (package limit)	-60	Α
	Continuous drain current ⁽¹⁾	-18	
I_{DM}	Pulsed drain current ⁽²⁾	-240	Α
п	Power dissipation ⁽¹⁾	2.8	W
P_D	Power dissipation, T _C = 25°C	96	VV
T _J , T _{stg}	Operating junction, storage temperature	-55 to 150	°C

- (1) R_{θJA} = 45°C/W on 1 inch² Cu (2 oz.) on 0.060 inch thick FR4 PCB.
- (2) Max $R_{\theta JC}$ = 1.3, pulse duration ≤100 µs, duty cycle ≤1%.

Gate Charge

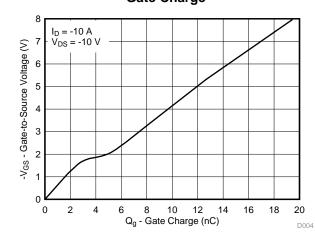






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4 Revision History

DATE	REVISION	NOTES
November 2015	*	Initial release.

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5 Specifications

5.1 Electrical Characteristics

 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$

	PARAMETER	TEST CONDITIONS	MIN T	YP MAX	UNIT
STATIC	CHARACTERISTICS		'		
BV _{DSS}	Drain-to-source voltage	$V_{GS} = 0 \text{ V}, I_{D} = -250 \mu\text{A}$	-20		V
I _{DSS}	Drain-to-source leakage current	V _{GS} = 0 V, V _{DS} = -16 V		-1	μΑ
I _{GSS}	Gate-to-source leakage current	V _{DS} = 0 V, V _{GS} = ±12 V		-100	nA
V _{GS(th)}	Gate-to-source threshold voltage	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	-0.65 -0	90 –1.15	V
		$V_{GS} = -1.8 \text{ V}, I_D = -1 \text{ A}$		40 150	mΩ
R _{DS(on)}	Drain-to-source on resistance	$V_{GS} = -2.5 \text{ V}, I_D = -10 \text{ A}$	1	0.1 12.1	mΩ
		$V_{GS} = -4.5 \text{ V}, I_D = -10 \text{ A}$		5.5 6.5	mΩ
9 _{fs}	Transconductance	$V_{DS} = -10 \text{ V}, I_{D} = -10 \text{ A}$		47	S
DYNAMI	C CHARACTERISTICS				
C _{ISS}	Input capacitance		16	30 2120	pF
Coss	Output capacitance	$V_{GS} = 0 \text{ V}, V_{DS} = -10 \text{ V},$ f = 1 MHz	9	02 1170	pF
C _{RSS}	Reverse transfer capacitance	, - 1 Wii 12		52 68	рF
R_G	Series gate resistance			0.8 2.4	Ω
Qg	Gate charge total (-4.5 V)		1	0.8 14.1	nC
Q_{gd}	Gate charge gate to drain	V 40 V 1 40 A		2.2	nC
Q _{gs}	Gate charge gate to source	$V_{DS} = -10 \text{ V}, I_{D} = -10 \text{ A}$		2.8	nC
Q _{g(th)}	Gate charge at V _{th}			1.5	nC
Q _{OSS}	Output charge	$V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V}$		9.0	nC
t _{d(on)}	Turn on delay time			13	ns
t _r	Rise time	$V_{DS} = -10 \text{ V}, V_{GS} = -4.5 \text{ V},$		8	ns
t _{d(off)}	Turn off delay time	$I_D = -10 \text{ A}, R_G = 5 \Omega$		35	ns
t _f	Fall time			13	ns
DIODE C	HARACTERISTICS				
V_{SD}	Diode forward voltage	I _S = -10 A, V _{GS} = 0 V	_	0.8 –1	V
Q _{rr}	Reverse recovery charge	$V_{DS} = -10 \text{ V}, I_F = -10 \text{ A},$	2	0.5	nC
t _{rr}	Reverse recovery time	di/dt = 200 A/μs		26	ns

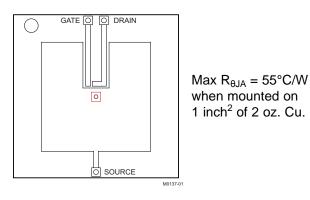
5.2 Thermal Information

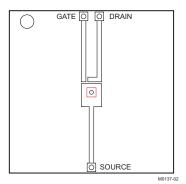
(T_A = 25°C unless otherwise stated)

	THERMAL METRIC	MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance ⁽¹⁾			1.3	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance ⁽¹⁾⁽²⁾			55	°C/W

 $R_{\theta JC}$ is determined with the device mounted on a 1 inch² (6.45 cm²), 2 oz. (0.071 mm thick) Cu pad on a 1.5 inch × 1.5 inch (3.81 cm × 3.81 cm), 0.06 inch (1.52 mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design. Device mounted on FR4 material with 1 inch² (6.45 cm²), 2 oz. (0.071 mm thick) Cu.



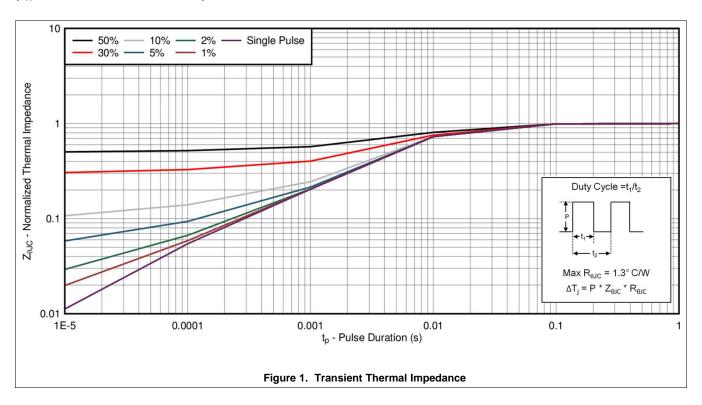




Max $R_{\theta JA} = 160^{\circ}\text{C/W}$ when mounted on minimum pad area of 2 oz. Cu.

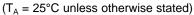
5.3 Typical MOSFET Characteristics

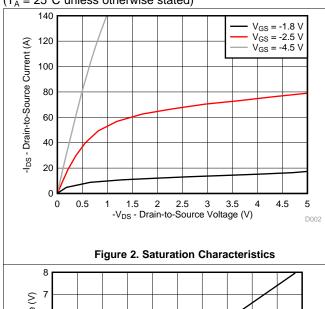
(T_A = 25°C unless otherwise stated)

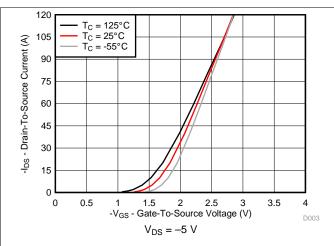




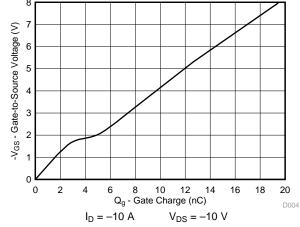
Typical MOSFET Characteristics (continued)











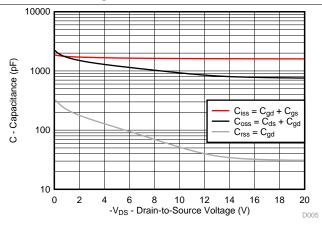
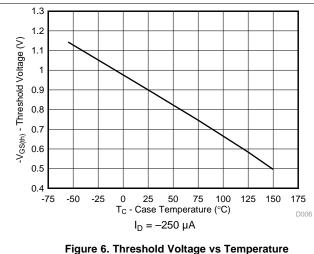


Figure 4. Gate Charge

Figure 5. Capacitance



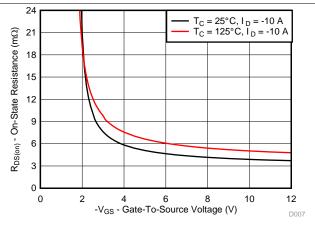
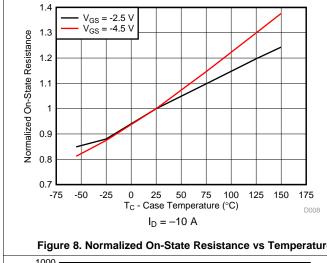


Figure 7. On-State Resistance vs Gate-to-Source Voltage

ISTRUMENTS

Typical MOSFET Characteristics (continued)

 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$



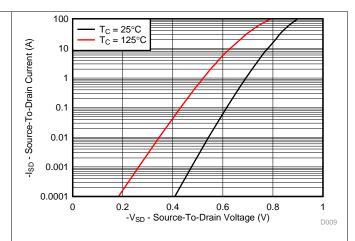


Figure 8. Normalized On-State Resistance vs Temperature

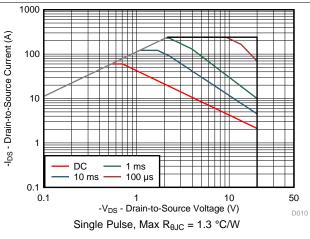


Figure 10. Maximum Safe Operating Area

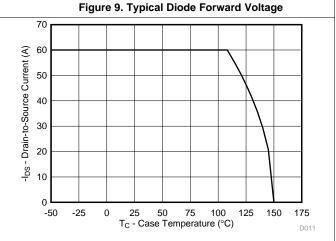


Figure 11. Maximum Drain Current vs Temperature



6 Device and Documentation Support

6.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.2 Trademarks

NexFET, E2E are trademarks of Texas Instruments.

All other trademarks are the property of their respective owners.

6.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.4 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

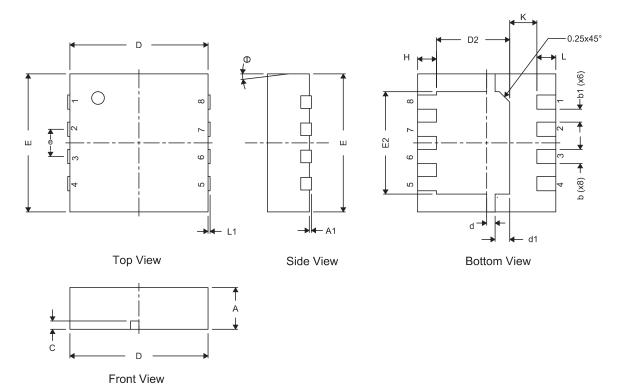
Product Folder Links: CSD25404Q3

TEXAS INSTRUMENTS

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 CSD25404Q3 Package Dimensions

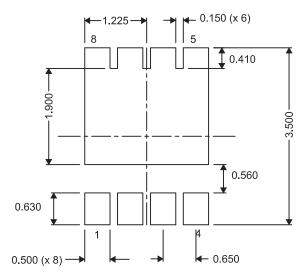


DIM	М	ILLIMETERS		INCHES			
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
Α	0.950	1.000	1.100	0.037	0.039	0.043	
A1	0.000	0.000	0.050	0.000	0.000	0.002	
b	0.280	0.340	0.400	0.011	0.013	0.016	
b1		0.310 NOM			0.012 NOM		
С	0.150	0.200	0.250	0.006	0.008	0.010	
D	3.200	3.300	3.400	0.126	0.130	0.134	
D2	1.650	1.750	1.800	0.065	0.069	0.071	
d	0.150	0.200	0.250	0.006	0.008	0.010	
d1	0.300	0.350	0.400	0.012	0.014	0.016	
E	3.200	3.300	3.400	0.126	0.130	0.134	
E2	2.350	2.450	2.550	0.093	0.096	0.100	
е		0.650 TYP			0.026 TYP		
Н	0.35	0.450	0.550	0.014	0.018	0.022	
K		0.650 TYP			0.026 TYP		
L	0.35	0.450	0.550	0.014	0.018	0.022	
L1	0	_	0	0		0	
θ	0		0	0		0	

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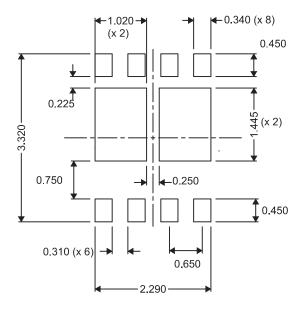
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7.2 Recommended PCB Pattern



For recommended circuit layout for PCB designs, see application note SLPA005 – Reducing Ringing Through PCB Layout Techniques.

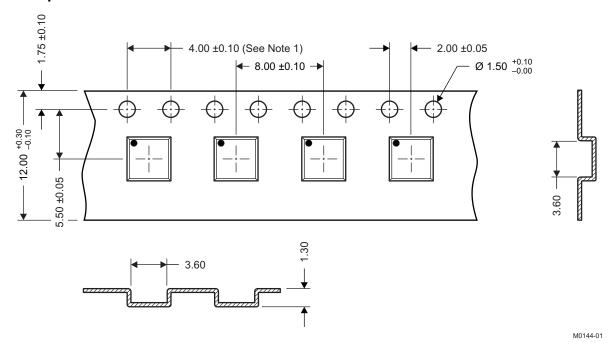
7.3 Recommended Stencil Opening



All dimensions are in mm, unless otherwise specified.

TEXAS INSTRUMENTS

7.4 Q3 Tape and Reel Information



Notes:

- 1. 10 sprocket hole pitch cumulative tolerance ±0.2
- 2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm
- 3. Material: black static dissipative polystyrene
- 4. All dimensions are in mm (unless otherwise specified).
- 5. Thickness: 0.30 ±0.05 mm
- 6. MSL1 260°C (IR and Convection) PbF-Reflow Compatible

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PACKAGE OPTION ADDENDUM

10-Nov-2015

PACKAGING INFORMATION

Orderable Device	Status	Package Type	_	Pins	_	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
CSD25404Q3	ACTIVE	VSON-CLIP	DQG	8	2500	Pb-Free (RoHS Exempt)	CU SN	Level-1-260C-UNLIM	-55 to 150	CSD25404	Samples
CSD25404Q3T	ACTIVE	VSON-CLIP	DQG	8	250	Pb-Free (RoHS Exempt)	CU SN	Level-1-260C-UNLIM	-55 to 150	CSD25404	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE OPTION ADDENDUM

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