LMP848x 具有电压输出的高精度 76V 高侧电流感测放大器

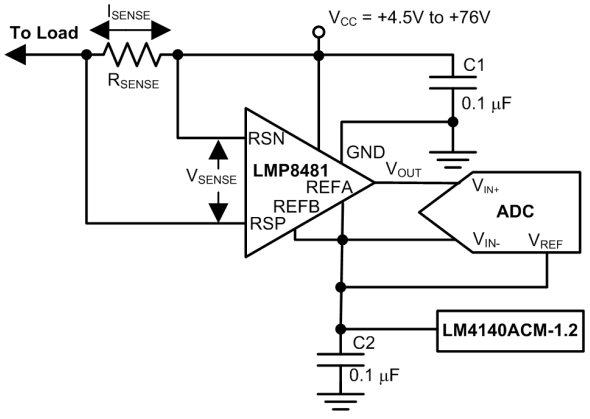
1 特性

- 典型值，T_A=25°C
- 双向或单向感测
- 共模电压范围为 4.0V 至 76V
- 电源电压范围为 4.5V 至 76V
- 固定增益包括 20V/V、60V/V 和 100V/V
- 增益精度为 ±0.1%
- 偏移为 ±80µV
- 带宽为 270kHz（–3dB 时）
- 静态电流 < 100µA
- 缓冲后的高电流输出 > 5mA
- 输入偏置电流为 7µA
- 电源抑制比 (PSRR) (DC) 为 122dB
- 共模抑制比 (CMRR) (DC) 为 124dB
- 温度范围：–40°C 至 125°C
- 8 引脚超薄小外形尺寸 (VSSOP) 封装

2 应用

- 高侧电流感测
- 车辆电流测量
- 电信
- 电机控制
- 激光或发光二极管 (LED) 驱动器
- 电源管理
- 太阳能面板监控

典型应用电路原理图



3 说明

LMP8480 和 LMP8481 是精密的高侧电流感测放大器，可将作用于电流感测电阻两端较小的差分电压放大为高输入共模电压。 此类放大器设计用于双向 (LMP8481) 或单向 (LMP8480) 电流应用，可接收共模电压范围为 4V 至 76V 且带宽为 270kHz 的输入信号。 由于 LMP848x 的工作电源电压范围与输入共模电压范围发生重叠，因此该器件可由同一电压（处于被监控状态）进行供电。 其优势是无需对电流受到监控的负载点施加中间电源电压，从而减少组件数并节省电路板空间。

LMP848x 系列器件的固定增益包括 20、60 和 100，适用于温度精度要求较高的应用。 低输入偏移电压允许在不增大系统误差的前提下使用较小的感测电阻。 凭借 –40°C 至 125°C 的宽运行温度范围，LMP848x 成为汽车、电信、工业和消费类应用的理想选择。 LMP8480 和 LMP8481 是 MAX4080 和 MAX4081 的引脚到引脚替代产品，可提升偏移电压、扩大基准调节范围并提高输出驱动能力。 LMP8480 和 LMP8481 采用 8 引脚 VSSOP 封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
LMP8480	VSSOP (8)	3.00mm x 3.00mm
LMP8481	VSSOP (8)	3.00mm x 3.00mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

目录

4 修订历史记录

Changes from Revision B (December 2014) to Revision C **Page**

- 已删除 LMP8480 和 LMP8481 的 WSON 封装选项 ... 1
- 已删除 -F 版本（50x 增益） ... 3
- Deleted WSON package options for LMP8480 and LMP8481 ... 3

Changes from Revision A (August 2012) to Revision B **Page**

- 已添加 *引脚配置和功能*部分，*ESD 额定值*表，*特性描述*部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分 ... 1

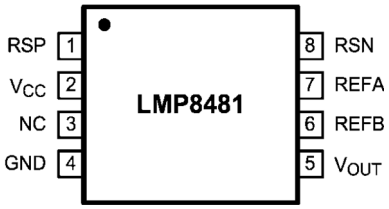
5 器件比较表

器件名称	增益	极性
LMP8480-T	x20	单向
LMP8480 和 LMP8481 的 LMP8480-S	x60	单向
LMP8480-H	x100	单向
LMP8481-T	x20	双向或单向
LMP8481-S	x60	双向或单向
LMP8481-H	x100	双向或单向

6 Pin Configuration and Functions

LMP8480 VSSOP PACKAGE
8 PINS
(TOP VIEW)

LMP8481 VSSOP PACKAGE
8 PINS
(TOP VIEW)



Pin Functions

PIN		I/O	DESCRIPTION	
NAME	NO.			
R_{SP}	1	I	Positive current sense input	
VCC	2	P	Positive supply voltage	
NC	3	—	No Connection – Not internally Connected.	
GND	4	P	Ground	
V_{OUT}	5	O	Output	
NC or R_{EFA}	6	I	LMP8480: No Connection	LMP8481: Reference Voltage “B” Input
NC or R_{EFB}	7	I	LMP8480: No Connection	LMP8481: Reference Voltage “A” Input
R_{SN}	8	I	Negative current sense input	

7 Specifications

7.1 Absolute Maximum Ratings(1)(2)

Over operating free-air temperature range (unless otherwise noted)(3)

		MIN	MAX	UNIT
Supply Voltage (V_{CC} to GND)		–0.3	85	V
R_{SP} or R_{SN} to GND		–0.3	85	V
V_{OUT} to GND		–0.3 to the lesser of (V_{CC} + 0.3) or +20		V
V_{REF} Pins (LMP8481 Only)	Other V_{REF} pin tied to ground	–0.3	12	V
	Applied to both V_{REF} Pins tied together	–0.3	6	V
Differential Input Voltage		–85	85	V
Current into output pin		–20(4)	20	mA
Current into any other pins		–5(4)	5	mA
Operating Temperature		–40	125	°C
Junction Temperature		-40	150	°C
Storage temperature		–65	150	°C

(1) The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_{J(MAX)}$, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation $P_{DMAX} = (T_{J(MAX)} – T_A)/ \theta_{JA}$ or the number given in *Absolute Maximum Ratings*, whichever is lower.
(2) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(4) When the input voltage (VIN) at any pin exceeds power supplies (VIN < GND or VIN > VS), the current at that pin must not exceed 5 mA, and the voltage (VIN) has to be within the *Absolute Maximum Ratings* for that pin. The 20-mA package input current rating limits the number of pins that can safely exceed the power supplies with current flow to four pins.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Expected normal operating conditions over free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply Voltage (V_{CC})		4.5	76	V
Common Mode Voltage		4.0	76	V
Reference Input (LMP8481 Only)	V_{REFA} and V_{REFB} tied together	–0.3 to the lesser of (V_{CC} – 1.5) or +6		V
	Single V_{REF} pin with other V_{REF} pin grounded	–0.3 or +12 where the average of the two V_{REF} pins is less than the lesser of (V_{CC} – 1.5) or +6		V

(1) Exceeding the *Recommended Operating Conditions* for extended periods of time may effect device reliability or cause parametric shifts.

7.4 Thermal Information

THERMAL METRIC(1)		LMP8480, LMP8481		UNIT
		DGK	NCQ	
		8 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	185	70	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

Unless otherwise specified, all limits specified for at T_A = 25°C, V_{CC} = 4.5 V to 76 V, 4.5V V_{CM} 76 V, R_L = 100 k, V_{SENSE} = (V_{RSP} – V_{RSN}) = 0 V.(1)

PARAMETER		TEST CONDITIONS		MIN(2)	TYP(3)	MAX(2)	UNIT
V_{OS}	Input Offset Voltage (RTI)	VCC = V_{RSP} = 48 V, ΔV = 100 mV	T_A = 25°C		±80	±265	µV
			–40°C ≤ T_A ≤ 125°C			±900	
TCV_{OS}	Input Offset Voltage Drift(4)				±6		µV°C
I_B	Input Bias Current(5)	V_{CC} = V_{RSP} = 76 V, Per Input			6.3		µA
		V_{CC} = V_{RSP} = 76 V, Per Input, –40°C ≤ T_A ≤ 125°C				12	
I_{LEAK}	Input Leakage Current	V_{CC} = 0, V_{RSP} = 86 V, Both inputs together			0.01		µA
		V_{CC} = 0, V_{RSP} = 86 V, Both inputs together, –40°C ≤ T_A ≤ 125°C				2	
$V_{SENSE(MAX)}$	Differential Input Voltage Across Sense Resistor(6)	V_{CC} = 16	-T Version, –40°C ≤ T_A ≤ 125°C			667	mV
			-F Version, –40°C ≤ T_A ≤ 125°C			267	
			-S Version, –40°C ≤ T_A ≤ 125°C			222	
			-H Version, –40°C ≤ T_A ≤ 125°C			133	
A_V	Gain	-T Version			20		V/V
		-T Version, –40°C ≤ T_A ≤ 125°C		19.8		20.2	
		-S Version			60		
		-S Version, –40°C ≤ T_A ≤ 125°C		59.5		60.5	
		-H Version			100		
		-H Version, –40°C ≤ T_A ≤ 125°C		99.2		100.8	
	Gain Error	V_{CC} = V_{RSP} = 48 V	T_A = 25°C			±0.6%	
			–40°C ≤ T_A ≤ 125°C			±0.8%	
DC PSRR	DC Power Supply Rejection Ratio	V_{RSP} = 48 V, V_{CC} = 4.5 to 76 V			122		dB
		V_{RSP} = 48 V, V_{CC} = 4.5 to 76 V, –40°C ≤ T_A ≤ 125°C		100			
DC CMRR	DC Common Mode Rejection Ratio	V_{CC} = 48 V, V_{RSP} = 4.5 to 76 V			124		dB
		V_{CC} = 48 V, V_{RSP} = 4.5 to 76 V, –40°C ≤ T_A ≤ 125°C		100			
		V_{CC} = 48 V, V_{RSP} = 4 to 76 V			124		dB
CMVR	Input Common Mode Voltage Range	CMRR > 100 dB, –40°C ≤ T_A ≤ 125°C		4		76	V
R_{OUT}	Output Resistance / Load Regulation	V_{SENSE} = 100 mV			0.1		
V_{OMAX}	Maximum Output Voltage (Headroom) (V_{OMAX} = V_{CC} – V_{OUT})	V_{CC} = 4.5 V, V_{RSP} = 48 V, V_{SENSE} = +1 V, I_{OUT} (sourcing) 500 µA			230	500	mV

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. ***No*** specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A.
(2) All limits are specified by testing, design, or statistical analysis.
(3) Typical values represent the most likely parametric norm at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) Offset voltage temperature drift is determined by dividing the change in V_{OS} at the temperature extremes by the total temperature change.
(5) Positive Bias Current corresponds to current flowing into the device.
(6) This parameter is specified by design and/or characterization and is not tested in production.

Electrical Characteristics (continued)

Unless otherwise specified, all limits specified for at T_A = 25°C, V_{CC} = 4.5 V to 76 V, 4.5V V_{CM} 76 V, R_L = 100 k, V_{SENSE} = (V_{RSP} – V_{RSN}) = 0 V.(1)

PARAMETER		TEST CONDITIONS	MIN(2)	TYP(3)	MAX(2)	UNIT
V_{OMIN}	Minimum Output Voltage	V_{CC} = V_{RSP} = 48 V, V_{SENSE} = –1 V, I_{OUT} (sinking) = 10 µA		3		mV
		V_{CC} = V_{RSP} = 48 V, V_{SENSE} = –1 V, I_{OUT} (sinking) = 10 µA, –40°C ≤ T_A ≤ 125°C			15	
		V_{CC} = V_{RSP} = 4.5 V, V_{SENSE} = –1 V, I_{OUT} (sinking) = 10 µA		3		
		V_{CC} = V_{RSP} = 48 V, V_{SENSE} = –1 V, I_{OUT} (sinking) = 100 µA		18		
		V_{CC} = V_{RSP} = 48 V, V_{SENSE} = –1 V, I_{OUT} (sinking) = 100 µA, –40°C ≤ T_A ≤ 125°C			55	
		V_{CC} = V_{RSP} = 4.5 V, V_{SENSE} = –1 V, I_{OUT} (sinking) = 100 µA		18		
V_{OLOAD}	Output voltage with load	V_{CC} = 28 V, V_{RSP}=28 V, V_{SENSE}= 600 mV, I_{OUT} (sourcing) = 500 µA		12		V
V_{OLREG}	Output Load Regulation	V_{CC} = 20, V_{RSP} = 16, V_{OUT} = 12, ΔI_L = 200 na to 8 mA		0.001%		
I_{CC}	Supply Current	V_{OUT} = 2 V, R_L = 10 M, V_{CC} = V_{RSP} = 76 V		88		µA
		V_{OUT} = 2 V, R_L = 10 M, V_{CC} = V_{RSP} = 76 V, –40°C ≤ T_A ≤ 125°C			155	
BW	–3 dB Bandwidth	R_L = 10 M, C_L = 20 pF		270		kHz
SR	Slew rate(7)	V_{SENSE} from 10 mV to 80 mV, R_L = 10 M, C_L = 20 pF		1		V/µs
e_{ni}	Input Referred Voltage Noise	f = 1 kHz		95		nV/√Hz
t_{SETTLE}	Output Settling Time to 1% of Final Value	V_{SENSE} = 10 mV to 100 mV and 100 mV to 10 mV		20		µs
t_{PU}	Power-up Time	V_{CC} = V_{RSP} = 48 V, VS_{ENSE} = 100 mV, output to 1% of final value		50		µs
$t_{RECOVERY}$	Saturation Recovery Time	Output settles to 1% of final value, the device will not experience phase reversal when overdriven.		50		µs
C_{LOAD}	Max Output Capacitance Load	No sustained oscillations		500		pF

(7) The number specified is the average of rising and falling slew rates and measured at 90% to 10%.

7.6 Typical Characteristics

Unless otherwise specified, T_A = 25°C, V_{CC} = 4.5 V to 76 V, 4.5 V < V_{CM} < 76 V, R_L = 100k, V_{SENSE} = (V_{RSP} – V_{RSN}) = 0 V, for all gain options.

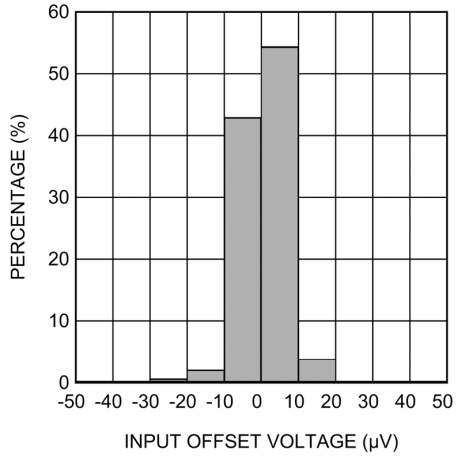


Figure 1. Offset Voltage Histogram

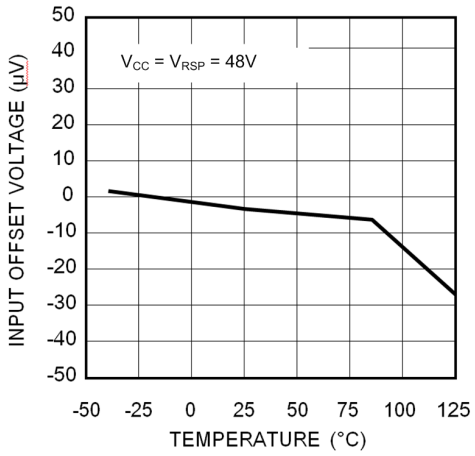


Figure 2. Typical Offset Voltage vs Temperature

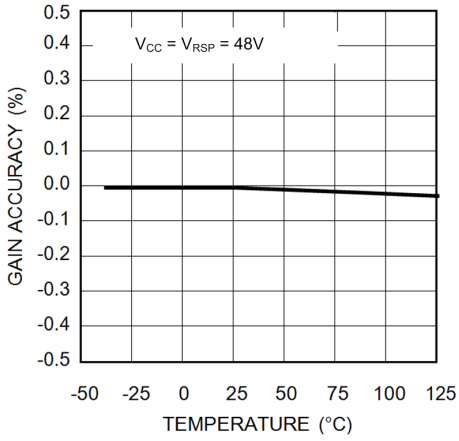


Figure 3. Typical Gain Accuracy vs Temperature

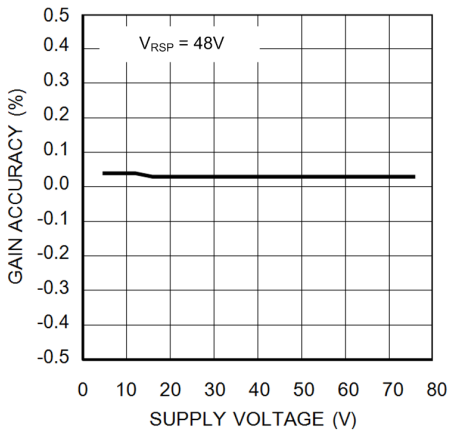


Figure 4. Typical Gain Accuracy vs Supply Voltage

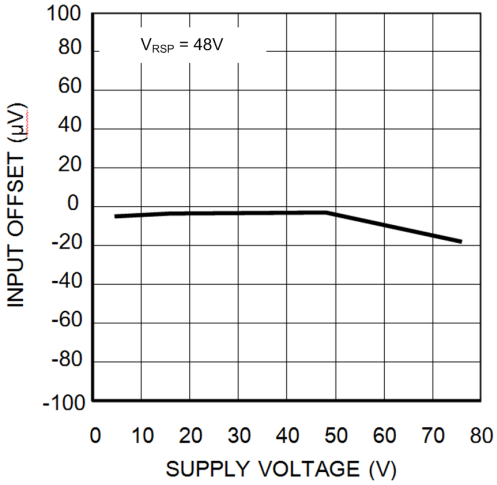


Figure 5. Typical Offset Voltage vs Supply Voltage

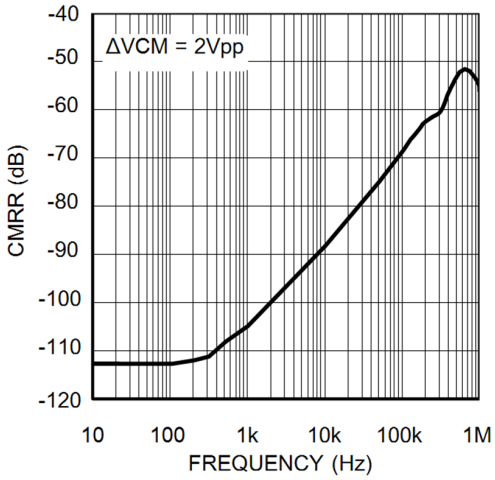


Figure 6. AC Common-Mode Rejection Ratio vs Frequency

Typical Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V_{CC} = 4.5 V to 76 V, 4.5 V < V_{CM} < 76 V, R_L = 100k, V_{SENSE} = (V_{RSP} – V_{RSN}) = 0 V, for all gain options.

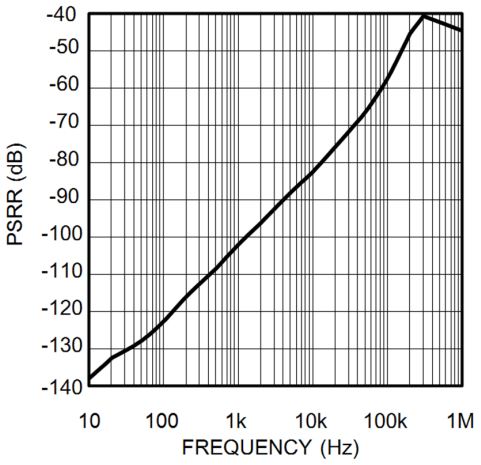


Figure 7. AC Power Supply Rejection Ratio vs Frequency

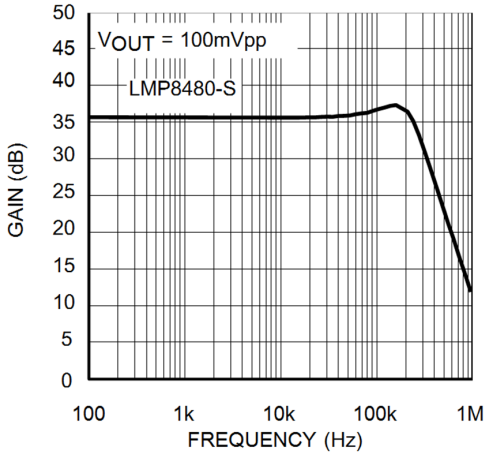


Figure 8. Small Signal Gain vs Frequency

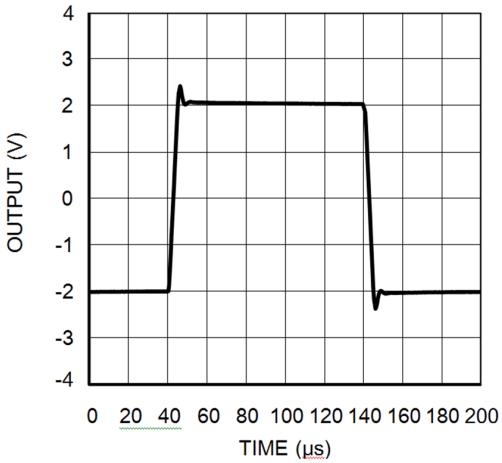


Figure 9. Large Signal Pulse Response

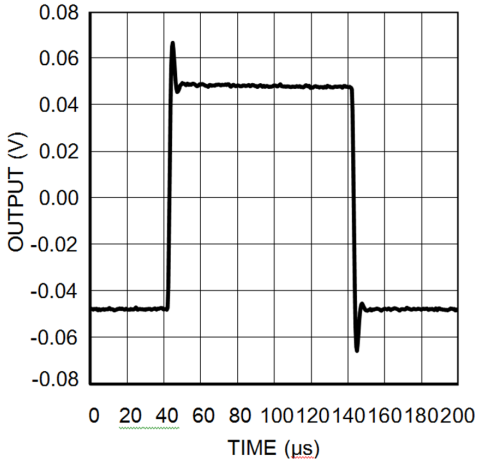


Figure 10. Small Signal Pulse Response

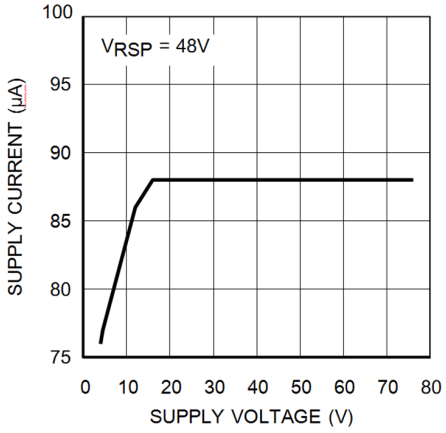


Figure 11. Supply Current vs Supply Voltage

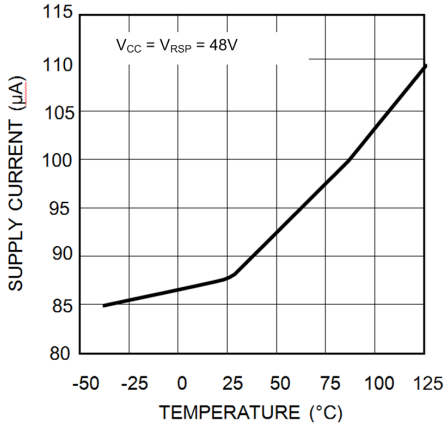


Figure 12. Supply Current vs Temperature

Typical Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V_{CC} = 4.5 V to 76 V, 4.5 V < V_{CM} < 76 V, R_L = 100k, V_{SENSE} = (V_{RSP} – V_{RSN}) = 0 V, for all gain options.

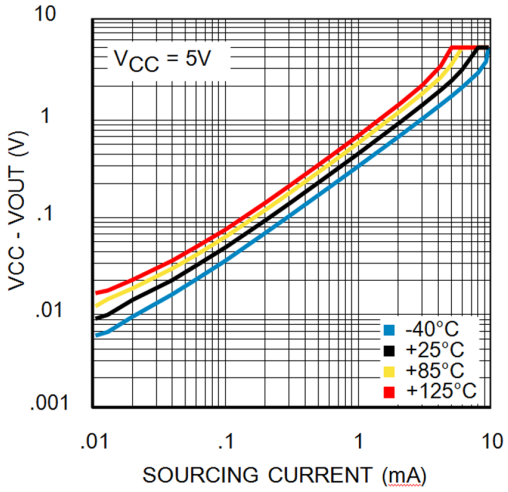


Figure 13. Saturated Output Sourcing Current at 4.5 V

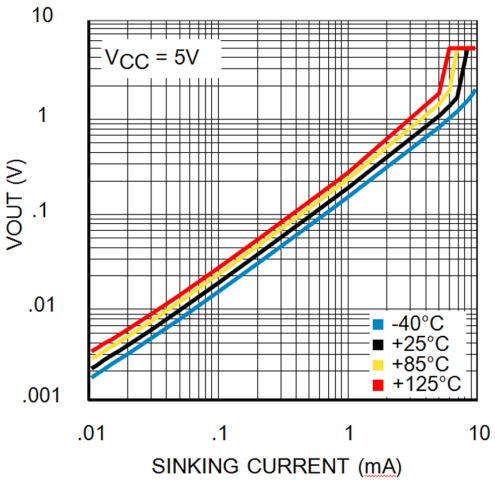


Figure 14. Saturated Output Sinking Current at 4.5 V

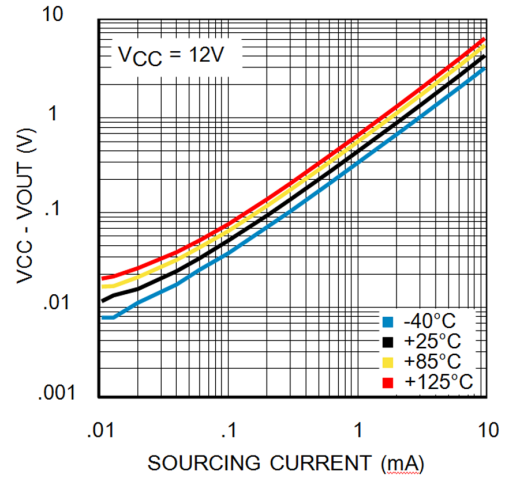


Figure 15. Saturated Output Sourcing Current at 12 V

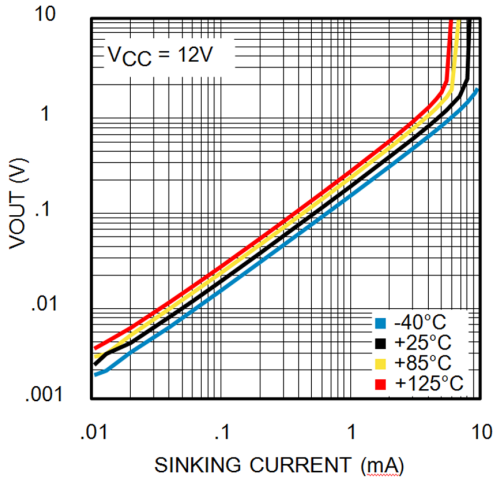


Figure 16. Saturated Output Current Sinking at 12 V

8 Detailed Description

8.1 Overview

The LMP8480 and LMP8481 are single-supply, high-side current sense amplifiers with available fixed gains of x20, x60 and x100. The power supply range is 4.5 V to 76 V, while the common-mode input voltage range is capable of 4.0-V to 76-V operation. The supply voltage and common-mode range are completely independent of each other. This makes the LMP848x supply voltage extremely flexible, as the LMP848x's supply voltage can be greater than, equal to, or less than the load source voltage, and allowing the device to be powered from the system supply or the load supply voltage.

The LMP8480 and LMP8481 supply voltage does not have to be larger than the load source voltage. A 76-V load source voltage with a 5-V supply voltage is perfectly acceptable.

8.1.1 Theory of Operation

The LMP8480 and LMP8481 are comprised of two main stages. The first stage is a differential input current to voltage converter, followed by a differential voltage amplifier and level-shifting output stage. Also present is an internal 14 Volt Low-Dropout Regulator (LDO) to power the amplifiers and output stage, as well as a reference divider resistor string to allow the setting of the reference level.

As seen in Figure 18, the current flowing through R_{SENSE} develops a voltage drop called V_{SENSE}. The voltage across the sense resistor, V_{SENSE}, is then applied to the input R_{SP} and R_{SN} pins of the amplifier.

Internally, the voltage on each input pin is converted to a current by the internal precision thin-film input resistors R_{GP} and R_{GN}. A second set of much higher value V_{CM} sense resistors between the inputs provide a sample of the input common-mode voltage for internal use by the differential amplifier.

V_{SENSE} is applied to the differential amplifier through R_{GP} and R_{GN}. These resistors change the input voltage to a differential current. The differential amplifier then servos the resistor currents through the MOSFETs to maintain a zero balance across the differential amplifier inputs.

With no input signal present, the currents in R_{GP} and R_{GN} are equal. When a signal is applied to V_{SENSE}, the current through R_{GP} and R_{GN} are imbalanced and are no longer equal. The amplifier then servos the MOSFETS to correct this current imbalance, and the extra current required to balance the input currents is then reflected down into the two lower 400-kΩ “tail” resistors. The difference in the currents into the tail resistors is therefore proportional to the amplitude and polarity of V_{SENSE}. The tail resistors, being larger than the input resistors for the same current, then provide voltage gain by changing the current into a proportionally larger voltage. The gain of the first stage is then set by the tail resistor value divided by R_G value.

The differential amplifier stage then samples the voltage difference across the two 400-kΩ tail resistors and also applies a further gain-of-five and output level-shifting according to the applied reference voltage (V_{REF}).

The resulting output of the amplifier will be equal to the differential input voltage times the gain of the device, plus any voltage value applied to the two VREF pins.

The resistor values in the schematic are ideal values for clarity and understanding. Table 1 shows the actual values used that account for parallel combinations and loading. This table can be used for calculating the effects of any additional external resistance.

The LMP8480 is identical to the LMP8481, except that both the V_{REF} pins are grounded internally.

Table 1. Actual Internal Resistor Values

Gain Option	R_{GP} and R_{GN} (each)	$R_{VCMSENSE}$ (each)	R_{TAIL} (each)	Differential Amp FB (each)	V_{REFx} Resistors (each)
20x	98.38 k	491.9 k	393.52 k	1967.6 k	98.38 k
60x	32.793 k	172.165 k	393.52 k	1967.6 k	98.38 k
100x	19.676 k	98.38 k	393.52 k	1967.6 k	98.38 k

8.2 Functional Block Diagrams

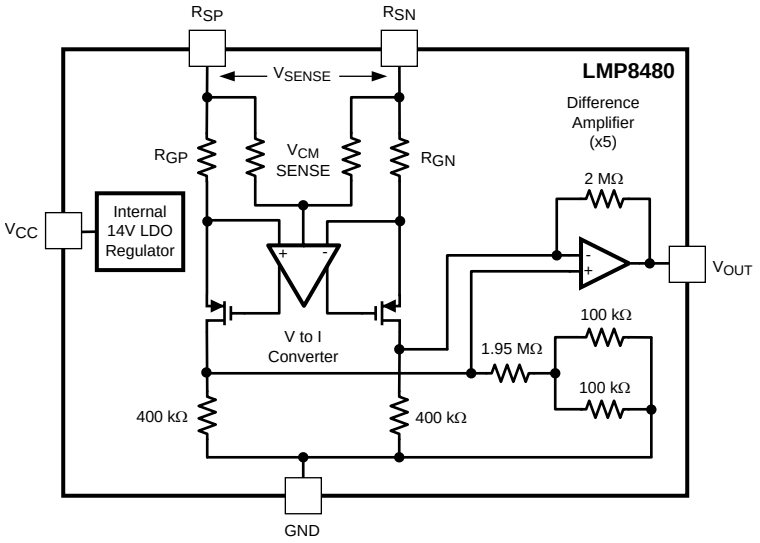


Figure 17. LMP8480 Block Diagram

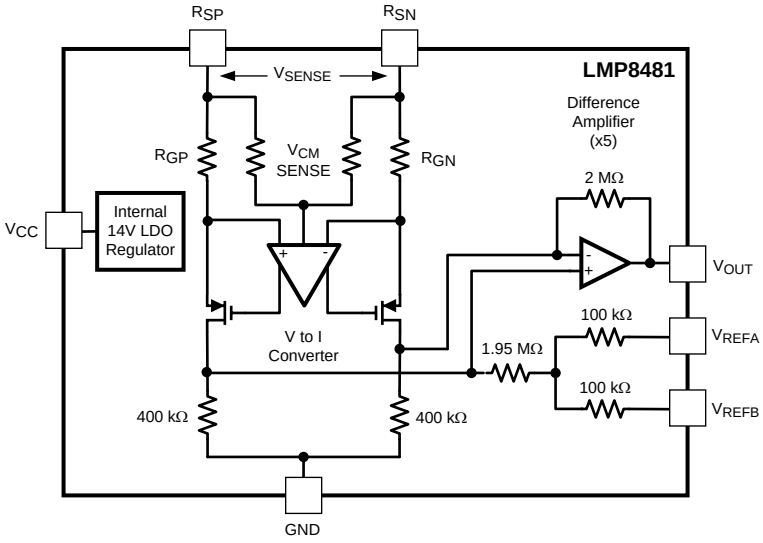


Figure 18. LMP8481 Block Diagram

8.3 Feature Description

8.3.1 Basic Connections

Figure 19 through Figure 22 show the basic connections for seveal different configurations.

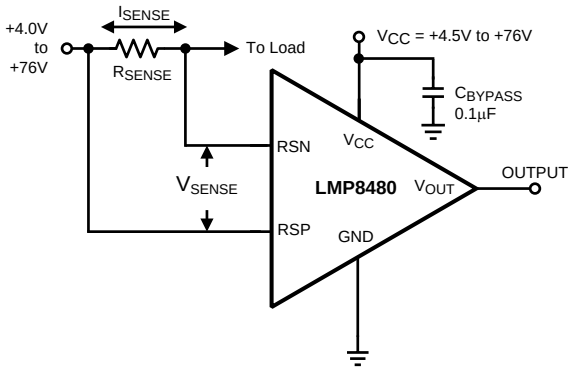


Figure 19. LMP8480 Basic Connections (Unidirectional)

Figure 19 shows the basic connections for the LMP8480 for Unidirectional applications. The output will be at zero with zero sense voltage.

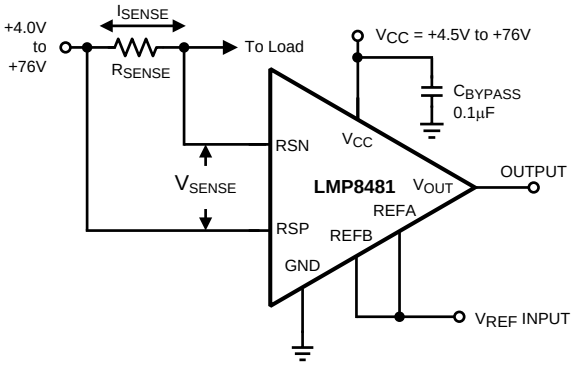


Figure 20. LMP8481 Basic Connections for External 1:1 V_{REF} Input (Bidirectional)

Figure 20 shows the basic connections for the LMP8481 for Bidirectional applications using an external reference input. At zero input voltage, the output will be at the applied reference voltage (V_{REF}), moving positive or negative from the zero reference point.

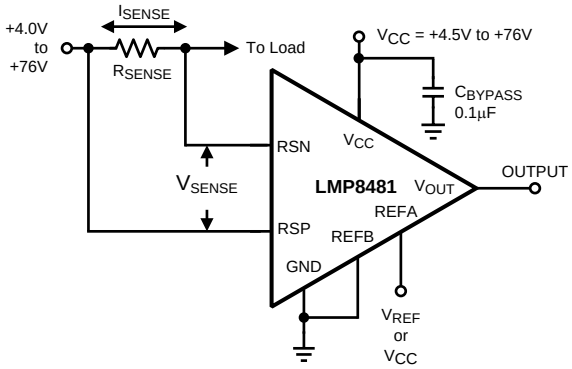


Figure 21. LMP8481 Basic Connections for Mid-Bias (V_{REF}/2) Input (Bidirectional)

Feature Description (continued)

Figure 21 shows the basic connections for the LMP8481 for Bidirectional applications centering the output at one-half the applied V_{REF} or V_{CC} voltage. If V_{REFA} is connected to V_{CC}, then the output "zero" point will be $V_{CC}/2$. If V_{REFA} is connected to the ADC V_{REF} line, then the "zero" output will be at mid-scale for the ADC.

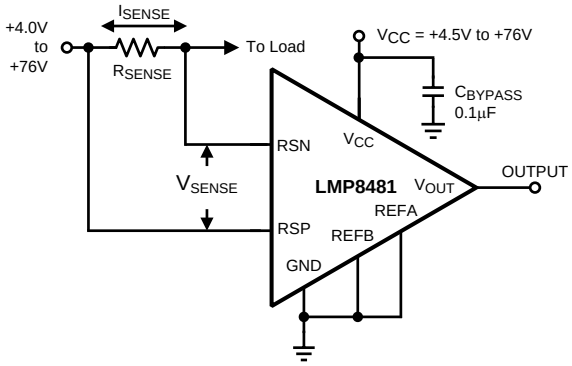


Figure 22. LMP8481 Connections for Unidirectional Configuration (Equivalent to LMP8480 Unidirectional)

Figure 22 shows the how to connect the LMP8481 for Bidirectional applications, thus making it equivalent to the LMP8480 in Figure 19.

8.3.2 Selection of the Sense Resistor

The accuracy of the current measurement depends heavily on the accuracy of the shunt resistor R_{SENSE}. Its value depends on the application and is a compromise between small-signal accuracy, maximum permissible voltage drop and allowable power dissipation in the current measurement circuit.

The use of a “4-terminal” or “Kelvin” sense resistor is highly recommended. See the *Layout Guidelines*.

For best results, the value of the resistor is calculated from the maximum expected load current I_{LMAX} and the expected maximum output swing V_{OUTMAX}, plus a few percent of headroom. See the *Maximum Output Voltage* section for details about the maximum output voltage limits.

High values of R_{SENSE} provide better accuracy at lower currents by minimizing the effects of amplifier offset. Low values of R_{SENSE} minimize load voltage loss, but at the expense of accuracy at low currents. A compromise between low current accuracy and load circuit losses must generally be made.

The maximum V_{SENSE} voltage that must be generated across the R_{SENSE} resistor will be:

$$V_{SENSE} = V_{OUTMAX} / A_V \quad (1)$$

NOTE

The maximum V_{SENSE} voltage should be no more than 667 mV.

From this maximum V_{SENSE} voltage, the R_{SENSE} value can be calculated from:

$$R_{SENSE} = V_{SENSE} / I_{LMAX} \quad (2)$$

Take care not exceed the maximum power dissipation of the resistor. The maximum sense resistor power dissipation will be:

$$P_{RSENSE} = V_{SENSE} \times I_{LMAX} \quad (3)$$

TI recommends using a 2-3x minimum safety margin in selecting the power rating of the resistor.

8.3.3 Using PCB Traces as Sense Resistors

While it may be tempting to use a known length of PCB trace resistance as a sense resistor, it is not recommended.

The temperature coefficient of copper is typically 3300-4000 ppm/°K, which can vary over PCB process variations and require measurement correction (possibly requiring ambient temperature measurements).

Feature Description (continued)

A typical surface mount sense resistor tempco is in the 50 ppm to 500 ppm/°C range offering more measurement consistency and accuracy over the copper trace. Special low-tempco resistors are available in the 0.1 to 50 ppm range, but at a higher cost.

8.3.4 V_{REFA} and V_{REFB} Pins (LMP8481 Only)

The voltage applied to the V_{REFA} and V_{REFB} pins controls the output zero reference level. Depending on how the pins are configured, the output reference level can be set to GND, or V_{CC}/2, or external V_{REF}/2, or the average of two different input references.

The reference inputs consist of a pair of divider resistors with equal values to a common summing point, V_{REF}' as shown in Figure 23. Assuming V_{SENSE} is zero, the output will be at the same value as V_{REF}'.

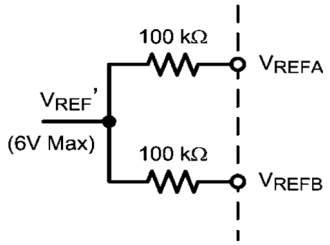


Figure 23. V_{REF} Input Resistor Network

$V_{REF'}$ is the voltage at the resistor tap-point that will be directly applied to the output as an offset. With the two V_{REF} inputs tied together, the output zero voltage will have a 1:1 ratio relationship with V_{REF}.

$$V_{OUT} = ((V_{RSP} – V_{RSN}) \times Av) + V_{REF'} \quad (4)$$

Where:

$$V_{REF'} = V_{REFA} = V_{REFB} \text{ (Equal Inputs)} \quad (5)$$

or:

$$V_{REF'} = (V_{REFA} + V_{REFB}) / 2 \text{ (Different Inputs)} \quad (6)$$

8.3.4.1 One-to-One (1:1) Reference Input

To directly set the reference level, the two inputs are connected to the external reference voltage. The applied VREF will be reflected 1:1 on the output.

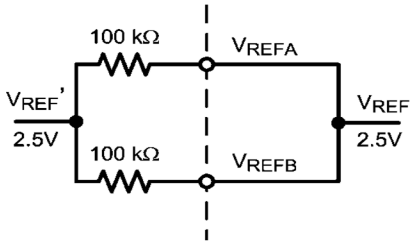


Figure 24. Applying 1:1 Direct Reference Voltage

Feature Description (continued)

8.3.4.2 Setting Output to One-Half V_{CC} or external V_{REF}

For mid-range operation V_{REFB} should be tied to ground and V_{REFA} can be tied to V_{CC} or an external A/D reference voltage. The output will be set to one-half the reference voltage. For example, a 5-V reference would result in a 2.5-V output "zero" reference.

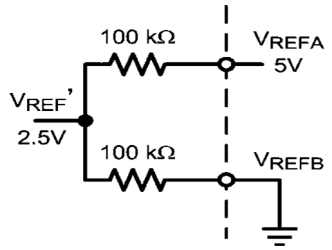


Figure 25. Applying a Divided Reference Voltage

$$V_{REF'} = (V_{REFA} - V_{REFB}) / 2 \quad (7)$$

When the reference pins are biased at different voltages, the output will be referenced to the average of the two applied voltages.

The reference pins should always be driven from clean, stable sources, such as A/D reference lines or clean supply lines. Any noise or drifts on the reference inputs are directly reflected in the output. Take care if the power supply is used as the reference source so as to not introduce supply noise, drift or sags into the measurement.

It is possible to set different resistor divider ratios by adding external resistors in series with the internal 100-K resistors, though the temperature coefficient (tempco) of the external resistors may not tightly track the internal resistors and there will be slight errors over temperature.

The LMP8480 is identical to the LMP8481, except that both the V_{REF} pins are grounded internally. The LMP8481 can replace the LMP8480 if both V_{REF} pins are grounded.

8.3.5 Reference Input Voltage Limits (LMP8481 Only)

The maximum voltage on either reference input pin is limited to VCC or 12 V, whichever is less.

The average voltage on the two V_{REF} pins, and thus the actual output reference voltage level, is limited to a maximum of 1.5 V below VCC, or 6 V, whichever is less. Beware that supply voltages of less than 7.5 V will have a diminishing V_{REF} maximum.

Both V_{REFA} and V_{REFB} may both be grounded to provide a ground referenced output (thus functionally duplicating the LMP8480).

It should be noted that there can be a dynamic error in the V_{REF} to output level matching of up to 100 µV/V. Normally this is not an issue for fixed references, but if the reference voltage is dynamically adjusted during operation, this error needs to be taken into account during calibration routines. This error will vary in both amplitude and polarity part-to-part, but the slope will generally be linear.

8.3.6 Low-Side Current Sensing

The LMP8480 and LMP8481 are not recommended for low-side current sensing at ground level. The voltage on either input pin must be a minimum of 4.0 V above the ground pin for proper operation. The output level may not be valid for common-mode voltages below 4 V. This should be taken into consideration for monitoring or feedback applications where the load-supply voltage may dip below 4 V or be switched completely off.

Feature Description (continued)

8.3.7 Input Series Resistance

Because the input stage uses precision resistors to convert the voltage on the input pin to a current, any resistance added in series with the input pins will change the gain. If a resistance is added in series with an input, the gain of that input will not track that of the other input, causing a constant gain error.

TI does not recommend using external resistances to alter the gain, as external resistors will not have the same thermal matching as the internal thin film resistors.

If resistors are purposely added for filtering, resistance should be added equally to both inputs and the user should be aware that the gain will change slightly. See the end of the *Theory of Operation* section for the internal resistor values. External resistances should be kept below 10 ohms.

8.3.8 Minimum Output Voltage

The amplifier output cannot swing to exactly 0 V. There will always be a minimum output voltage set by the output transistor saturation and input offset errors. This will create a minimum output swing around the zero current reading due to the output saturation. The user should be aware of this when designing any servo loops or data acquisition systems that may assume 0 V = 0 A. If a true zero is required, the LMP8481 should be used with a VREF set slightly above ground (> 50 mV). See the *Swinging Output Below Ground* section for a possible solution to this issue.

8.3.9 Swinging Output Below Ground

If a negative supply is available, a pulldown resistor can be added from the output to the negative voltage to allow the output to swing a few millivolts below ground. This will now allow the ADC to resolve true zero and recover codes that would normally be lost to the negative output saturation limit.

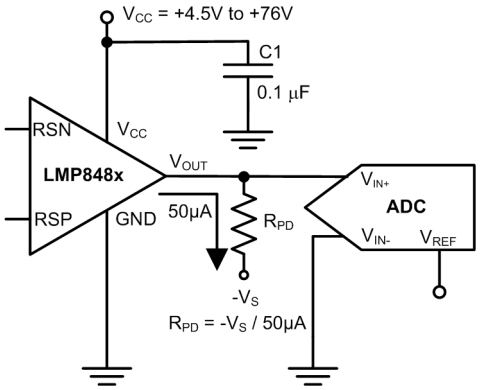


Figure 26. Output Pulldown Resistor Example

A minimum of 50 µA should be sourced (“pulled”) from the output to a negative voltage. The pulldown resistor can be calculated from:

$$R_{PD} = -V_S/50\ \mu A \quad (8)$$

For example, if a –5-V supply is available, a pulldown resistor of 5 V/50 µA = 100 kΩ should be used. This will allow the output to swing to about 10 mV below ground.

This technique may also reduce the maximum positive swing voltage. Do not forget to include the parallel loading effects of the pulldown any output load. TI recommends not to exceed –100 mV on the output. Source currents greater than 100 µA should be avoided to prevent self-heating at high-supply voltages. Pulldown resistor values should not be so low as to heavily load the output during positive output excursions. This mode of operation is not directly specified and is not ensured.

Feature Description (continued)

8.3.10 Maximum Output Voltage

The LMP8481 has an internal precision 14-V low-dropout regulator which limits the maximum amplifier output swing to about 250 mV below V_{CC} or 13.7 V (whichever is less). This effectively clamps the maximum output to slightly less than 13.7 V even with a V_{CC} greater than 14 V. See *Typical Application With Resistive Divider* for more information.

8.4 Device Functional Modes

8.4.1 Unidirectional vs Bidirectional Operation

Unidirectional operation is where the load current only flows in one direction (V_{SENSE} is always positive). Application examples would be PA monitoring, non-inductive load monitoring and laser or LED drivers. This allows the output zero reference to be true zero volts on the output. The LMP8480 is designed for unidirectional applications where the setting of VREF is not required. See the *Unidirectional Application With LMP8480* for more details.

Bidirectional operation is where the load current can flow in both directions (V_{SENSE} can be positive or negative). Application examples would be battery-charging or regenerative motor monitoring. The LMP8481 is designed for bidirectional applications and has a pair of VREF pins to allow the setting of the output zero reference level (V_{REF}). See the *Unidirectional Application With LMP8480* section for more details.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LMP848x amplifies the voltage developed across a current-sensing resistor when current passes through it. Flexible offset inputs allow adjusting the functionality of the output for multiple configurations, as discussed throughout this section.

9.1.1 Input Common-Mode and Differential Voltage Range

The input common-mode range, where "common-mode range" is defined as the voltage from ground to the voltage on R_{SP} input, should be in the range of 4.0 V to 76 V. Operation below 4.0 V on either input pin will introduce severe gain error and nonlinearities.

The maximum differential voltage (defined as the voltage difference between R_{SP} and R_{SN}) should be 667 mV or less. The theoretical maximum input is 700 mV (14 V / 20).

Taking the inputs below 4 V will not damage the device, but the output conditions during this time are not predictable and are not ensured.

If the load voltage (Vcm) is expected to fall below 4 V as part of normal operation, preparations must be made for invalid output levels during this time.

9.2 Typical Applications

9.2.1 Unidirectional Application With LMP8480

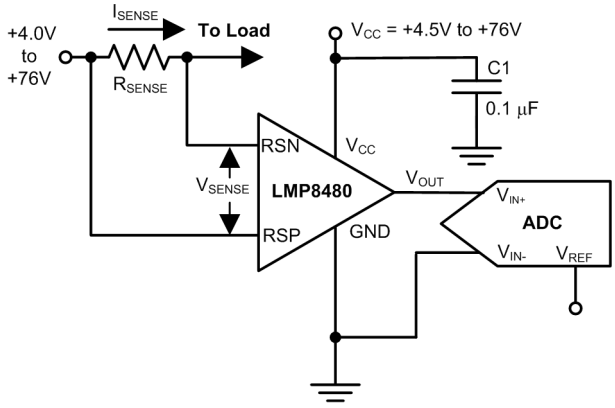


Figure 27. Unidirectional Application with LMP8480

9.2.1.1 Design Requirements

The LMP8480 is designed for unidirectional current sense applications. The output of the amplifier will be equal to the differential input voltage times the fixed device gain.

9.2.1.2 Detailed Design Procedure

The output voltage can be calculated from:

$$VOUT = ((V_{RSP} – V_{RSN}) \times Av) \quad (9)$$

Typical Applications (continued)

It should be noted that the minimum “zero” reading will be limited by the lower output swing and input offset. The LMP8480 is functionally identical to the LMP8481, but with the V_{REFA} and V_{REFB} nodes grounded internally. The LMP8481 can replace the LMP8480 if both the V_{REF} inputs (pins 6 and 7) are grounded.

9.2.1.3 Application Curve

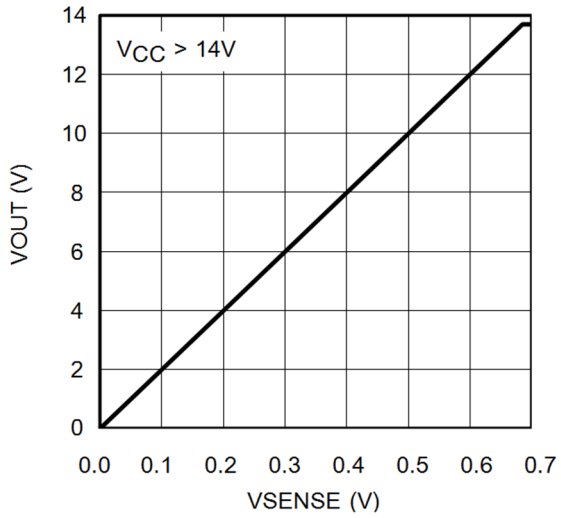


Figure 28. Unidirectional Transfer Function for Gain-of-20 Option

9.2.2 Bidirectional Current Sensing Using LMP8481

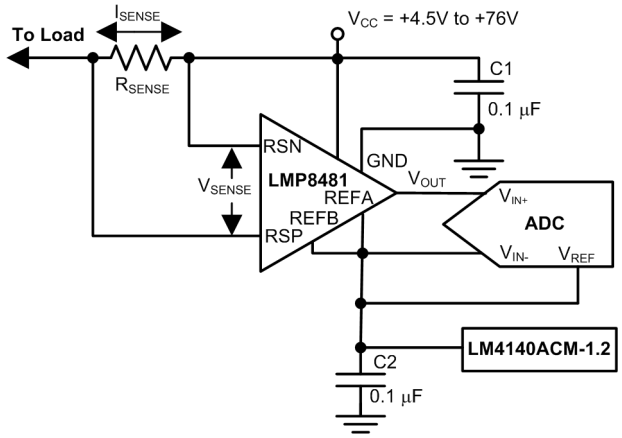


Figure 29. Bidirectional Current Sensing Using LMP8481

9.2.2.1 Design Requirements

Bidirectional operation is required where the measured load current can be positive or negative. Because V_{SENSE} can be positive or negative, and the output cannot swing negative, the “zero” output level must be level-shifted above ground to a known zero reference point. The LMP8481 allows for the setting this reference point.

9.2.2.2 Detailed Design Procedure

The V_{REFA} and V_{REFB} pins set the zero reference point. The output “zero” reference point is set by applying a voltage to the REFA and/or REFB pins. See the *Unidirectional Application With LMP8480* section. *V_{REFA} and V_{REFB} Pins (LMP8481 Only)* shows the output transfer function with a 1.2-V reference applied to the Gain-of-20 option.

Typical Applications (continued)

9.2.2.3 Application Curve

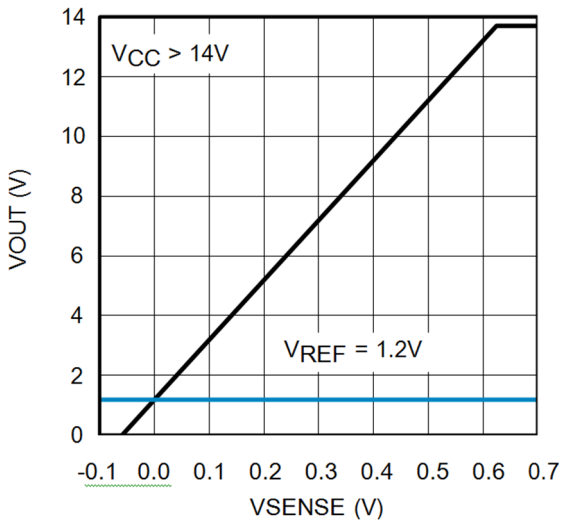


Figure 30. Bidirectional Transfer Function Using 1.2-V Reference Voltage

9.2.3 Typical Application With Resistive Divider

Take care if the output is driving an A/D input with a maximum A/D maximum input voltage lower than the amplifier supply voltage, as the output can swing higher than the planned load maximum due to input transients or shorts on the load and overload or possibly damage the A/D input.

A resistive attenuator, as shown in Figure 31, can be used to match the maximum swing to the input range of the A/D.

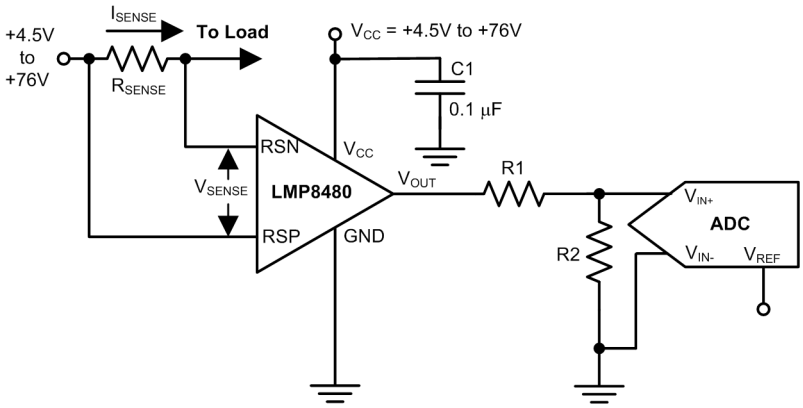


Figure 31. Typical Application With Resistive Divider Example

10 Power Supply Recommendations

10.1 Power Supply Decoupling

In order to decouple the LMP848x from AC noise on the power supply, TI recommends using a 0.1-µF bypass capacitor between the V_{CC} and GND pins. This capacitor should be placed as close as possible to the supply pins. In some cases, an additional 10-µF bypass capacitor may further reduce the supply noise.

Do not forget that these bypass capacitors must be rated for the full supply and / or load source voltage. TI recommends that the working voltage of the capacitor (WVDC) should be at least two times the maximum expected circuit voltage.

11 Layout

11.1 Layout Guidelines

The traces leading to and from the sense resistor can be significant error sources. With small value sense resistors (< 100 mΩ), any trace resistance shared with the load current can cause significant errors.

The amplifier inputs should be directly connected to the sense resistor pads using “Kelvin” or “4-wire” connection techniques. The traces should be one continuous piece of copper from the sense resistor pad to the amplifier input pin pad, and ideally on the same copper layer with minimal vias or connectors. This can be important around the sense resistor if it is generating any significant heat gradients.

To minimize noise pickup and thermal errors, the input traces should be treated as a differential signal pair and routed tightly together with a direct path to the input pins. The input traces should be run away from noise sources, such as digital lines, switching supplies or motor drive lines. Remember that these traces can contain high voltage, and should have the appropriate trace routing clearances.

Since the sense traces only carry the amplifier bias current (about 7 µA at room temperature), the connecting input traces can be thinner, signal level traces. Excessive Resistance in the trace should also be avoided.

The paths of the traces should be identical, including connectors and vias, so that these errors will be equal and cancel.

The sense resistor will heat up as the load increases. As the resistor heats up, the resistance generally goes up, which will cause a change in the readings The sense resistor should have as much heatsinking as possible to remove this heat through the use of heatsinks or large copper areas coupled to the resistor pads. A reading drifting over time after turn-on can usually be traced back to sense resistor heating.

11.2 Layout Example

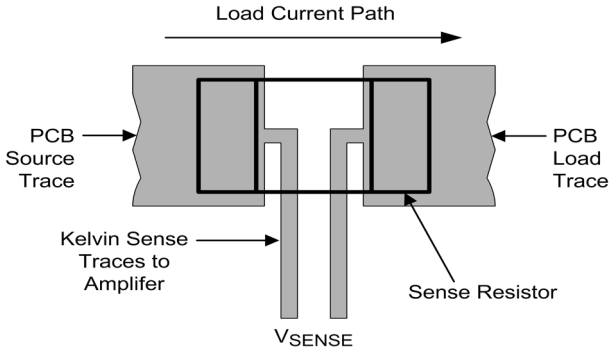


Figure 32. “Kelvin” or “4–wire” Connection to the Sense Resistor

12 器件和文档支持

12.1 器件支持

12.1.1 开发支持

《LMP8480/1 PSPICE 模型》，SNVM046

《LMP8480/1 TINA 参考设计》，SNVM048

TINA-TI 基于 SPICE 的模拟仿真程序，http://www.ti.com.cn/tool/cn/tina-ti

LMP8480/1 评估板，产品页

《LMP8480/1 评估板手册》，SNOU031

12.2 相关链接

以下表格列出了快速访问链接。 范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 2. 相关链接

器件	产品文件夹	样片与购买	技术文章	工具与软件	支持与社区
LMP8480	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
LMP8481	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMP8480MM-T/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AV8A	Samples
LMP8480MME-S/NOPB	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AY8A	Samples
LMP8480MME-T/NOPB	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AV8A	Samples
LMP8480MMX-S/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AY8A	Samples
LMP8480MMX-T/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AV8A	Samples
LMP8481MM-H/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AH9A	Samples
LMP8481MM-S/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AA9A	Samples
LMP8481MM-T/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AT9A	Samples
LMP8481MME-H/NOPB	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AH9A	Samples
LMP8481MME-S/NOPB	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AA9A	Samples
LMP8481MME-T/NOPB	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AT9A	Samples
LMP8481MMX-H/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AH9A	Samples
LMP8481MMX-S/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AA9A	Samples
LMP8481MMX-T/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AT9A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

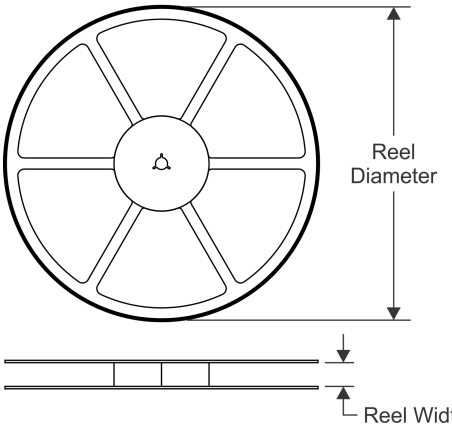
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

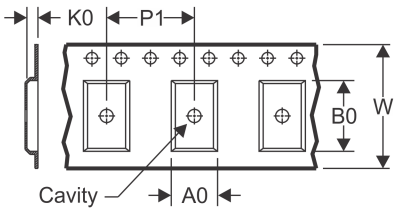
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

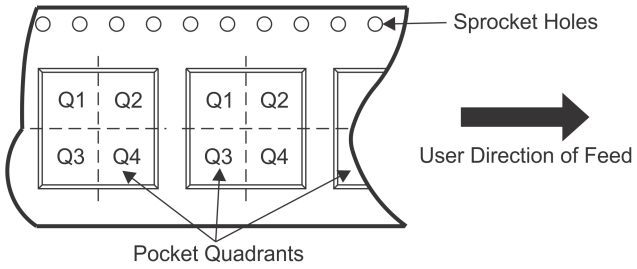


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

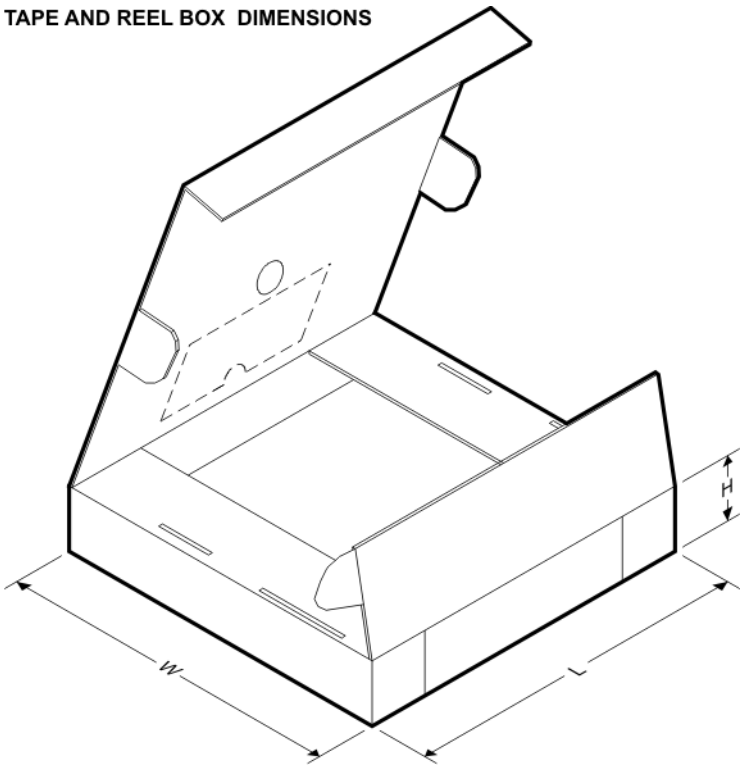
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMP8480MM-T/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP8480MME-S/NOPB	VSSOP	DGK	8	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP8480MME-T/NOPB	VSSOP	DGK	8	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP8480MMX-S/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP8480MMX-T/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP8481MM-H/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP8481MM-S/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP8481MM-T/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP8481MME-H/NOPB	VSSOP	DGK	8	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP8481MME-S/NOPB	VSSOP	DGK	8	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP8481MME-T/NOPB	VSSOP	DGK	8	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP8481MMX-H/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP8481MMX-S/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP8481MMX-T/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

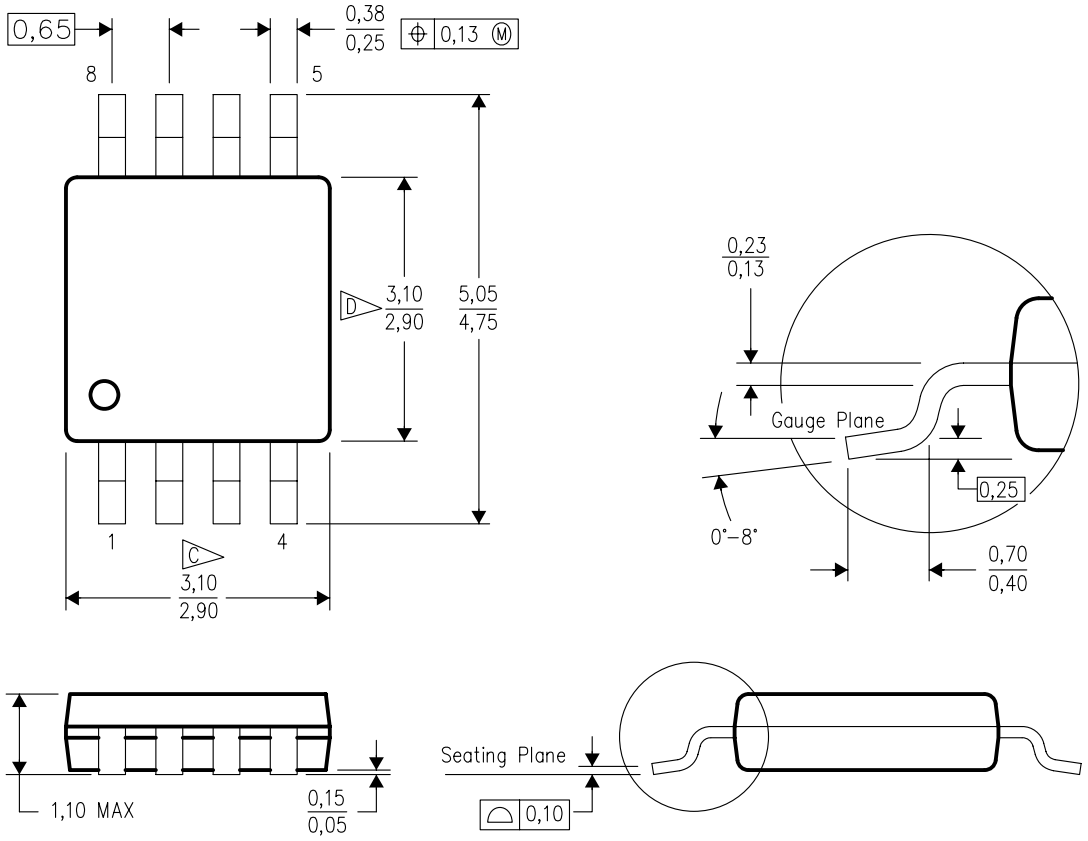
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMP8480MM-T/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMP8480MME-S/NOPB	VSSOP	DGK	8	250	210.0	185.0	35.0
LMP8480MME-T/NOPB	VSSOP	DGK	8	250	210.0	185.0	35.0
LMP8480MMX-S/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMP8480MMX-T/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMP8481MM-H/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMP8481MM-S/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMP8481MM-T/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMP8481MME-H/NOPB	VSSOP	DGK	8	250	210.0	185.0	35.0
LMP8481MME-S/NOPB	VSSOP	DGK	8	250	210.0	185.0	35.0
LMP8481MME-T/NOPB	VSSOP	DGK	8	250	210.0	185.0	35.0
LMP8481MMX-H/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMP8481MMX-S/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMP8481MMX-T/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



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NOTES:
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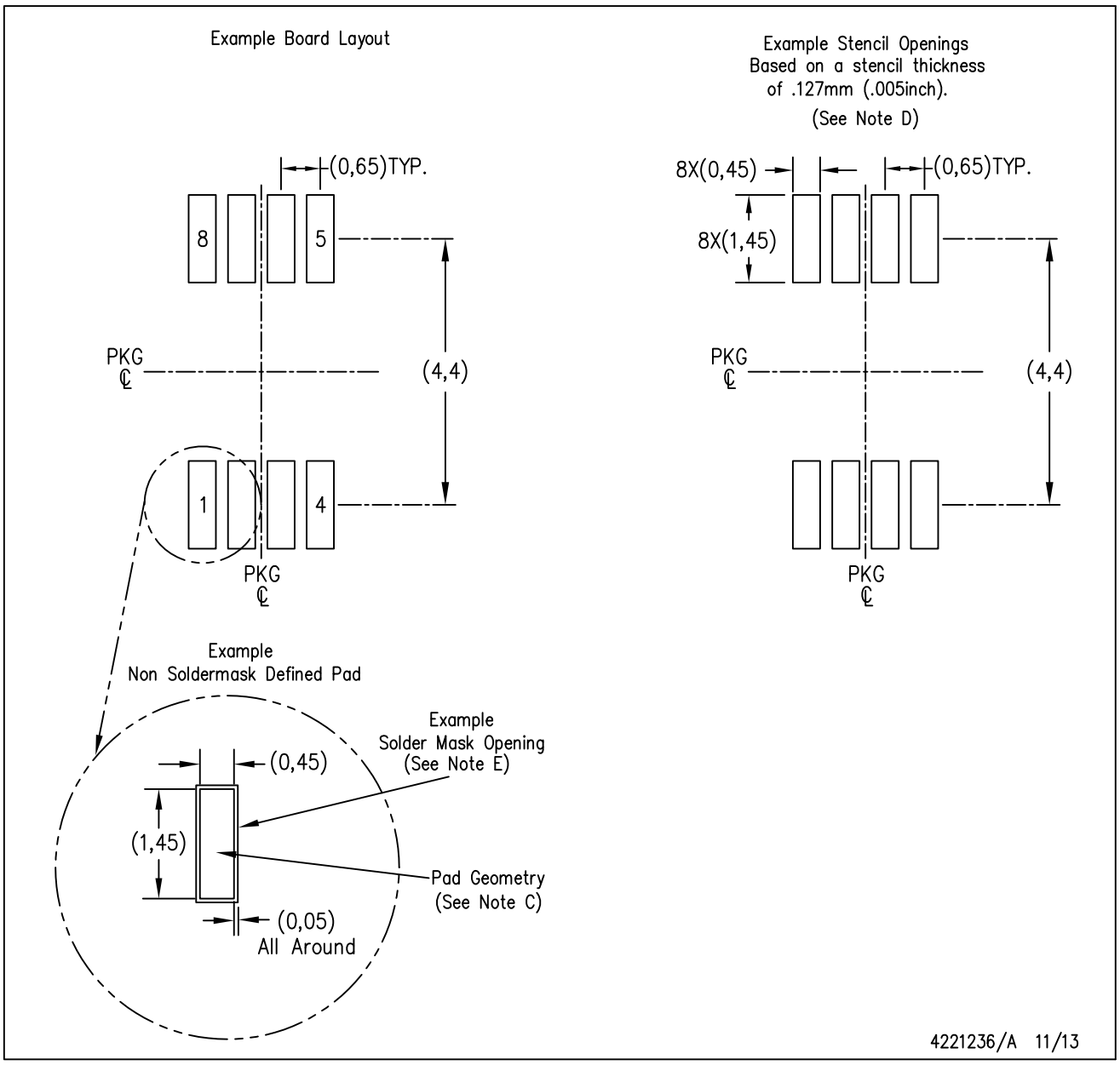
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265