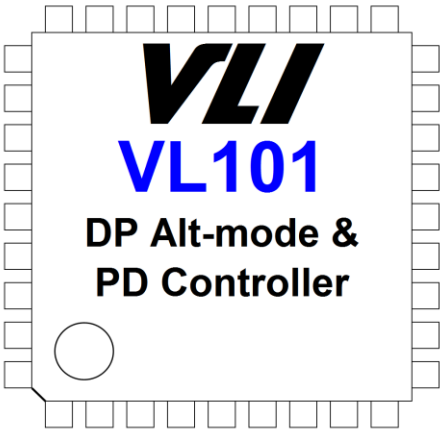
VIA Labs, Inc.

Data Sheet

VL101
Enhanced DP Alt-mode & PD
Controller for USB-C Devices

Dec. 21, 2015
Revision 0.8



VIA Labs, Inc.
www.via-labs.com

7F, 529-1, Chung-Cheng Road,
Hsin-Tien, New Taipei City 231, Taiwan
Tel: (886-2) 2218-1838
Fax: (886-2) 2218-8924
Email: sales@via-labs.com.tw

Revision History

Rev	Date	Initial	Note
0.7	11/11/2015	HC	Preliminary release
0.8	12/21/2015	HC	Adding Electrical spec

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Product Features

VL101

Enhanced DisplayPort Alt-mode & PD Controller for USB-C Devices

- **CC Logic & PD Engine supporting one charging UFP and one DRP**
  - Compliant to USB Type-C Cable and Connector Specification Revision 1.1
  - Compliant to USB Power Delivery Specification Revision 2.0 Version 1.1
  - Integrated Type-C transceivers, supporting one charging UFP and one DRP
  - Built-in pull-up/pull down resistors, including Rp, Rd, and Ra
- **DP Alt-mode Configuration**
  - Compliant to VESA DisplayPort Alt Mode on USB Type-C Standard Version 1.0a
  - DP mode Discovery/Enter/Exit
  - DP configure & status update
  - DP source/sink connection detection
  - Built-in Aux_CH switch
- **USB-C Charging UFP Capability**
  - Charging connected PD hosts once external power is available
  - Support Provider and Consumer roles
  - Support up to PD power Profile 5 as Source
  - Support charging dead battery
- **USB-C DRP Capability**
  - Support Provider and Consumer roles
  - Support up to PD power Profile 5 as Sink and 5V up to 3A as Source
- **USB Billboard Device**
  - Compliant to USB Device Class Definition for Billboard Devices Revision 1.1
  - Integrated in-house USB2.0 PHY
- **Fast 8051 Macro cell 80C32-Compatible Microcontroller**
  - Standard 1T 8051 instruction set
  - Embedded Mask ROM and SRAM
  - Support external SPI flash for firmware upgrade
- **Built-in Voltage Regulators and Voltage Detector**
  - 5.0V to 3.3V LDO & 3.3V to 1.8V LDO
  - 5.0V to 1.8V/1.2V DC-DC to supply power for video converter
  - Auto power source selection between Vbus and Vconn
  - Vbus Voltage Detector for both USB-C ports
- **GPIOs for Special Function and Control**
  - 11 GPIOs in QFN48 and 7 GPIOs in QFN40 for application customization
  - One I^2C master interface
- **Physical**
  - QFN 48 green package (6x6x0.85 mm) for two USB-C ports
  - QFN 40 green package (5x5x0.85 mm) for one USB-C port
- **Certification**
  - TBD
- **Applications**
  - USB-C video adapters
  - USB-C Multi-function docks
  - USB-C TV, monitor, and projector

VL101 System Overview

VIA Lab's VL101 is a highly integrated single chip DisplayPort Alternate mode and Power Delivery controller for USB-C devices that designed for applications like USB-C video adapters, USB-C TV/monitor/projector, and USB-C multi-function docking stations. Integrated USB-C charging UFP, VL101 can perform DP alt-mode video out functionality and simultaneously enable charging connected PD host once external power is detected. Integrated USB-C DRP can either connect to USB-C power adapter to charge PD host or connect to USB-C devices to do data transfer. VL101's Device Policy Manager could negotiate power profiles with PD engine on USB-C power adapter (source) and PD engine on connected PD host (sink) then enable power charging-through. Charging a host under dead battery mode is supported as well. SBU1/SBU2 switch is built-in to support USB-C cable flipping feature. USB Billboard device is implemented to meet "VESA DP Alt-Mode on USB Type-C" spec.

Built-in required linear voltage regulators and power source detector, VL101 can work perfectly with power input either from Vconn power or from Vbus power. Built-in 5V to 1.8V/1.2V DC-DC converter is designed to provide core power for video converter to save BOM. Up to 11 GPIO pins and two voltage detector pins are available for port power detection, power discharge control, power switch control, data switch control, or other special application usage. The SPI interface can support external flash for firmware upgrades through USB Billboard device. VL101 is available in QFN 48L (6x6x0.85 mm) and QFN 40L (5x5x0.85 mm) green packages to fit small form-factor design.

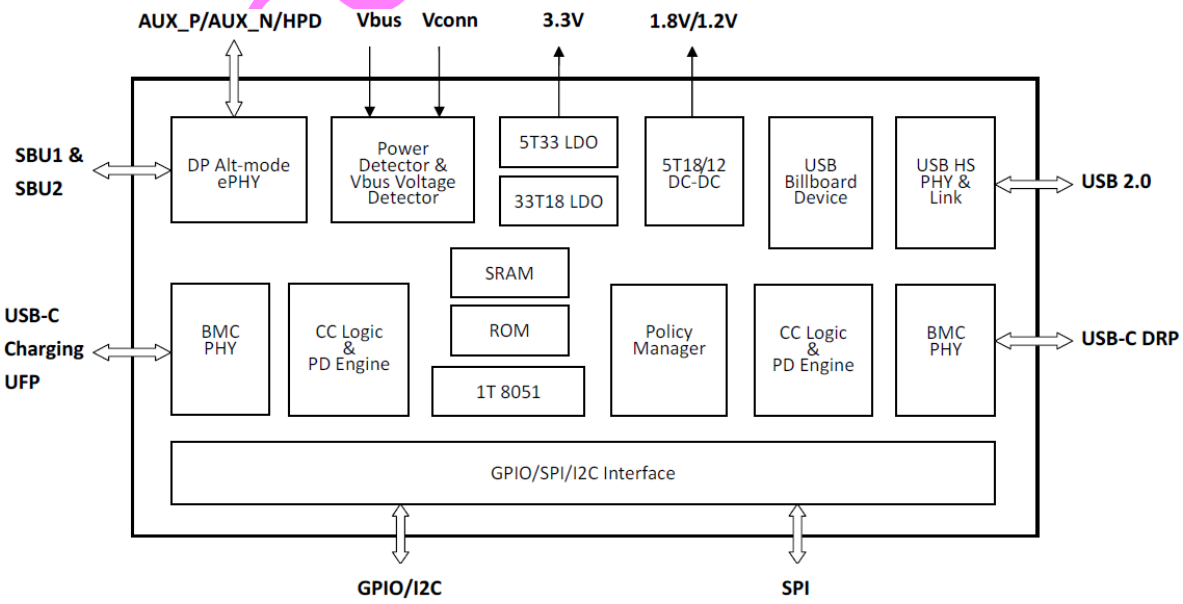


Figure 1 – VL101 Block Diagram

Typical Applications

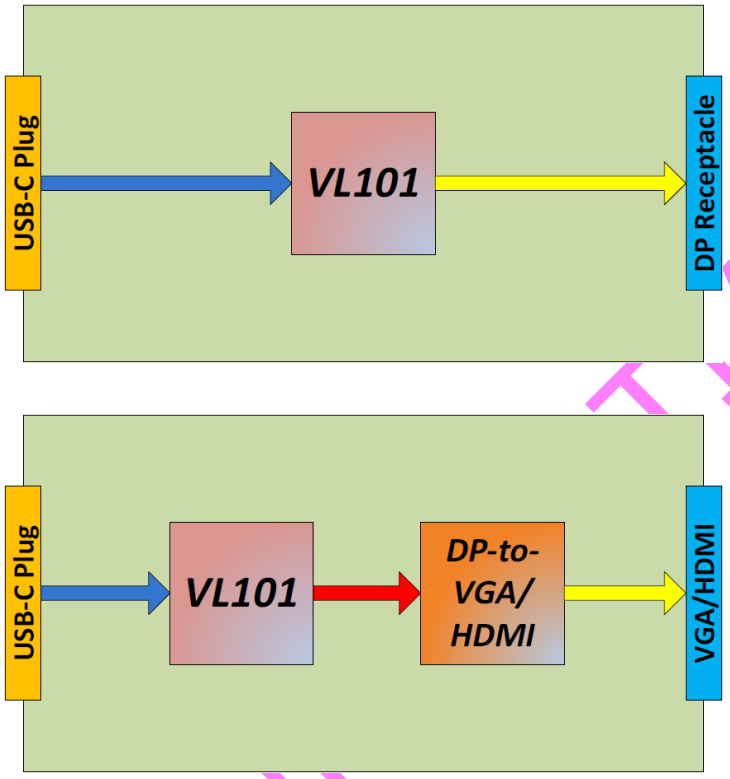


Figure 2 – Generic VL101 USB-C Video Adapters

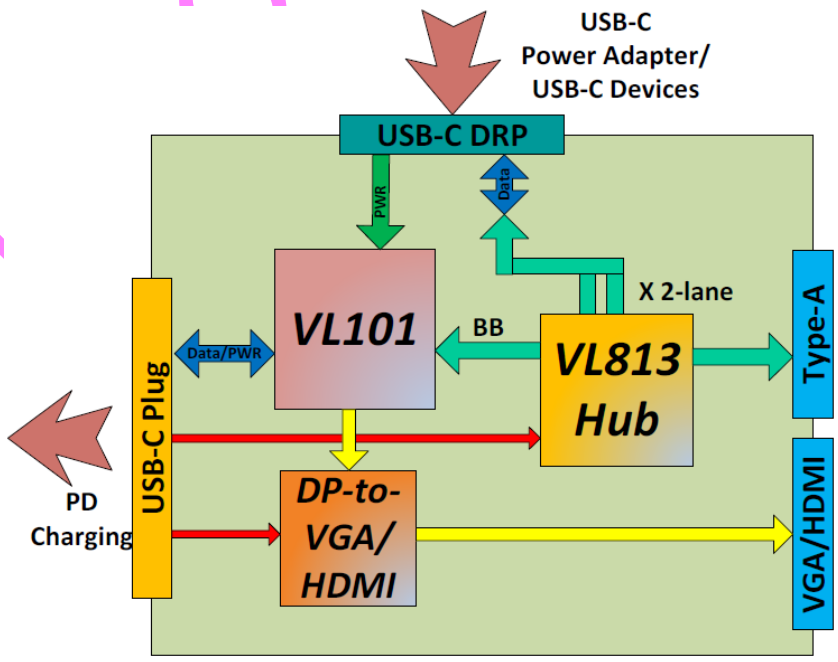


Figure 3 – VL101 USB-C Video Adapters with Hub and PD Charging-Thru

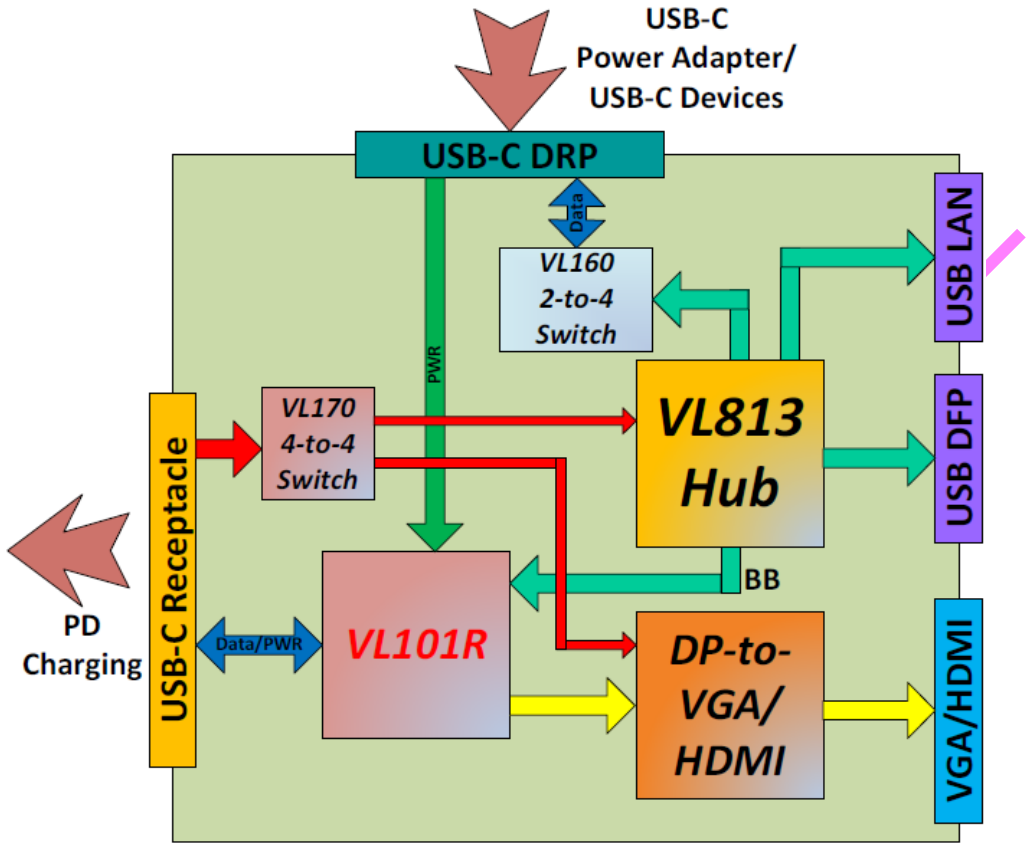


Figure 4 – VL101 USB-C Multi-function Dock

Pinout

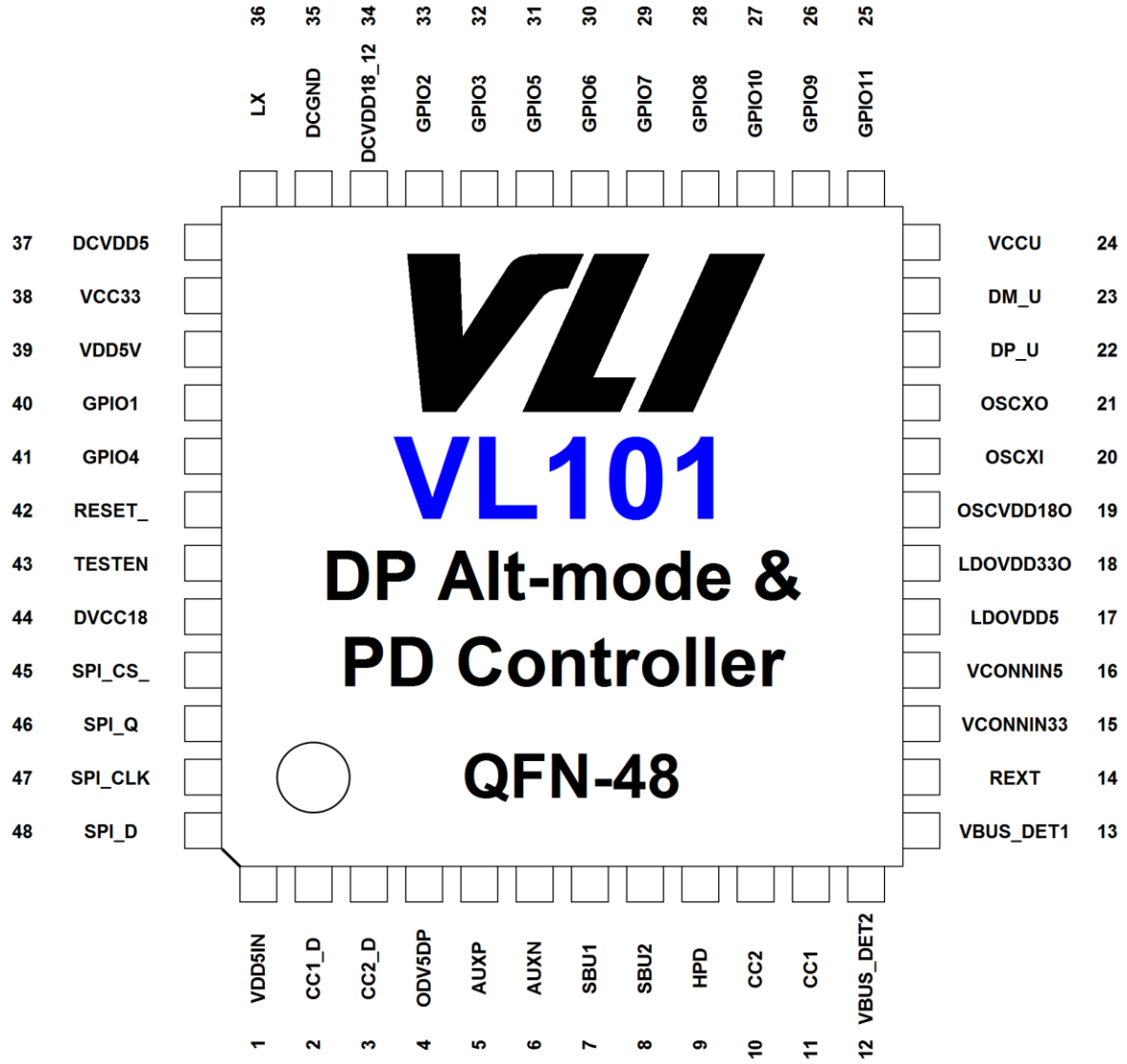


Figure 5 – VL101 QFN-48 Pin Diagram

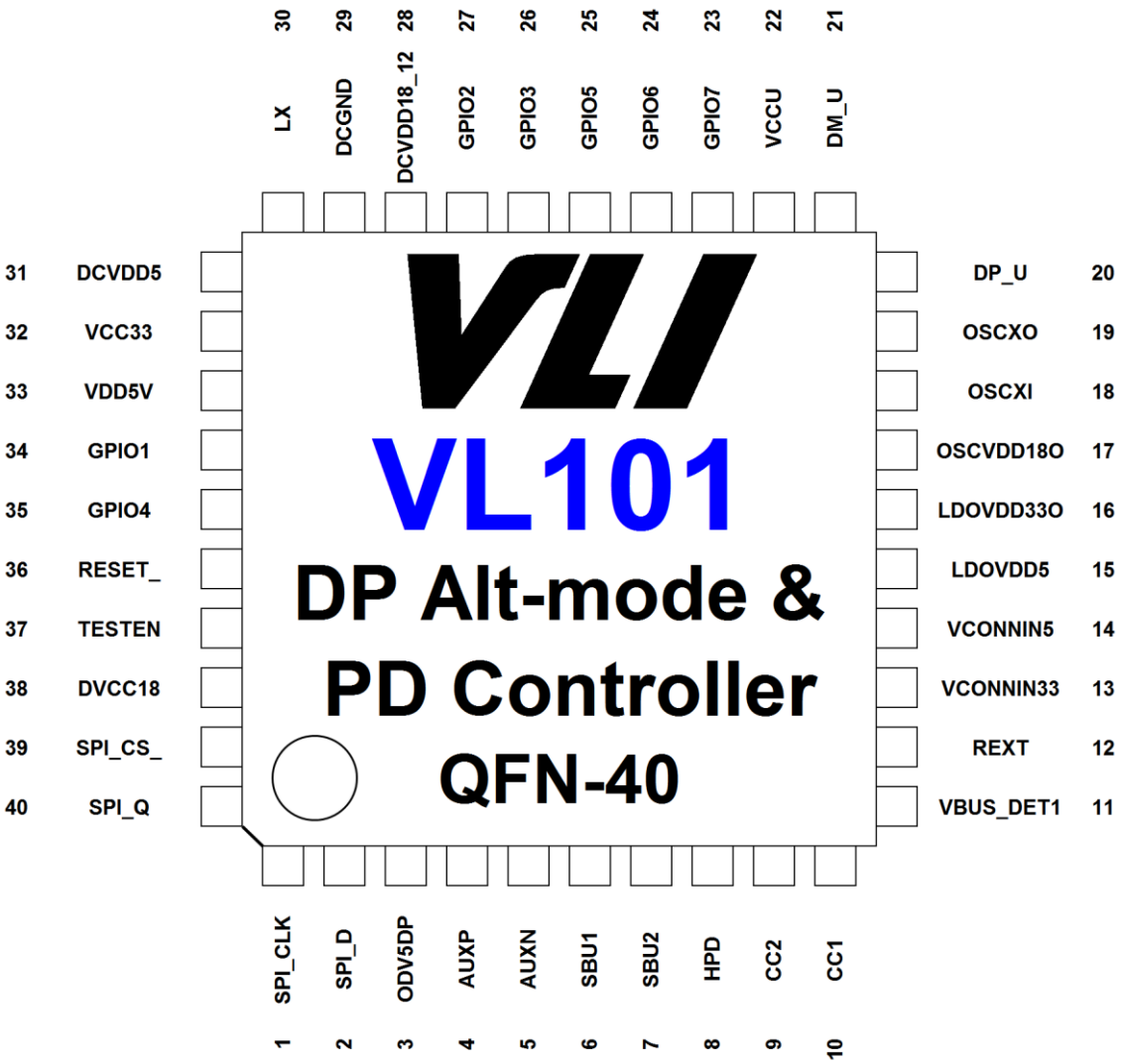


Figure 6 – VL101 QFN-40 Pin Diagram

Pin List

Table 1 – VL101 QFN-48 Pin List

Pin	Pin Name	Pin	Pin Name
1	VDD5IN	25	GPIO11
2	CC1_D	26	GPIO9
3	CC2_D	27	GPIO10
4	ODV5DP	28	GPIO8
5	AUXP	29	GPIO7
6	AUXN	30	GPIO6
7	SBU1	31	GPIO5
8	SBU2	32	GPIO3
9	HPD	33	GPIO2
10	CC2	34	DCVDD18_12
11	CC1	35	DCGND
12	VBUS_DET2	36	LX
13	VBUS_DET1	37	DCVDD5
14	REXT	38	VCC33
15	VCONNIN33	39	VDD5V
16	VCONNIN5	40	GPIO1
17	LDOVDD5	41	GPIO4
18	LDOVDD33O	42	RESET_
19	OSCVDD18O	43	TESTEN
20	OSCXI	44	DVCC18
21	OSCXO	45	SPI_CS_
22	DP_U	46	SPI_Q
23	DM_U	47	SPI_CLK
24	VCCU	48	SPI_D

Table 2 – VL101 QFN-40 Pin List

Pin	Pin Name	Pin	Pin Name
1	SPI_CLK	21	DM_U
2	SPI_D	22	VCCU
3	ODV5DP	23	GPIO7
4	AUXP	24	GPIO6
5	AUXN	25	GPIO5
6	SBU1	26	GPIO3
7	SBU2	27	GPIO2
8	HPD	28	DCVDD18_12
9	CC2	29	DCGND
10	CC1	30	LX
11	VBUS_DET1	31	DCVDD5
12	REXT	32	VCC33
13	VCONNIN33	33	VDD5V
14	VCONNIN5	34	GPIO1
15	LDOVDD5	35	GPIO4
16	LDOVDD33O	36	RESET_
17	OSCVDD18O	37	TESTEN
18	OSCXI	38	DVCC18
19	OSCXO	39	SPI_CS_
20	DP_U	40	SPI_Q

Pin Descriptions

Signal Type Definition

Name	Type	Signal Description
Input	I	A standard input-only signal
Output	O	A standard active driver
Input/Output	I/O	A bi-directional signal
Analog bias	A_{BIAS}	Analog bias or reference signal. Must be tied to external resistor and/or capacitor bias network
Power	PWR	A power pin
Ground	GND	A ground pin

USB-C Interface

Pin Name	QFN48	QFN40	I/O	Signal Description
CC1	11	10	I/O	Charging UFP Configuration Channel 1
CC2	10	9	I/O	Charging UFP Configuration Channel 2
CC1_D	2	—	I/O	DRP Port Configuration Channel 1
CC2_D	3	—	I/O	DRP Port Configuration Channel 2
SBU1	7	6	I/O	Sideband Use 1
SBU2	8	7	I/O	Sideband Use 2

Billboard Interface

Pin Name	QFN48	QFN40	I/O	Signal Description
DP_U	22	20	I/O	USB 2.0 Bus Data Plus (D+)
DM_U	23	21	I/O	USB 2.0 Bus Data Minus (D–)

DP Alt-mode Interface

Pin Name	QFN48	QFN40	I/O	Signal Description
AUXP	5	4	I/O	DP AUX Channel Positive
AUXN	6	5	I/O	DP AUX Channel Negative
HPD	9	8	I	DP Hot Plug Detect

SPI Interface

Pin Name	QFN48	QFN40	I/O	Signal Description
SPI_CS_	45	39	O	Serial Flash Chip Enable
SPI_D	48	2	O	Serial Flash Data Input
SPI_Q	46	40	I	Serial Flash Data Output
SPI_CLK	47	1	O	Serial Flash Clock

Analog Command Block

Pin Name	QFN48	QFN40	I/O	Signal Description
OSCXI	20	18	I	24MHz Crystal Input
OSCXO	21	19	O	24MHz Crystal Output
REXT	14	12	A_{BIAS}	Connect to External Resistor (20.5K ohm, +/- 1% accuracy)
LDOVDD5	17	15	PWR	5V Input for 5V-to-3.3V LDO
LDOVDD33O	18	16	PWR	3.3V Output Pin for 5V-to-3.3V LDO
OSCVDD18O	19	17	PWR	Analog 1.8V Power Output
VCONNIN33	15	13	PWR	3.3V Vconn Power Input
VCONNIN5	16	14	PWR	5V Vconn Power Input
DCVDD5	37	31	PWR	5.0V Voltage Input for DC2DC Regulator
LX	36	30	O	1.2V/1.8V Voltage Output for DC2DC Regulator
DCGND	35	29	GND	Ground for DC2DC Regulator
DCVDD18_12	34	28	I	DC2DC Regulator Feedback Pin
VBUS_DET1	13	11	I	USB-C Charging UFP VBus Voltage Detector
VBUS_DET2	12	—	I	USB-C DRP Vbus Voltage Detector
VDD5IN	1	—	PWR	5V Power Input for Vconn Power Output
ODV5DP	4	3	O	Open-Drain IO for 5V Video Power Control

General Purpose I/O and Miscellaneous

Pin Name	QFN48	QFN40	I/O	Signal Description
RESET_	42	36	I	External Chip Reset
GPIO1	40	34	I/O	General Purpose I/O
GPIO2	33	27	I/O	General Purpose I/O
GPIO3	32	26	I/O	General Purpose I/O
GPIO4	41	35	I/O	General Purpose I/O
GPIO5	31	25	I/O	General Purpose I/O
GPIO6	30	24	I/O	General Purpose I/O
GPIO7	29	23	I/O	General Purpose I/O
GPIO8	28	—	I/O	General Purpose I/O
GPIO9	26	—	I/O	General Purpose I/O
GPIO10	27	—	I/O	General Purpose I/O
GPIO11	25	—	I/O	General Purpose I/O

Test Pin

Pin Name	QFN48	QFN40	I/O	Signal Description
TESTEN	43	37	I	Test Mode Enable Do not connect for normal operation. Internal pull down

Power and Ground

Pin Name	QFN48	QFN40	I/O	Signal Description
VDD5V	39	33	PWR	E-fuse Power Input
VCC33	38	32	PWR	Digital 3.3V IO Power Input
DVCC18	44	38	PWR	Digital 1.8V Core Power Input
VCCU	24	22	PWR	Analog 3.3V Power Input

Electrical Specification

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Note
T_{STG}	Storage Temperature	-55	125	°C	—
V_{DD33}	3.3V Power Input Voltage	-0.5	3.69	V	—
V_{DD50}	5V Power Input Voltage	-0.5	5.5	V	—
V_O	Output Voltage at any output	-0.5	VCC+ 0.5	V	—
V_{ESD}	Electrostatic Discharge	-2	2	kV	Human Body Model

Note: Stress above conditions may cause permanent damage to the device.
Functional operation of this device should be restricted to the conditions described.

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
LDOVDD5	5V to 3.3V LDO 5V Power Input	4.5	5	5.5	V
DCVDD5	5V to 1.8/1.2V DC2DC 5V Power Input	4.5	5	5.5	V
VCONNIN5	5V Vconn power input	4.5	5	5.5	V
VCONNIN33	3.3V Vconn power input	3.0	3.3	3.6	V
V_{CC33}	Digital IO power 3.3V	3.0	3.3	3.6	V
DV_{CC18}	Digital Core power 1.8V	1.62	1.8	1.98	V
DGND	Ground	—	0	—	V
T_A	Ambient Temperature	0		70	°C

General IO DC Characteristics

Symbol	Parameter	Min	Max	Unit	Note
V_{IL}	Input Low Voltage	-0.30	0.8	V	—
V_{IH}	Input High Voltage	2.0	3.6	V	—
V_{OL}	Output Low Voltage	—	0.4	V	IOL=15.8mA
V_{OH}	Output High Voltage	2.4	—	V	IOH=26.5mA
I_{IL}	Input Leakage Current	—	+/-10	μA	0<VIN<VCC
I_{OZ}	Tristate Leakage Current	—	+/-10	μA	0<VOUT<VCC

Internal 3.3V to 1.8V LDO Regulator

Parameter	Min	Typ.	Max	Unit	Note
Input Voltage	3.0	3.3	3.6	V	
Output Voltage	1.71	1.8	1.89	V	
Max. Output Current			100	mA	
Output Voltage Tolerance		+/- 5%			

Internal 5V to 3.3V LDO Regulator

Parameter	Min	Typ.	Max	Unit	Note
Input Voltage	4.5	5.0	5.5	V	
Output Voltage	3.135	3.3	3.465	V	
Max. Output Current			100	mA	
Output Voltage Tolerance		+/- 5%			

Internal 5V to 1.8V/1.2V DC-DC Converter Regulator

Parameter	Min	Typ.	Max	Unit	Note
Input Voltage	4.5	5.0	5.5	V	
Output Voltage (1.8V)	1.71	1.8	1.89	V	
Output Voltage (1.2V)	1.14	1.2	1.26		
Max. Output Current			500	mA	
Output Voltage Tolerance		+/- 5%			

PD BMC DC/AC Characteristics

Symbol	Parameter	Min	Max	Unit	Note
$V_{BMCSWING}$	Voltage Swing	1.05	1.2	V	—
Z_{BMCDRV}	Drive Output Resistance	33	75	Ω	—
T_{BMCR}	Rise Time	300		ns	—
T_{BMCF}	Fall Time	300		ns	—

USB Full Speed DC/AC Characteristics

Symbol	Parameter	Min	Max	Unit	Note
V_{FSIH}	Full-speed Input High	2.0		V	—
V_{FSIL}	Full-speed Input Low		0.8	V	—
V_{FSCM}	Differential Common Mode Voltage	0.8	2.5	V	—
V_{FSOL}	Full-speed Output Low	0.0	0.3	V	—
V_{FSOH}	Full-speed Output High	2.8	3.6	V	—
T_{FSR}	Full-speed Rise Time	4	20	ns	—
T_{FSF}	Full-speed Fall Time	4	20	ns	—
V_{FSCRS}	Full-speed Output Signal Crossover Voltage	1.3	2.0	V	—

USB High Speed DC/AC Characteristics

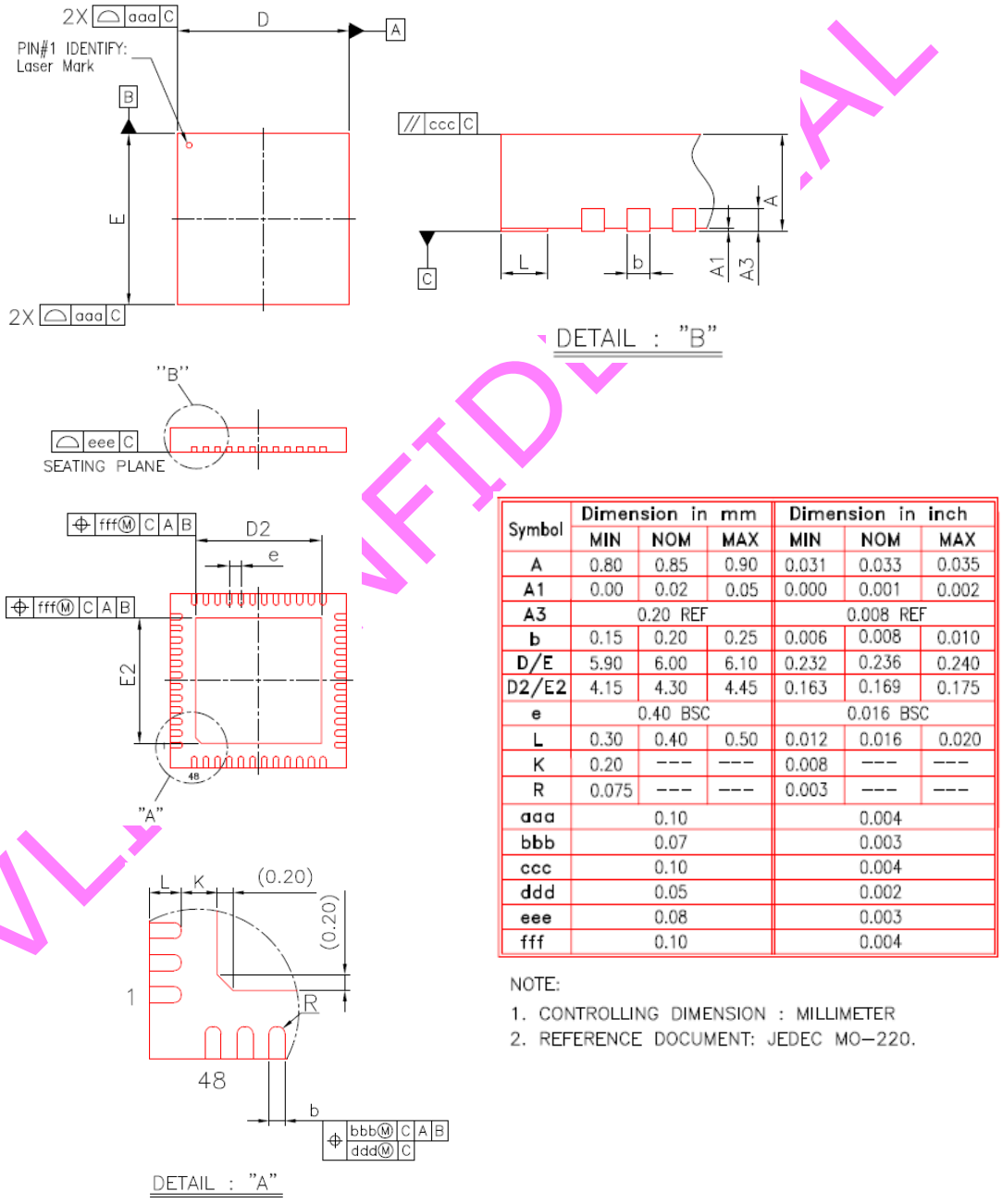
Symbol	Parameter	Min	Max	Unit	Note
V_{HSSQ}	High-speed squelch detection threshold	100	150	mV	—
V_{HSCM}	High-speed data signaling common mode voltage	-50	500	mV	—
V_{HSOI}	High-speed idle level	-10	10	mV	—
V_{HSOH}	High-speed data high	360	440	mV	—
V_{HSOL}	High-speed data low	-10	10	mV	—
V_{CHIRPJ}	Chirp J level	700	1100	mV	—
V_{CHIRPK}	Chirp K level	-900	-500	mV	—

Z_{HSDRV}	Drive output resistance	40.5	49.5	Ω	—
T_{HSR}	High-speed Rise Time	500		ps	—
T_{HSF}	High-speed Fall Time	500		ps	—

Package Mechanical Specifications

QFN-48 Pb-free Maximum Temperature for IR Reflow

Parameter	Value	Unit
Maximum Temperature Tp	250	°C
Max Time within 5°C of Tp	30	seconds



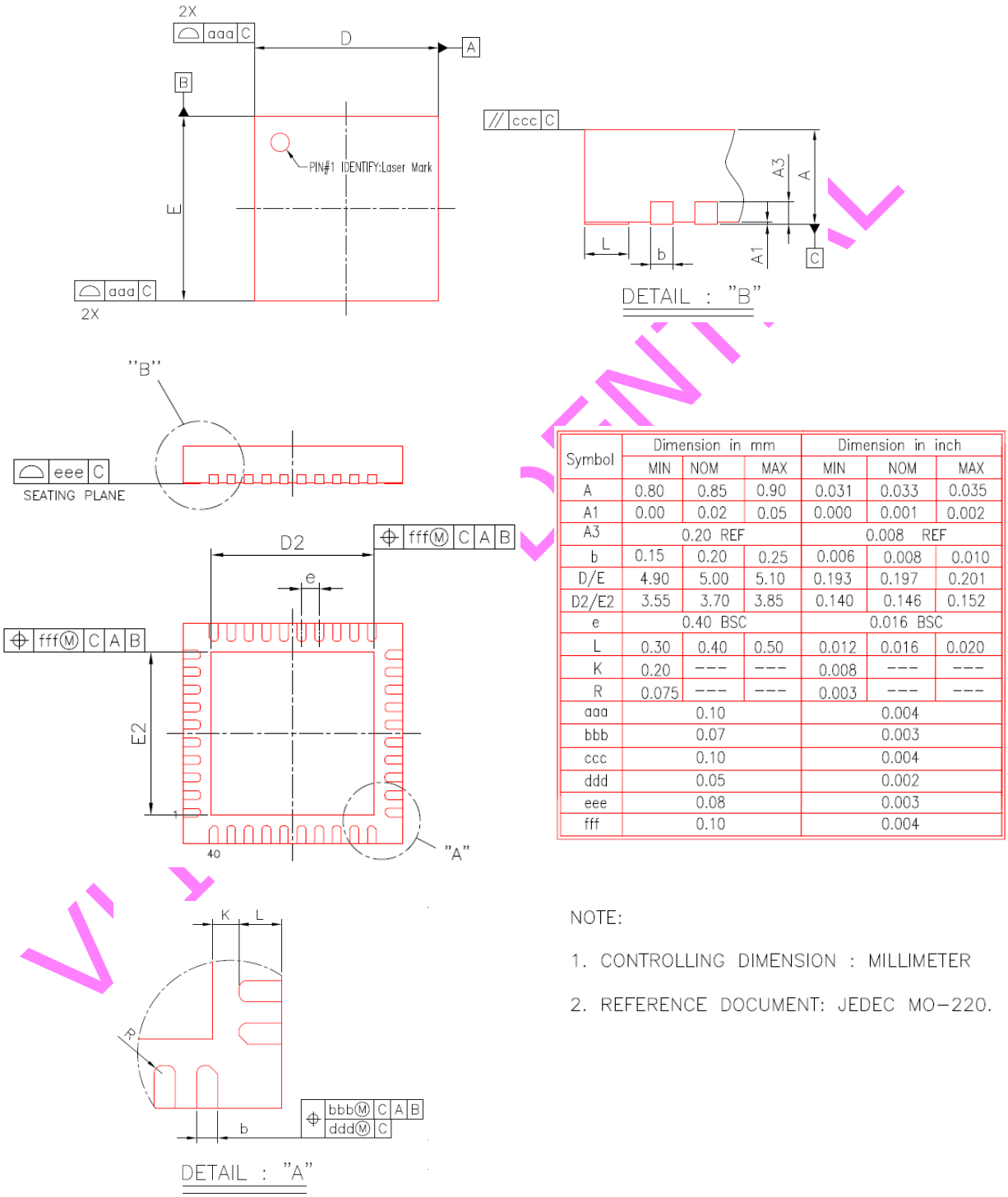
Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	5.90	6.00	6.10	0.232	0.236	0.240
D2/E2	4.15	4.30	4.45	0.163	0.169	0.175
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
K	0.20	---	---	0.008	---	---
R	0.075	---	---	0.003	---	---
aaa	0.10			0.004		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

NOTE:
1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT: JEDEC MO-220.

Figure 7 – QFN 48L 6x6x0.85 mm Mechanical Specification

QFN-40 Pb-free Maximum Temperature for IR Reflow

Parameter	Value	Unit
Maximum Temperature Tp	250	°C
Max Time within 5°C of Tp	30	Seconds



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3		0.20 REF			0.008 REF	
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	4.90	5.00	5.10	0.193	0.197	0.201
D2/E2	3.55	3.70	3.85	0.140	0.146	0.152
e		0.40 BSC			0.016 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020
K	0.20	---	---	0.008	---	---
R	0.075	---	---	0.003	---	---
aaa		0.10			0.004	
bbb		0.07			0.003	
ccc		0.10			0.004	
ddd		0.05			0.002	
eee		0.08			0.003	
fff		0.10			0.004	

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT: JEDEC MO-220.

Figure 8 – QFN 40L 5x5x0.85 mm Mechanical Specification

Package Top Side Marking

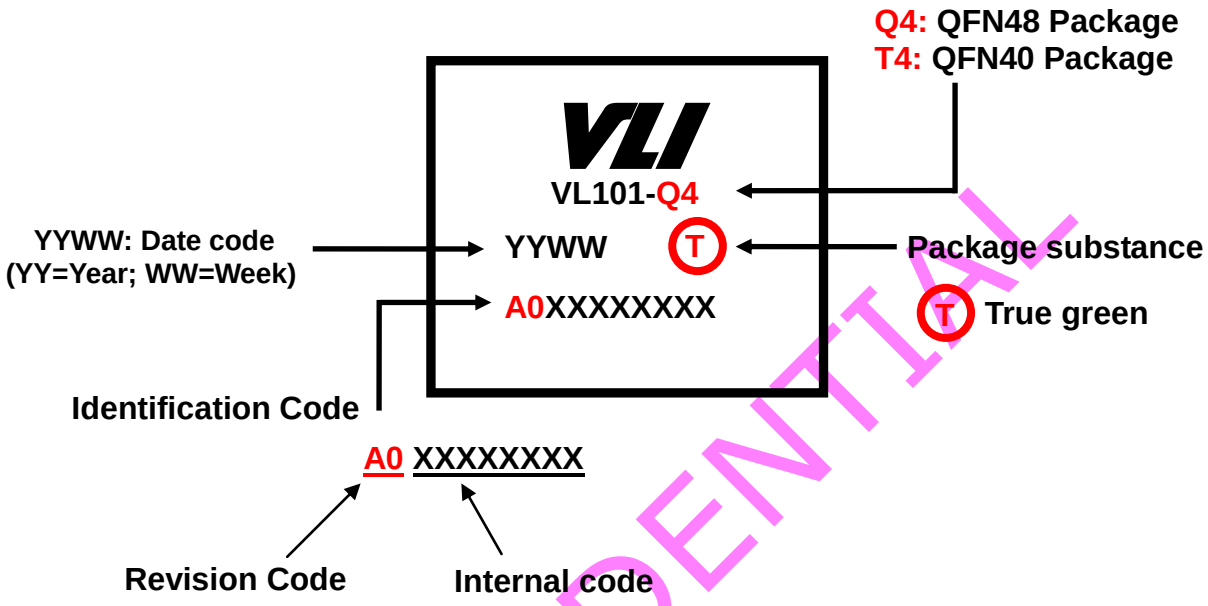


Figure 9 – VL101 Package Top Side Marking

Ordering Information

Part Number	Description	Package
VL101-T4	**USB-C Alt-Mode Accessory w/ Captive Cable** (One charging UFP only; UFP CC2 bonding to Ra)	40-pin QFN (5x5mm)
VL101-Q4	**USB-C Charging-Through w/ Captive Cable** (One charging UFP and one DRP; UFP CC2 bonding to Ra)	48-pin QFN (6x6mm)
VL101R-Q4	**USB-C Charging-Through w/ USB-C Receptacle** (One charging UFP and one DRP; UFP CC2 bonding to Rd)	48-pin QFN (6x6mm)

VIA Labs, Inc.
www.via-labs.com

7F, 529-1, Chung-Cheng Road,
Hsin-Tien, New Taipei City, Taiwan
Tel: (886-2) 2218-1838
Fax: (886-2) 2218-8924
Email: sales@via-labs.com.tw