ISL8483E, ISL8485E

ESD Protected to ±15kV, 5V, Low Power, High Speed or Slew Rate Limited RS-485/RS-422 Transceivers

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The ISL8483E and ISL8485E are ESD protected, BiCMOS 5V powered, single transceivers that meet both the RS-485 and RS-422 standards for balanced communication. Each driver output/receiver input is protected against ±15kV ESD strikes, without latch-up. Unlike competitive devices, this Intersil family is specified for 10% tolerance supplies (4.5V to 5.5V).

The ISL8483E uses slew rate limited drivers which reduce EMI and minimize reflections from improperly terminated transmission lines or unterminated stubs in multidrop and multipoint applications.

Data rates up to 10Mbps are achievable by using the ISL8485E, which features higher slew rates.

Both devices present a “single unit load” to the RS-485 bus, which allows up to 32 transceivers on the network.

Receiver (Rx) inputs feature a “fail-safe if open” design, which ensures a logic high Rx output if Rx inputs are floating.

Driver (Tx) outputs are short-circuit protected, even for voltages exceeding the power supply voltage. Additionally, on-chip thermal shutdown circuitry disables the Tx outputs to prevent damage if power dissipation becomes excessive.

These half duplex configurations multiplex the Rx inputs and Tx outputs to allow transceivers with Rx and Tx disable functions in 8 Ld packages.

Related Literature

- For a full list of related documents, visit our website
  - ISL8483E and ISL8485E product pages

Features

- Pb-Free (RoHS compliant)
- Extended industrial temperature options (+125°C)
- RS-485 I/O pin ESD protection . . . . . ±15kV HBM
  - Class 3 ESD level on all other pins. . . . . >7kV HBM
- Specified for 10% tolerance supplies
- High data rate version (ISL8485E). . . . . up to 10Mbps
- Slew rate limited version for error free data transmission (ISL8483E) . . . . . up to 250kbps
- Single unit load allows up to 32 devices on the bus
- 1nA low current Shutdown mode (ISL8483E)
- Low quiescent current:
  - 160µA (ISL8483E)
  - 500µA (ISL8485E)
- -7V to +12V common-mode input voltage range
- Three-state Rx and Tx outputs
- 30ns propagation delays, 5ns skew (ISL8485E)
- Operate from a single +5V supply (10% tolerance)
- Current limiting and thermal shutdown for driver overload protection

Applications

- Factory automation
- Security networks
- Building environmental control systems
- Industrial/process control networks
- Level translators (such as RS-232 to RS-422)
- RS-232 “extension cords”

TABLE 1. SUMMARY OF FEATURES

PART NUMBER	HALF/FULL DUPLEX	NO. OF DEVICES ALLOWED ON BUS	DATA RATE (Mbps)	SLEW-RATE LIMITED?	RECEIVER/DRIVER ENABLE?	QUIESCENT I_{CC} (µA)	LOW POWER SHUTDOWN?	PIN COUNT
ISL8483E	Half	32	0.25	Yes	Yes	160	Yes	8
ISL8485E	Half	32	10	No	Yes	500	No	8

Ordering Information

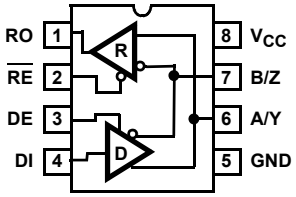
PART NUMBER (Notes 4, 5)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (RoHS COMPLIANT)	PKG. DWG. #
ISL8483EIBZ (Note 3)	8483EIBZ	-40 to +85	8 Ld SOIC	M8.15
ISL8483EIPZ **(No longer available, recommended replacement: ISL8487EIPZ)**	ISL8483EIPZ	-40 to +85	8 Ld PDIP (Note 1)	E8.3
ISL8485EABZ (Note 2)	8485EABZ	-40 to +125	8 Ld SOIC	M8.15
ISL8485ECBZ (Note 2)	8485ECBZ	0 to +70	8 Ld SOIC	M8.15
ISL8485EIBZ (Note 2)	8485EIBZ	-40 to +85	8 Ld SOIC	M8.15
ISL8485EIPZ	ISL8485EIPZ	-40 to +85	8 Ld PDIP (Note 1)	E8.3

NOTES:

1. Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in reflow solder processing applications.
2. Add “-T” suffix for 2.5k unit tape and reel option. Refer to TB347 for details on reel specifications.
3. Add “-T” suffix for 2.5k unit or “-T7A” suffix for 250 unit tape and reel options. Refer to TB347 for details on reel specifications
4. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal- (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
5. For Moisture Sensitivity Level (MSL), refer to the product information pages for the ISL8483E and the ISL8485E. For more information on MSL, refer to TB363.

Pin Configuration

ISL8483E, ISL8485E
(8 LD PDIP, SOIC)
TOP VIEWt



Truth Tables

TRANSMITTING

INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	Z	Y
X	1	1	0	1
X	1	0	1	0
0	0	X	High-Z	High-Z
1	0	X	High-Z *	High-Z *

*Shutdown mode for ISL8483E (see Note 12)

RECEIVING

INPUTS			OUTPUT
$\overline{RE}$	DE	A-B	RO
0	0	$V_{AB} \geq 0.2V$	1
0	0	$0.2V > V_{AB} > -0.2V$	Undetermined
0	0	$V_{AB} \leq -0.2V$	0
0	0	Inputs Open	1
1	0	X	High-Z*
1	1	X	High-Z

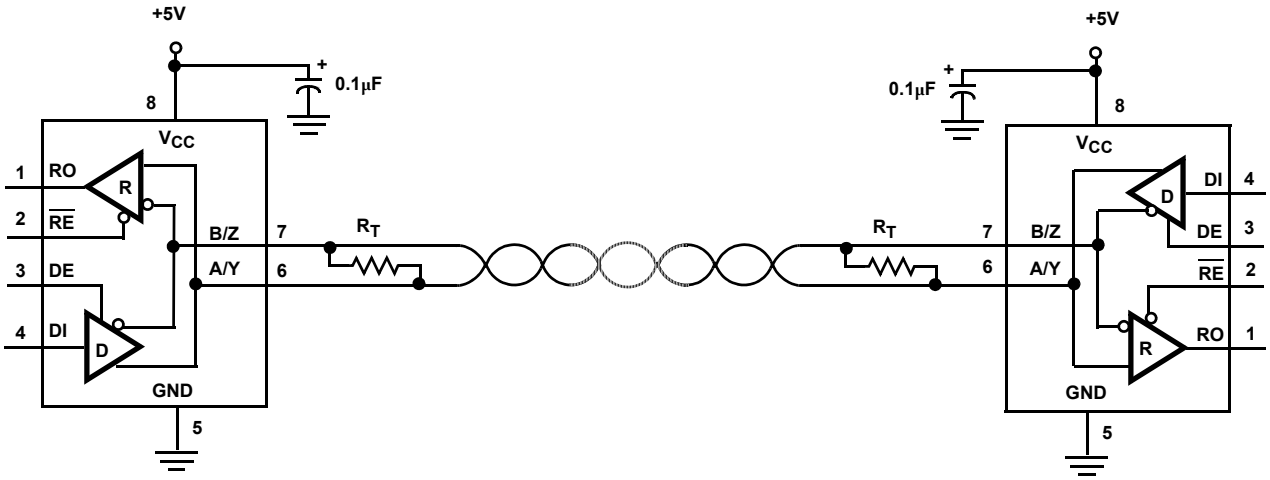
*Shutdown mode for ISL8483E (see Note 12)

Pin Descriptions

PIN	FUNCTION
RO	Receiver output: If A > B by at least 0.2V, RO is high. If A < B by 0.2V or more, RO is low. If A and B are unconnected (floating), RO is high.
$\overline{RE}$	Receiver output enable. RO is enabled when $\overline{RE}$ is low; RO is high impedance when $\overline{RE}$ is high.
DE	Driver output enable. The driver outputs, Y and Z, are enabled by bringing DE high. They are high impedance when DE is low.
DI	Driver input. A low on DI forces output Y low and output Z high. Similarly, a high on DI forces output Y high and output Z low.
GND	Ground connection.
A/Y	±15kV HBM ESD protected, RS-485, RS-422 level noninverting receiver input and noninverting driver output. Pin is an input (A) if DE = 0; pin is an output (Y) if DE = 1.
$\overline{B/Z}$	±15kV HBM ESD protected, RS-485, RS-422 level inverting receiver input and inverting driver output. Pin is an input (B) if DE = 0; pin is an output (Z) if DE = 1.
V_{CC}	System power supply input (4.5V to 5.5V).

Typical Operating Circuits

ISL8483E, ISL8485E



Absolute Maximum Ratings

V_{CC} to Ground 7V
Input Voltages
DI, DE, $\overline{RE}$. . . . . -0.5V to (V_{CC} +0.5V)
Input/Output Voltages
A/Y, B/Z. . . . . -8V to +12.5V
RO. . . . . -0.5V to (V_{CC} +0.5V)
Short-Circuit Duration
Y, Z . . . . . Continuous
ESD Rating . . . . . See "Electrical Specifications"

Thermal Information

Thermal Resistance (Typical, Note 6)	θ_{JA} (°C/W)
8 Ld SOIC Package	170
8 Ld PDIP Package*	140

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . see TB493
*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in reflow solder processing applications.

Operating Conditions

Temperature Range
ISL8485ECx. . . . . 0°C to +70°C
ISL848xEIx . . . . . -40°C to +85°C
ISL8485EAx. . . . . -40°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

6. θ_{JA} is measured with the component mounted on a low-effective thermal conductivity test board in free air. Refer to TB379 for details.

Electrical Specifications

Test Conditions: V_{CC} = 4.5V to 5.5V; unless otherwise specified. Typical values are at V_{CC} = 5V, T_A = +25°C, (Note 7)

PARAMETER	SYMBOL	TEST CONDITIONS		TEMP (°C)	MIN (Note 17)	TYP	MAX (Note 17)	UNIT
DC CHARACTERISTICS								
Driver Differential V_{OUT} (No Load)	V_{OD1}			Full	-	-	V_{CC}	V
Driver Differential V_{OUT} (With Load)	V_{OD2}	R = 50Ω (RS-422), (Figure 1 on page 6)		Full	2	3	-	V
		R = 27Ω (RS-485), (Figure 1 on page 6)		Full	1.5	2.3	5	V
Change in Magnitude of Driver Differential V_{OUT} for Complementary Output States	ΔV_{OD}	R = 27Ω or 50Ω, (Figure 1 on page 6)		Full	-	0.01	0.2	V
Driver Common-Mode V_{OUT}	V_{OC}	R = 27Ω or 50Ω, (Figure 1 on page 6)		Full	-	-	3	V
Change in Magnitude of Driver Common-Mode V_{OUT} for Complementary Output States	ΔV_{OC}	R = 27Ω or 50Ω, (Figure 1 on page 6)		Full	-	0.01	0.2	V
Logic Input High Voltage	V_{IH}	DE, DI, $\overline{RE}$		Full	2	-	-	V
Logic Input Low Voltage	V_{IL}	DE, DI, $\overline{RE}$		Full	-	-	0.8	V
Logic Input Current	I_{IN1}	DE, DI, $\overline{RE}$ (ISL8483E)		Full	-2	-	2	µA
	I_{IN1}	DI (ISL8485E)		Full	-2	-	2	µA
	I_{IN1}	DE, $\overline{RE}$ (ISL8485E)		Full	-25	-	25	µA
Input Current (A, B), (Note 15)	I_{IN2}	DE = 0V, V_{CC} = 0V or 4.5 to 5.5V	V_{IN} = 12V	Full	-	-	1	mA
			V_{IN} = -7V	Full	-	-	-0.8	mA
Receiver Differential Threshold Voltage	V_{TH}	-7V ≤ V_{CM} ≤ 12V		Full	-0.2	-	0.2	V
Receiver Input Hysteresis	ΔV_{TH}	V_{CM} = 0V		25	-	70	-	mV
Receiver Output High Voltage	V_{OH}	I_O = -4mA, V_{ID} = 200mV		Full	3.5	-	-	V
Receiver Output Low Voltage	V_{OL}	I_O = -4mA, V_{ID} = 200mV		Full	-	-	0.4	V
Three-State (High Impedance) Receiver Output Current	I_{OZR}	0.4V ≤ V_O ≤ 2.4V		Full	-	-	±1	µA

Electrical Specifications Test Conditions: V_{CC} = 4.5V to 5.5V; unless otherwise specified. Typical values are at V_{CC} = 5V, T_A = +25°C, (Note 7) **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		TEMP (°C)	MIN (Note 17)	TYP	MAX (Note 17)	UNIT
Receiver Input Resistance	R_{IN}	-7V ≤ V_{CM} ≤ 12V		Full	12	-	-	kΩ
No-Load Supply Current, (Note 8)	I_{CC}	ISL8485E, DI, $\overline{RE}$ = 0V or V_{CC}	DE = V_{CC}	Full	-	700	900	µA
			DE = 0V	Full	-	500	565	µA
		ISL8483E, DI, $\overline{RE}$ = 0V or V_{CC}	DE = V_{CC}	Full	-	470	650	µA
			DE = 0V	Full	-	160	250	µA
Shutdown Supply Current	I_{SHDN}	ISL8483E, DE = 0V, $\overline{RE}$ = V_{CC}, DI = 0V or V_{CC}		Full	-	1	50	nA
Driver Short-Circuit Current, V_O = High or Low	I_{OSD1}	DE = V_{CC}, -7V ≤ V_Y or V_Z ≤ 12V, (Note 9)		Full	35	-	250	mA
Receiver Short-Circuit Current	I_{OSR}	0V ≤ V_O ≤ V_{CC}		Full	7	-	85	mA
SWITCHING CHARACTERISTICS (ISL8485E)								
Driver Input to Output Delay	t_{PLH}, t_{PHL}	R_{DIFF} = 54Ω, C_L = 100pF, (Figure 2 on page 7)		Full	18	30	50	ns
Driver Output Skew	t_{SKEW}	R_{DIFF} = 54Ω, C_L = 100pF, (Figure 2 on page 7)		Full	-	2	10	ns
Driver Differential Rise or Fall Time	t_R, t_F	R_{DIFF} = 54Ω, C_L = 100pF, (Figure 2 on page 7)		Full	3	11	25	ns
Driver Enable to Output High	t_{ZH}	C_L = 100pF, SW = GND, (Figure 3 on page 7)		Full	-	17	70	ns
Driver Enable to Output Low	t_{ZL}	C_L = 100pF, SW = V_{CC}, (Figure 3 on page 7)		Full	-	14	70	ns
Driver Disable from Output High	t_{HZ}	C_L = 15pF, SW = GND, (Figure 3 on page 7)		Full	-	19	70	ns
Driver Disable from Output Low	t_{LZ}	C_L = 15pF, SW = V_{CC}, (Figure 3 on page 7)		Full	-	13	70	ns
Receiver Input to Output Delay	t_{PLH}, t_{PHL}	(Figure 4 on page 7)		Full	30	40	150	ns
Receiver Skew | t_{PLH} - t_{PHL} |	t_{SKD}	(Figure 4 on page 7)		25	-	5	-	ns
Receiver Enable to Output High	t_{ZH}	C_L = 15pF, SW = GND, (Figure 5 on page 8)		Full	-	9	50	ns
Receiver Enable to Output Low	t_{ZL}	C_L = 15pF, SW = V_{CC}, (Figure 5 on page 8)		Full	-	9	50	ns
Receiver Disable from Output High	t_{HZ}	C_L = 15pF, SW = GND, (Figure 5 on page 8)		Full	-	9	50	ns
Receiver Disable from Output Low	t_{LZ}	C_L = 15pF, SW = V_{CC}, (Figure 5 on page 8)		Full	-	9	50	ns
Maximum Data Rate	f_{MAX}	(Note 16)		Full	10	-	-	Mbps
SWITCHING CHARACTERISTICS (ISL8483E)								
Driver Input to Output Delay	t_{PLH}, t_{PHL}	R_{DIFF} = 54Ω, C_L = 100pF, (Figure 2 on page 7)		Full	250	800	2000	ns
Driver Output Skew	t_{SKEW}	R_{DIFF} = 54Ω, C_L = 100pF, (Figure 2 on page 7)		Full	-	160	800	ns
Driver Differential Rise or Fall Time	t_R, t_F	R_{DIFF} = 54Ω, C_L = 100pF, (Figure 2 on page 7)		Full	250	800	2000	νσ
Driver Enable to Output High	t_{ZH}	C_L = 100pF, SW = GND, (Figure 3 on page 7), (Note 10)		Full	250	-	2000	νσ
Driver Enable to Output Low	t_{ZL}	C_L = 100pF, SW = V_{CC}, (Figure 3 on page 7), (Note 10)		Full	250	-	2000	νσ
Driver Disable from Output High	t_{HZ}	C_L = 15pF, SW = GND, (Figure 3 on page 7)		Full	300	-	3000	νσ
Driver Disable from Output Low	t_{LZ}	C_L = 15pF, SW = V_{CC}, (Figure 3 on page 7)		Full	300	-	3000	νσ
Receiver Input to Output Delay	t_{PLH}, t_{PHL}	(Figure 4 on page 7)		Full	250	350	2000	ns
Receiver Skew | t_{PLH} - t_{PHL} |	t_{SKD}	(Figure 4 on page 7)		25	-	25	-	ns
Receiver Enable to Output High	t_{ZH}	C_L = 15pF, SW = GND, (Figure 5 on page 8), (Note 11)		Full	-	10	50	ns
Receiver Enable to Output Low	t_{ZL}	C_L = 15pF, SW = V_{CC}, (Figure 5 on page 8), (Note 11)		Full	-	10	50	ns

Electrical Specifications Test Conditions: V_{CC} = 4.5V to 5.5V; unless otherwise specified. Typical values are at V_{CC} = 5V, T_A = +25°C, (Note 7) **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	MIN (Note 17)	TYP	MAX (Note 17)	UNIT
Receiver Disable from Output High	t_{HZ}	C_L = 15pF, SW = GND, (Figure 5 on page 8)	Full	-	10	50	ns
Receiver Disable from Output Low	t_{LZ}	C_L = 15pF, SW = V_{CC}, (Figure 5 on page 8)	Full	-	10	50	ns
Maximum Data Rate	f_{MAX}	(Note 16)	Full	250	-	-	kbps
Time to Shutdown	t_{SHDN}	(Note 12)	Full	50	200	600	ns
Driver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	C_L = 100pF, SW = GND, (Figure 3 on page 7), (Notes 12, 13)	Full	-	-	2000	νσ
Driver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	C_L = 100pF, SW = V_{CC}, (Figure 5 on page 8), (Notes 12, 13)	Full	-	-	2000	νσ
Receiver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	C_L = 15pF, SW = GND, (Figure 5 on page 8), (Notes 12, 14)	Full	-	-	2500	ns
Receiver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	C_L = 15pF, SW = V_{CC}, (Figure 5 on page 8), (Notes 12, 14)	Full	-	-	2500	ns
ESD PERFORMANCE							
RS-485 Pins (A/Y, B/Z)		Human Body Model	25	-	±15	-	kV
All Other Pins			25	-	>±7	-	kV

NOTES:

7. All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.
8. Supply current specification is valid for loaded drivers when DE = 0V.
9. Applies to peak current. See "Typical Performance Curves" on page 10 for more information.
10. When testing the ISL8483E, keep $\overline{RE}$ = 0 to prevent the device from entering SHDN.
11. When testing the ISL8483E, the $\overline{RE}$ signal high time must be short enough (typically <200ns) to prevent the device from entering SHDN.
12. The ISL8483E is put into shutdown by bringing $\overline{RE}$ high and DE low. If the inputs are in this state for less than 50ns, the parts are guaranteed not to enter shutdown. If the inputs are in this state for at least 600ns, the parts are guaranteed to have entered shutdown. See "Low Power Shutdown Mode (ISL8483E Only)" on page 9.
13. Keep $\overline{RE}$ = V_{CC}, and set the DE signal low time >600ns to ensure that the device enters SHDN.
14. Set the $\overline{RE}$ signal high time >600ns to ensure that the device enters SHDN.
15. Devices meeting these limits are denoted as "single unit load (1 UL)" transceivers. The RS-485 standard allows up to 32 unit loads on the bus.
16. Limits established by characterization and are not production tested.
17. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Test Circuits and Waveforms

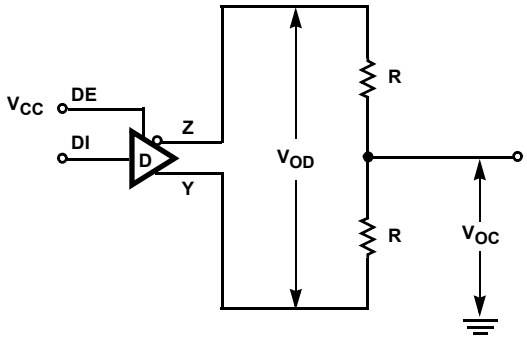


FIGURE 1. DRIVER V_{OD} AND V_{OC}

Test Circuits and Waveforms (Continued)

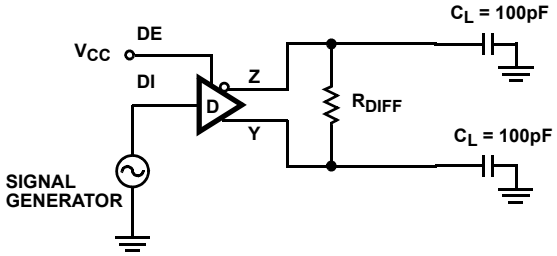
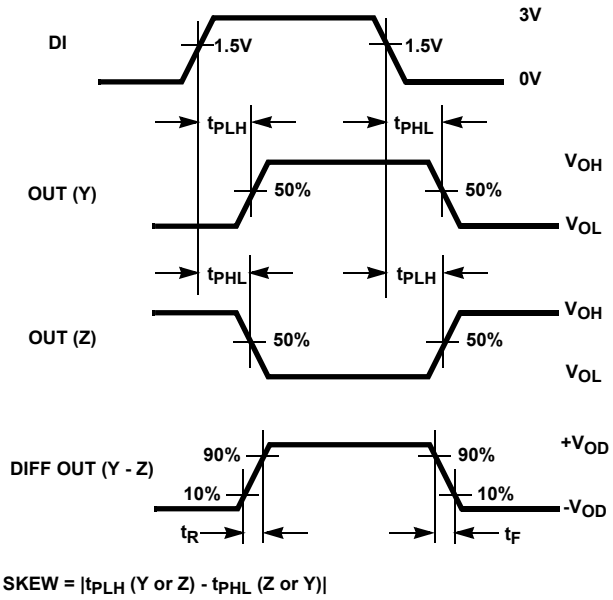


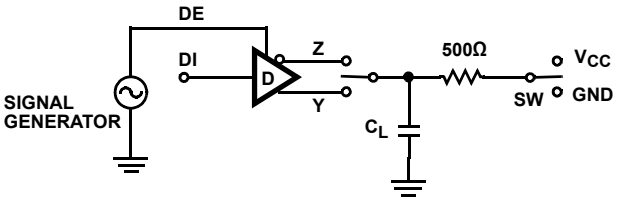
FIGURE 2A. TEST CIRCUIT



SKEW = $|t_{PLH}$ (Y or Z) - t_{PHL} (Z or Y)|

FIGURE 2B. MEASUREMENT POINTS

FIGURE 2. DRIVER PROPAGATION DELAY AND DIFFERENTIAL TRANSITION TIMES



(SHDN) FOR ISL8483E ONLY

PARAMETER	OUTPUT	$\overline{RE}$	DI	SW	C_L (pF)
t_{HZ}	Y/Z	X	1 / 0	GND	15
t_{LZ}	Y/Z	X	0 / 1	V_{CC}	15
t_{ZH}	Y/Z	0 (Note 10)	1 / 0	GND	100
t_{ZL}	Y/Z	0 (Note 10)	0 / 1	V_{CC}	100
$t_{ZH(SHDN)}$	Y/Z	1 (Note 13)	1 / 0	GND	100
$t_{ZL(SHDN)}$	Y/Z	1 (Note 13)	0 / 1	V_{CC}	100

FIGURE 3A. TEST CIRCUIT

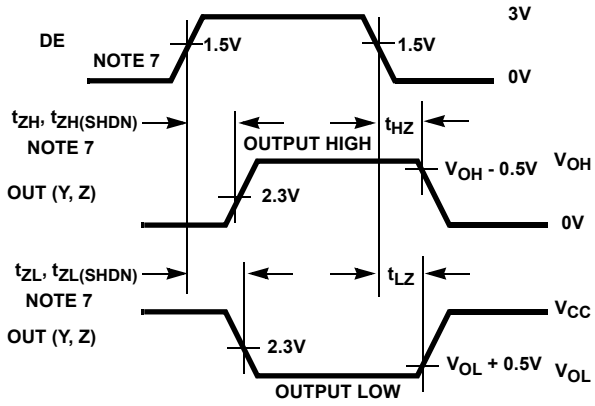


FIGURE 3B. MEASUREMENT POINTS

FIGURE 3. DRIVER ENABLE AND DISABLE TIMES

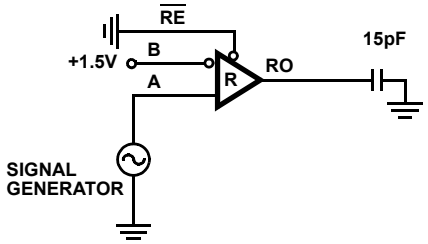


FIGURE 4A. TEST CIRCUIT

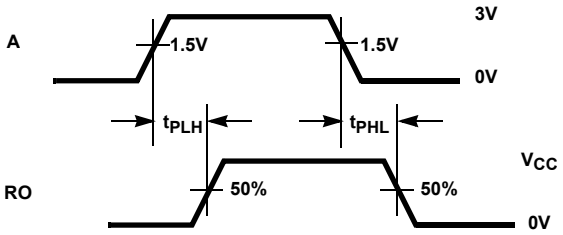
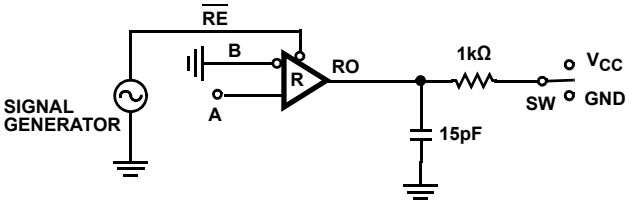


FIGURE 4B. MEASUREMENT POINTS

FIGURE 4. RECEIVER PROPAGATION DELAY

Test Circuits and Waveforms (Continued)



(SHDN) FOR ISL8483E ONLY

PARAMETER	DE	A	SW
t_{HZ}	0	+1.5V	GND
t_{LZ}	0	-1.5V	V_{CC}
t_{ZH} (Note 11)	0	+1.5V	GND
t_{ZL} (Note 11)	0	-1.5V	V_{CC}
$t_{ZH(SHDN)}$ (Note 14)	0	+1.5V	GND
$t_{ZL(SHDN)}$ (Note 14)	0	-1.5V	V_{CC}

FIGURE 5A. TEST CIRCUIT

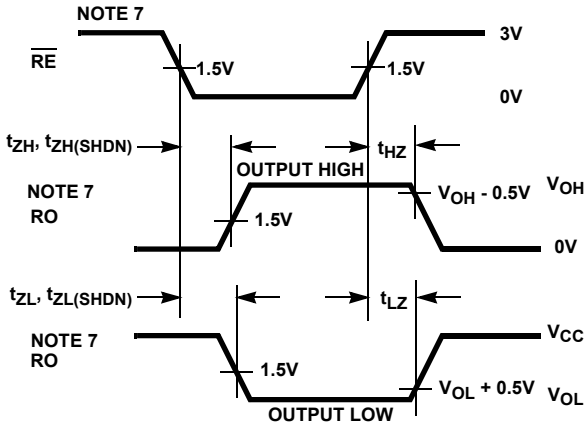


FIGURE 5B. MEASUREMENT POINTS

FIGURE 5. RECEIVER ENABLE AND DISABLE TIMES

Application Information

RS-485 and RS-422 are differential (balanced) data transmission standards for use in long haul or noisy environments. RS-422 is a subset of RS-485, so RS-485 transceivers are also RS-422 compliant. RS-422 is a point-to-multipoint (multidrop) standard, which allows only one driver and up to 10 receivers on each bus, assuming one unit load devices. RS-485 is a true multipoint standard, which allows up to 32 one unit load devices (any combination of drivers and receivers) on each bus. To allow for multipoint operation, the RS-485 specification requires that drivers must handle bus contention without sustaining any damage.

Another important advantage of RS-485 is the extended Common-Mode Range (CMR), which specifies that the driver outputs and receiver inputs withstand signals that range from +12V to -7V. RS-422 and RS-485 are intended for runs as long as 4000 feet, so the wide CMR is necessary to handle ground potential differences, as well as voltages induced in the cable by external fields.

Receiver Features

These devices use a differential input receiver for maximum noise immunity and common-mode rejection. Input sensitivity is ±200mV, as required by the RS-422 and RS-485 specifications.

Receiver input impedance surpasses the RS-422 spec of 4kΩ, and meets the RS-485 “Unit Load” requirement of 12kΩ minimum.

Receiver inputs function with common-mode voltages as high as ±7V outside the power supplies (for example, +12V and -7V), making them ideal for long networks where induced voltages are a realistic concern.

All the receivers include a “fail-safe if open” function that guarantees a high level receiver output if the receiver inputs are unconnected (floating).

Receivers easily meet the data rates supported by the corresponding driver.

ISL8483E and ISL8485E receiver outputs are tri-statable via the active low $\overline{RE}$ input.

Driver Features

The RS-485, RS-422 driver is a differential output device that delivers at least 1.5V across a 54Ω load (RS-485), and at least 2V across a 100Ω load (RS-422). The drivers feature low propagation delay skew to maximize bit width, and to minimize EMI.

The ISL8483E and ISL8485E drivers are tri-statable using the active high DE input.

The ISL8483E driver outputs are slew rate limited to minimize EMI, and to minimize reflections in unterminated or improperly terminated networks. The data rate on these slew rate limited versions is a maximum of 250kbps. The ISL8485E driver outputs are not limited, so faster output transition times allow data rates of at least 10Mbps.

Data Rate, Cables, and Terminations

RS-485 and RS-422 are intended for network lengths up to 4000 feet, but the maximum system data rate decreases as the transmission length increases. Devices operating at 10Mbps are limited to lengths less than 100 feet, whereas the 250kbps versions can operate at full data rates with lengths in excess of 1000 feet.

Twisted pair is the cable of choice for RS-485 and RS-422 networks. Twisted pair cables tend to pick up noise and other electromagnetically induced voltages as common-mode signals, which are effectively rejected by the differential receivers in these ICs.

Proper termination is imperative when using the 10Mbps devices to minimize reflections. Short networks using the 250kbps versions need not be terminated, but terminations are recommended unless power dissipation is an overriding concern.

In point-to-point, or point-to-multipoint (single driver on bus) networks, the main cable should be terminated in its characteristic impedance (typically 120Ω) at the end farthest from the driver. In multi-receiver applications, stubs connecting receivers to the main cable should be kept as short as possible. Multipoint (multi-driver) systems require that the main cable be terminated in its characteristic impedance at both ends. Stubs connecting a transceiver to the main cable should be kept as short as possible.

Built-In Driver Overload Protection

As stated previously, the RS-485 specification requires that drivers survive worst case bus contentions undamaged. The ISL848xE devices meet this requirement through driver output short-circuit current limits and on-chip thermal shutdown circuitry.

The driver output stages incorporate short-circuit current limiting circuitry which ensures that the output current never exceeds the RS-485 specification, even at the common-mode voltage range extremes. Additionally, these devices use a foldback circuit which reduces the short-circuit current, and thus the power dissipation, whenever the contending voltage exceeds either supply.

In the event of a major short-circuit condition, ISL848xE devices perform a thermal shutdown that disables the drivers whenever the die temperature becomes excessive. This eliminates the power dissipation, allowing the die to cool. The drivers automatically re-enable after the die temperature drops about 15°. If the contention persists, the thermal shutdown/re-enable cycle repeats until the fault is cleared. Receivers stay operational during thermal shutdown.

Low Power Shutdown Mode (ISL8483E Only)

These CMOS transceivers all use a fraction of the power required by their bipolar counterparts, but the ISL8483E includes a shutdown feature that reduces the already low quiescent I_{CC} to a 1nA trickle. The ISL8483E enters shutdown whenever the receiver and driver are *simultaneously* disabled ($\overline{RE}$ = V_{CC} and DE = GND) for a period of at least 600ns. Disabling both the driver and the receiver for fewer than 50ns guarantees that the ISL8483E will not enter shutdown.

Note that receiver and driver enable times increase when the ISL8483E enables from shutdown. Refer to Notes 10 through Notes 13 on page 6, at the end of the "Electrical Specifications" table for more information.

ESD Protection

All pins on these interface devices include Class 3 Human Body Model (HBM) ESD protection structures, but the RS-485 pins (driver outputs and receiver inputs) incorporate advanced structures allowing them to survive ESD events in excess of ±15kV HBM. The RS-485 pins are particularly vulnerable to ESD damage because they typically connect to an exposed port on the exterior of the finished product. Simply touching the port pins or connecting a cable can cause an ESD event that might destroy unprotected ICs. These new ESD structures protect the device whether or not it is powered up without allowing any latchup mechanism to activate and without degrading the RS-485 common-mode range of -7V to +12V. This built-in ESD protection eliminates the need for board level protection structures (such as transient suppression diodes), and the associated, undesirable capacitive load they present.

Human Body Model Testing

As the name implies, this test method emulates the ESD event delivered to an IC during human handling. The tester delivers the charge stored on a 100pF capacitor through a 1.5kΩ current limiting resistor into the pin under test. The HBM method determines an IC's ability to withstand the ESD events typically present during handling and manufacturing.

The RS-485 pin survivability on this high ESD family has been characterized to be in excess of ±15kV for discharges to GND.

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

GND

TRANSISTOR COUNT:

518

PROCESS:

Si Gate CMOS

Typical Performance Curves V_{CC} = 5V, T_A = +25°C, ISL8483E and ISL8485E; unless otherwise specified.

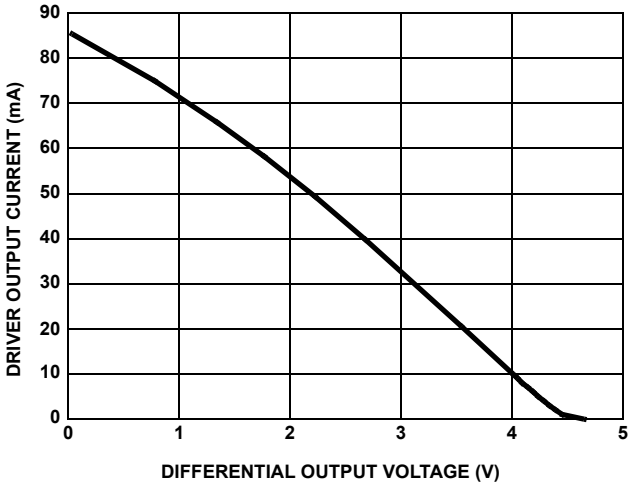


FIGURE 6. DRIVER OUTPUT CURRENT vs DIFFERENTIAL OUTPUT VOLTAGE

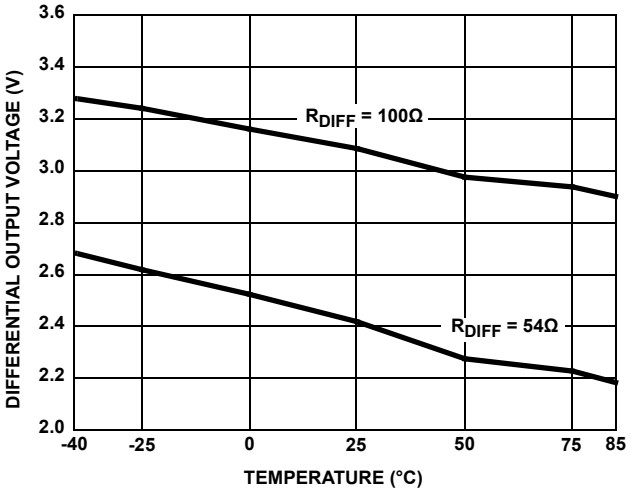


FIGURE 7. DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs TEMPERATURE

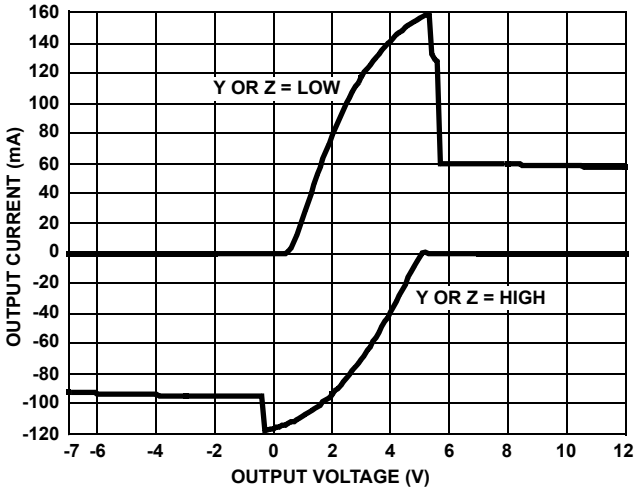


FIGURE 8. DRIVER OUTPUT CURRENT vs SHORT-CIRCUIT VOLTAGE

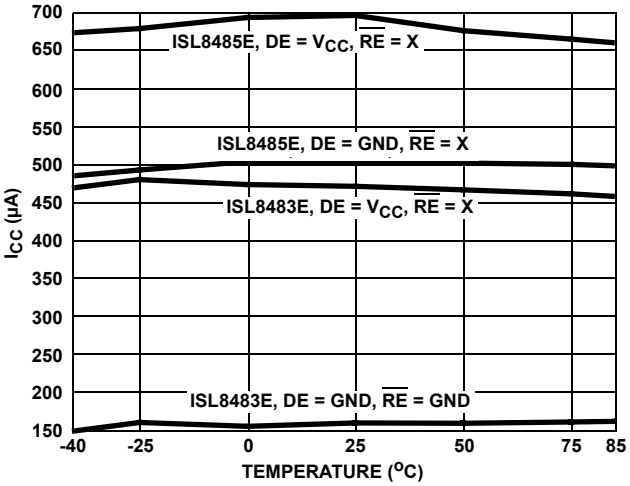


FIGURE 9. SUPPLY CURRENT vs TEMPERATURE

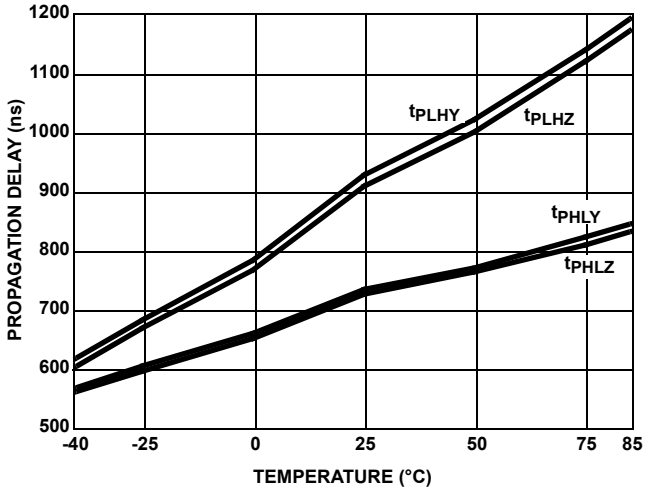


FIGURE 10. DRIVER PROPAGATION DELAY vs TEMPERATURE (ISL8483E)

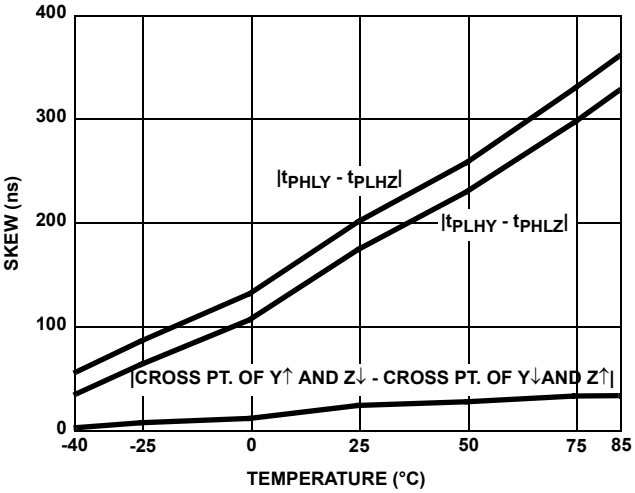


FIGURE 11. DRIVER SKEW vs TEMPERATURE (ISL8483E)

Typical Performance Curves V_{CC} = 5V, T_A = +25°C, ISL8483E and ISL8485E; unless otherwise specified. (Continued)

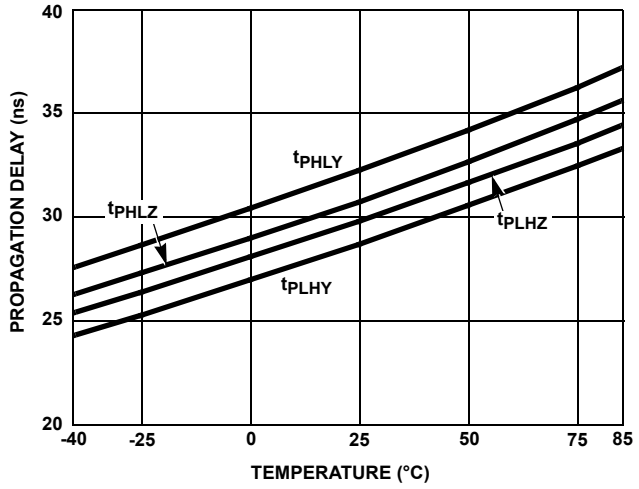


FIGURE 12. DRIVER PROPAGATION DELAY vs TEMPERATURE (ISL8485E)

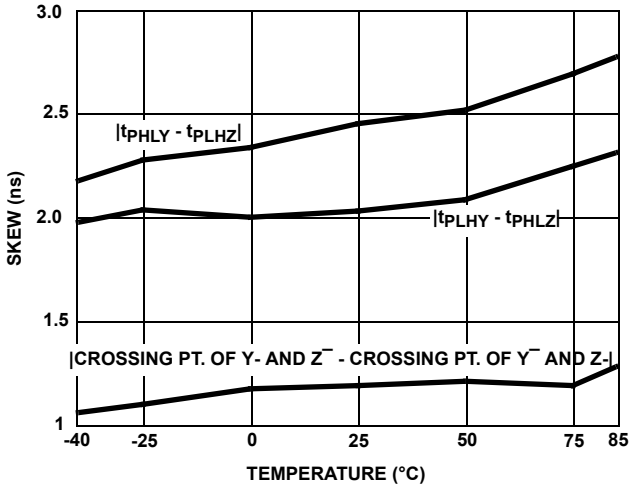


FIGURE 13. DRIVER SKEW vs TEMPERATURE (ISL8485E)

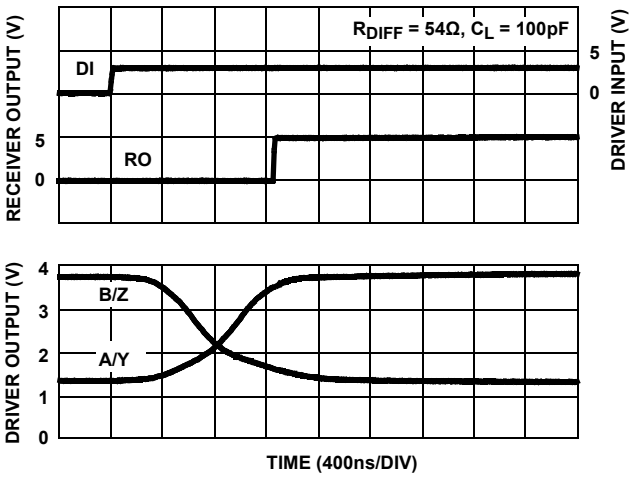


FIGURE 14. DRIVER AND RECEIVER WAVEFORMS, LOW TO HIGH (ISL8483E)

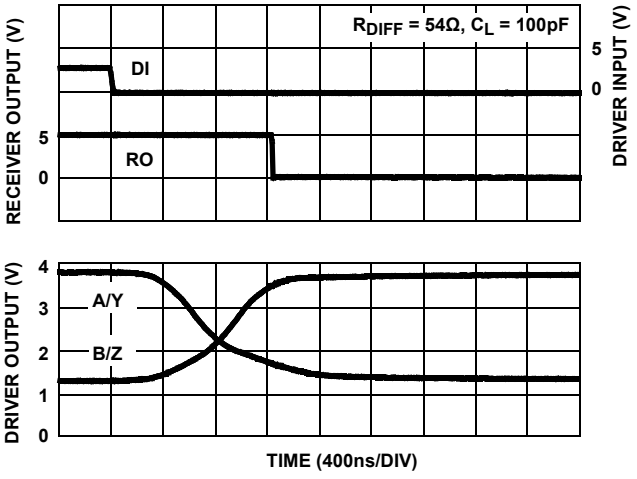


FIGURE 15. DRIVER AND RECEIVER WAVEFORMS, HIGH TO LOW (ISL8483E)

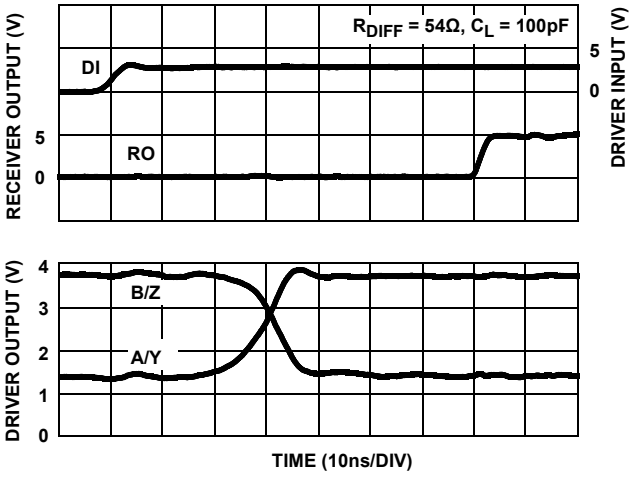


FIGURE 16. DRIVER AND RECEIVER WAVEFORMS, LOW TO HIGH (ISL8485E)

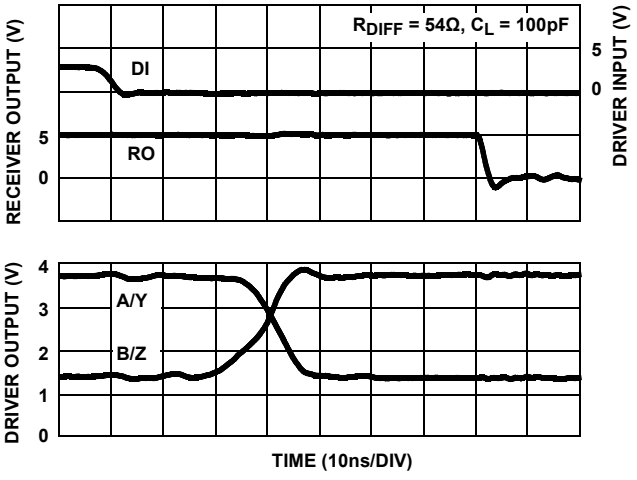


FIGURE 17. DRIVER AND RECEIVER WAVEFORMS, HIGH TO LOW (ISL8485E)

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure that you have the latest revision.

DATE	REVISION	CHANGE
Aug 31, 2017	FN6048.12	Updated Receiving Truth table on page 2. Applied Intersil A Renesas Company template.
May 8, 2017	FN6048.11	Applied new header/footer Removed any mention of military version. Updated ordering information table on page 2 as follows: Updated Note 2, added Notes 3, and 5.
Sept 3, 2015	FN6048.10	- Ordering Information Table on page 2. - Added Revision History. - Added About Intersil Verbiage. -Updated POD M8.15 to most current revision with changes as follows: -Revision 1 to Revision 2 Changes: Updated to new POD format by removing table and moving dimensions onto drawing and adding land pattern -Revision 2 to Revision 3 Changes: Changed Note 1 "1982" to "1994" Changed in Typical Recommended Land Pattern the following: 2.41(0.095) to 2.20(0.087) 0.76 (0.030) to 0.60(0.023) 0.200 to 5.20(0.205) -Revision 3 to Revision 4 Changes: Changed Note 1 "1982" to "1994"

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing, and high-end consumer markets.

For the most updated datasheet, application notes, related documentation, and related parts, see the respective product information page found at www.intersil.com.

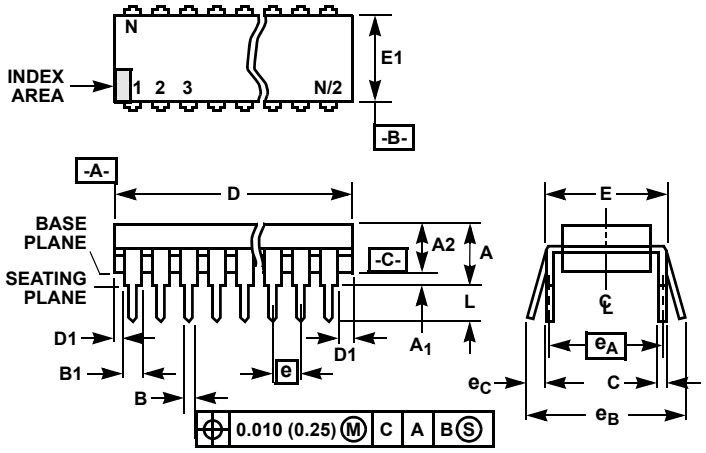
For a listing of definitions and abbreviations of common terms used in our documents, visit www.intersil.com/glossary.

You can report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support.

Dual-In-Line Plastic Packages (PDIP)

For the most recent package outline drawing, see E8.3.



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E8.3 (JEDEC MS-001-BA ISSUE D)

8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8		8		9

Rev. 0 12/93

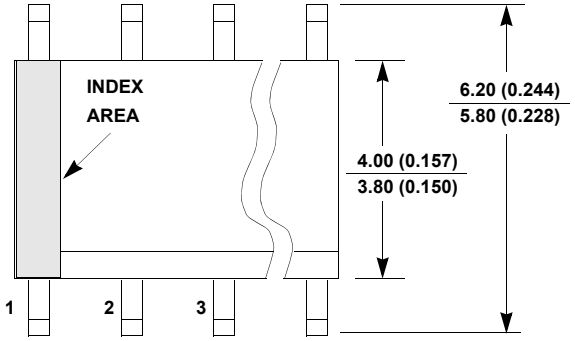
Package Outline Drawing

For the most recent package outline drawing, see M8.15.

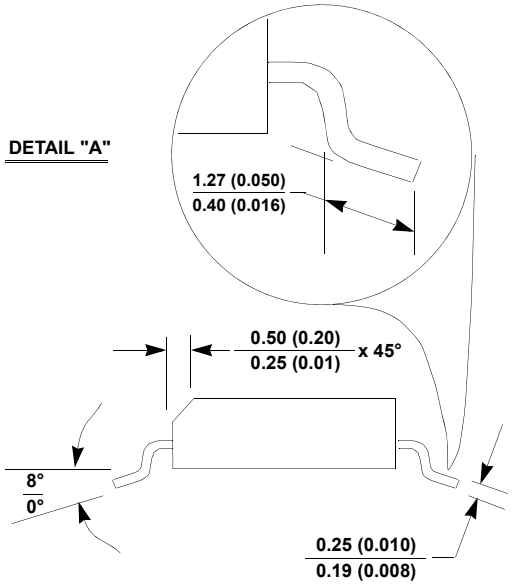
M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

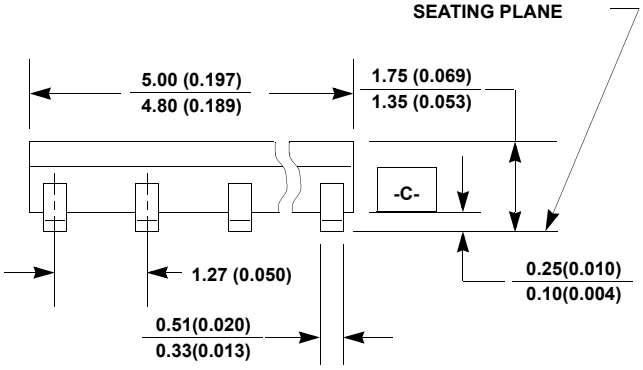
Rev 4, 1/12



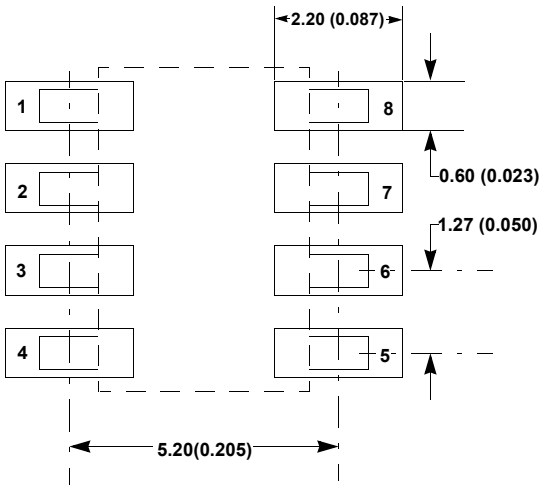
TOP VIEW



SIDE VIEW "B"



SIDE VIEW "A



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.