Applications Note: SY8087

High Efficiency 1.5MHz, 1.5A Synchronous Step Down Regulator

General Description

The SY8087 is a high-efficiency, high frequency synchronous step-down DC-DC regulator IC capable of delivering up to 1.5A output currents. SY8087 operates over a wide input voltage range from 3V to 5.5V and integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

Low output voltage ripple and small external inductor and capacitor sizes are achieved with greater than 1MHz switching frequency.

Features

- Low $R_{DS(ON)}$ for internal switches (top/bottom) 180mΩ/120mΩ
- 3-5.5V input voltage range
- High switching frequency 1.5MHz minimizes the external components
- Internal softstart limits the inrush current
- 100% dropout operation
- RoHS Compliant and Halogen Free
- Compact package: SOT23-5

Ordering Information

SY8087 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note[1]
SY8087AAC	SOT23-5	1.5A

Applications

- LCD TV
- Set Top Box
- Net PC
- Mini-Notebook PC
- Access Point Router

Typical Applications

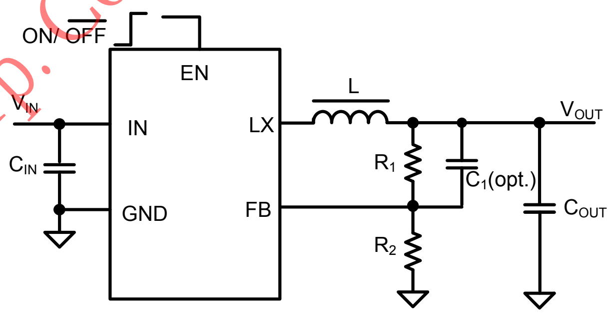
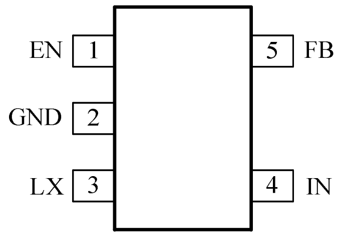


Figure 1.Schematic diagram

Pinout (top view)



SOT23-5

Top Mark: HL*xyz* (device code: HL, ***x=year code, y=week code, z= lot number code*****)**

Pin Name	Pin Number	Pin Description
EN	1	Enable control. Pull high to turn on. Do not float.
GND	2	Ground pin
LX	3	Inductor pin. Connect this pin to the switching node of inductor.
IN	4	Power input pin.
FB	6	Output Feedback Pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: Vout=0.6*(1+R_1/R_2).

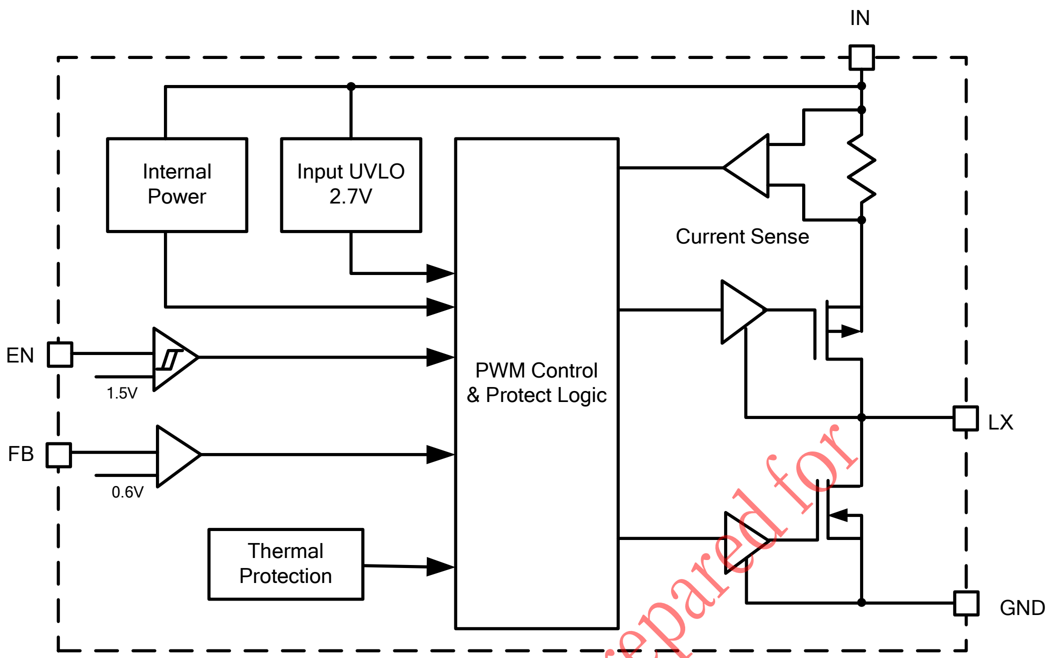
Absolute Maximum Ratings (Note 1)

Supply Input Voltage -- 6.0V
Enable, FB Voltage--- V_{IN} + 0.6V
Power Dissipation, P_D @ T_A = 25°C,
SOT23-5-- 0.6W
Package Thermal Resistance (Note 2)
SOT23-5, θ_{JA} -- 170°C/W
SOT23-5, θ_{JC} --130°C/W
Junction Temperature Range ---125°C
Lead Temperature (Soldering, 10 sec.)-- 260°C
Storage Temperature Range -- -65°C to 150°C
ESD Susceptibility (Note 2)
HBM (Human Body Mode) -- 2kV
MM (Machine Mode) --- 200V
Dynamic LX voltage in 50ns duration ---------------------------------- IN+3V to GND-4V

Recommended Operating Conditions (Note 3)

Supply Input Voltage --3V to 5.5V
Junction Temperature Range --- -40°C to 125°C
Ambient Temperature Range -- -40°C to 85°C

Function Block



Electrical Characteristics

(V_{IN} = 5V, V_{OUT} = 2.5V, L = 2.2uH, C_{OUT} = 10uF, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		3		5.5	V
Quiescent Current	I_Q	I_{OUT}=0, V_{FB}=V_{REF} · 105%	70	80	100	μA
Shutdown Current	I_{SHDN}	EN=0		0.1	1	μA
Feedback Reference Voltage	V_{REF}		0.588	0.6	0.612	V
FB Input Current	I_{FB}	V_{FB}=V_{IN}	-50		50	nA
PFET RON	$R_{DS(ON),P}$			180	200	mΩ
NFET RON	$R_{DS(ON),N}$			120	160	mΩ
PFET Current Limit	I_{LIM}		1.8			A
EN rising threshold	V_{ENH}		1.5			V
EN falling threshold	V_{ENL}				0.4	V
Input UVLO threshold	V_{UVLO}				2.7	V
UVLO hysteresis	V_{HYS}			0.1		V
Oscillator Frequency	F_{OSC}		1.3	1.5	2.0	MHz
Min ON Time				50		ns
Max Duty Cycle			100			%
Thermal Shutdown Temperature	T_{SD}			160		°C

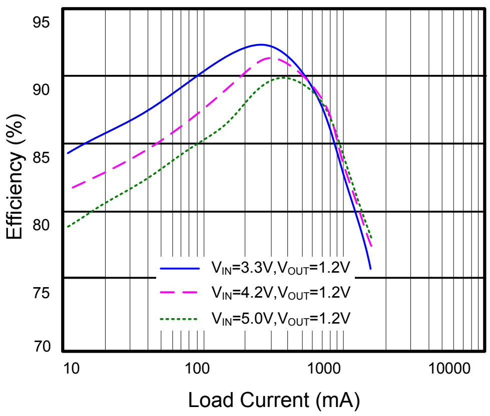
Note 1: Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2: θJA is measured in the natural convection at TA = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Pin 2 of SOT23-5 packages is the case position for θJC measurement. Test condition: Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane

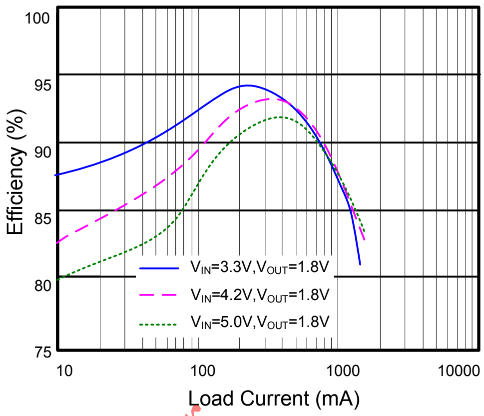
Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

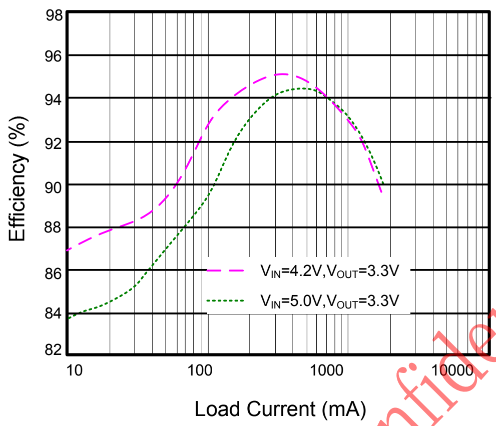
Efficiency vs. Load Current



Efficiency vs. Load Current

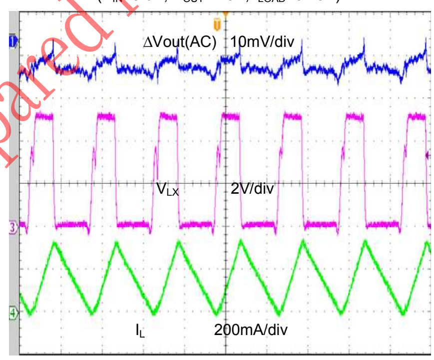


Efficiency vs. Load Current



Output Ripple

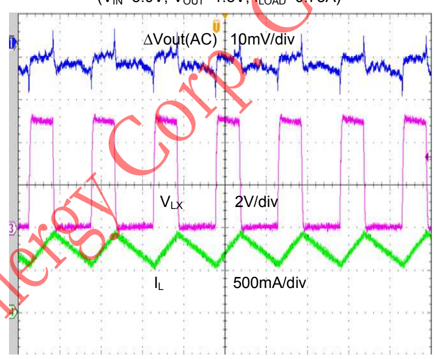
(V_{IN}=5.0V, V_{OUT}=1.8V, I_{LOAD}=0.15A)



Time (400ns/div)

Output Ripple

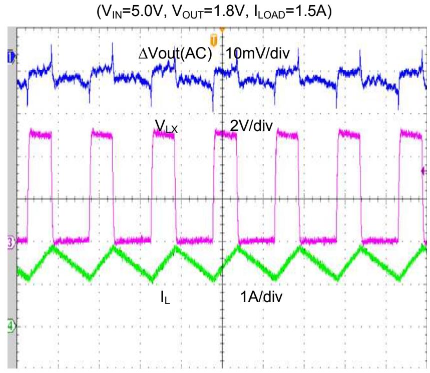
(V_{IN}=5.0V, V_{OUT}=1.8V, I_{LOAD}=0.75A)



Time (400ns/div)

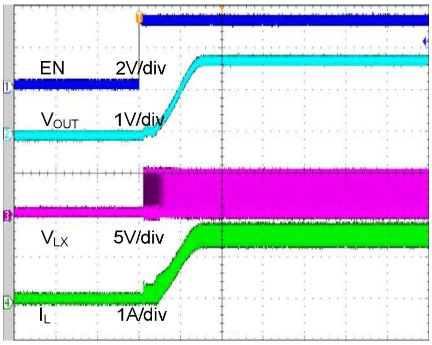
Output Ripple

(V_{IN}=5.0V, V_{OUT}=1.8V, I_{LOAD}=1.5A)



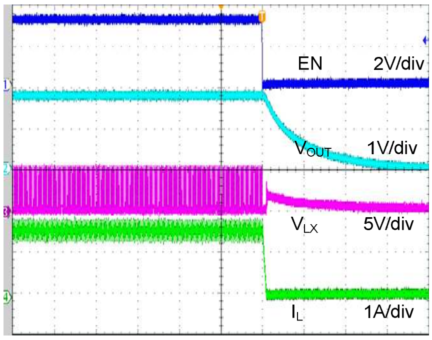
Time (400ns/div)

Startup from Enable
(V_{IN}=5.0V, V_{OUT}=1.8V,I_{LOAD}=1.5A)



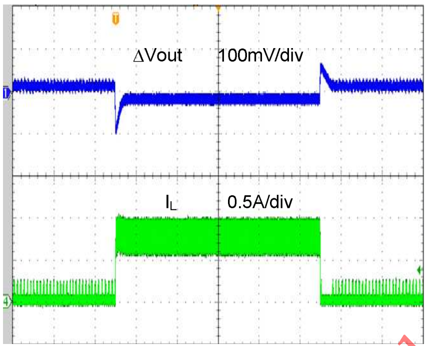
Time (800us/div)

Shutdown from Enable
(V_{IN}=5.0V, V_{OUT}=1.8V,I_{LOAD}=1.5A)



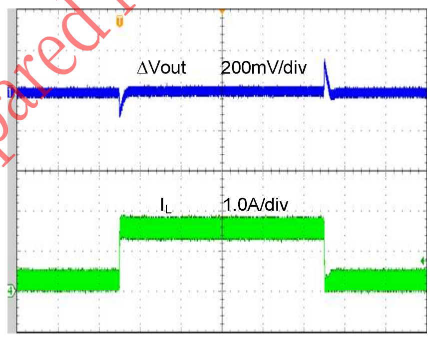
Time (20us/div)

Load Transient
(V_{IN}=5.0V, V_{OUT}=1.8V,I_{LOAD}=0-0.75A)



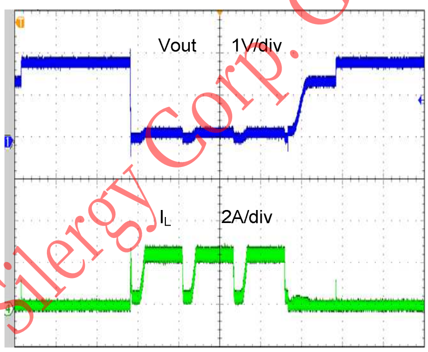
Time (100us/div)

Load Transient
(V_{IN}=5.0V, V_{OUT}=1.8V,I_{LOAD}=0.15-1.5A)



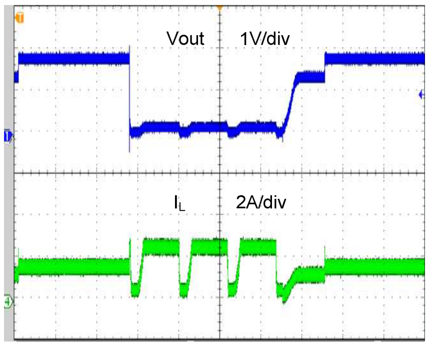
Time (100us/div)

Short Circuit Protection
(V_{IN}=5.0V, V_{OUT}=1.8V,Null load to short)



Time (2ms/div)

Short Circuit Protection
(V_{IN}=5.0V, V_{OUT}=1.8V,1.5A to short)



Time (2ms/div)

Operation

SY8087 is a synchronous buck regulator IC that integrates the PWM control, top and bottom switches on the same die to minimize the switching transition loss and conduction loss. With ultra low $R_{DS(ON)}$ power switches and proprietary PWM control, this regulator IC can achieve the highest efficiency and the highest switch frequency simultaneously to minimize the external inductor and capacitor size, and thus achieving the minimum solution footprint.

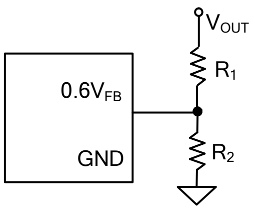
Applications Information

Because of the high integration in the SY8087 IC, the application circuit based on this regulator IC is rather simple. Only input capacitor C_{IN}, output capacitor C_{OUT}, output inductor L and feedback resistors (R1 and R2) need to be selected for the targeted applications specifications.

SY8087 will sense the output voltage conditions for the fault protection. If the DC output voltage is about 3% over the regulation level, both switches will turn off and remain in this OFF state. If the DC output voltage is below 33% of the regulation level, the internal soft-start node is discharged and the error amplifier output is reset to minimum. Then the part will restart. When the output voltage is below 33% of the regulation, the frequency is folded back to 25% of the normal frequency and the current limit is decreased to 60% of the normal current limit to prevent the inductor current runaway and to reduce the power dissipation within the IC under true short circuit conditions.

<u>Feedback resistor dividers R1 and R2</u>:
Choose R1 and R2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R1 and R2. A value of between 10k and 1M is highly recommended for both resistors. If Vout is 1.8V, R1=100k is chosen, then R2 can be calculated to be 50k:

$$R_2 = \frac{0.6V}{V_{OUT} - 0.6V} R_1 .$$



<u>Input capacitor CIN</u>:
This ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = I_{OUT} \bullet \sqrt{D(1-D)}$$

This formula has a maximum at VIN=2VOUT condition, where ICIN_RMS=IOUT/2. This simple worst-case condition is commonly used for DC/DC design.

With the maximum load current at 1.5A. A typical X5R or better grade ceramic capacitor with 6V rating and more than 1 pcs 10uF capacitor can handle this ripple current well. To minimize the potential noise problem, place this ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by CIN, and IN/GND pins

<u>Output capacitor COUT:</u>
The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use X5R or better grade ceramic capacitor with 6V rating and greater than 40uF capacitance.

<u>Output inductor L:</u>
There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{F_{SW} \times I_{OUT,MAX} \times 40\%}$$

where Fsw is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.
The SY8087 regulator IC is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1-V_{OUT}/V_{IN,MAX})}{2 \cdot F_{SW} \cdot L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<50mΩ to achieve a good overall efficiency.

Enable Operation

Pulling the EN pin low (<0.4V) will shut down the device. During shut down mode, the SY8087 shutdown current drops to lower than 0.1uA. Driving the EN pin high (>1.5V) will turn on the IC again.

Load Transient Considerations:

The SY8087 regulator IC integrates the compensation components to achieve good stability and fast transient responses. In some applications, adding a 22pF ceramic cap in parallel with R1 may further speed up the load transient responses and is thus recommended for applications with large load transient step requirements.

Layout Design:

The layout design of SY8087 regulator is relatively simple. For the best efficiency and minimum noise problems, we should place the following components close to the IC: C_{IN}, L, R1 and R2.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

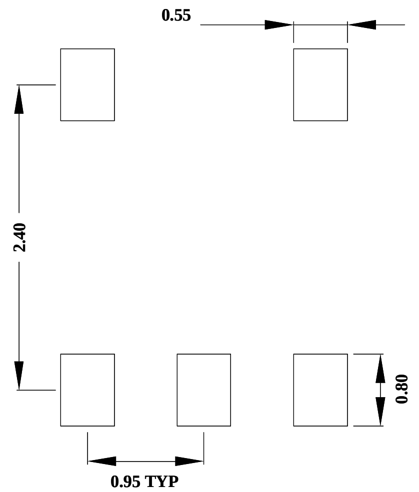
2) C_{IN} must be close to Pins IN and GND. The loop area formed by C_{IN} and GND must be minimized.

3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.

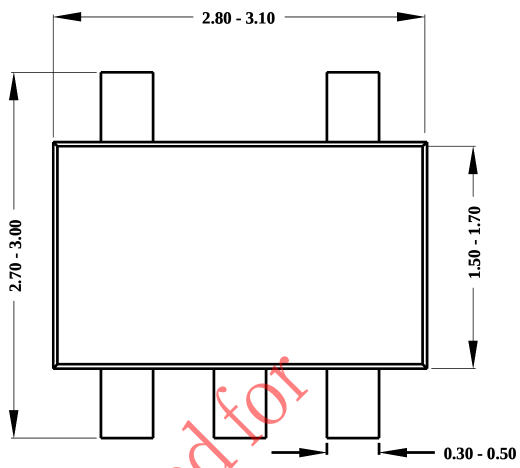
4) The components R1 and R2, and the trace connecting to the FB pin must NOT be adjacent to the LX net on the PCB layout to avoid the noise problem.

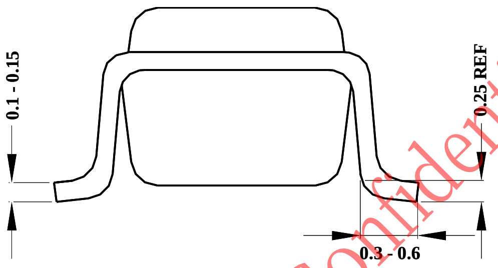
5) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a LiIon battery, it is desirable to add a pull down 1MΩ resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

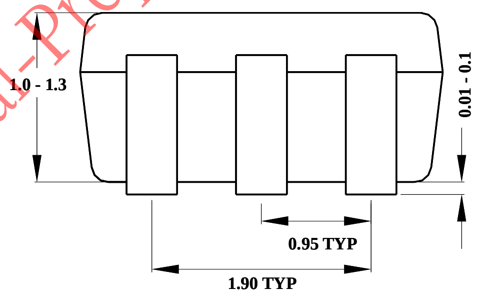
SOT23-5 Package outline & PCB layout design



Recommended Pad Layout





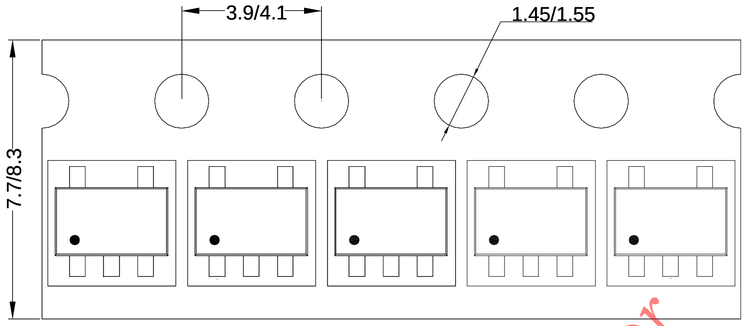


Notes: All dimensions are in millimeters.
All dimensions don't include mold flash & metal burr.

Taping & Reel Specification

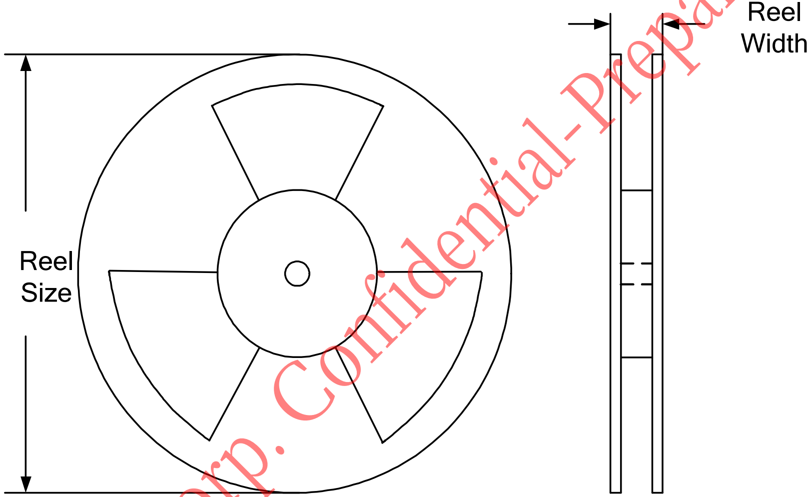
1. Taping orientation

SOT23-5



Feeding direction →

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Reel width(mm)	Trailer length(mm)	Leader length (mm)	Qty per reel
SOT23-5	8	4	7"	8.4	280	160	3000

3. Others: NA