TPS92561 Phase-Dimmable, Single-Stage Boost Controller for LED Lighting

1 Features

- Simple Hysteretic Control
- Compact Solution and Simple Bill Of Materials
- Naturally Dimmable TRIAC and Reverse Phase Dimmers
- Implements LED Drive Circuits Capable of High >90% Efficiency, >0.9 Power Factor, and <20% THD
- Programmable Output Over-voltage Protection
- Overtemperature Shutdown
- VCC Undervoltage Lockout
- 8-Pin VSSOP (MSOP) With Exposed Pad

2 Applications

- Off-Line TRIAC Dimmable Applications
- Off-Line Non-Dimmable Lamps
- Lamps Requiring the Highest Efficiency and Lowest BOM Cost
- Industrial and Commercial Solid State Lighting

3 Description

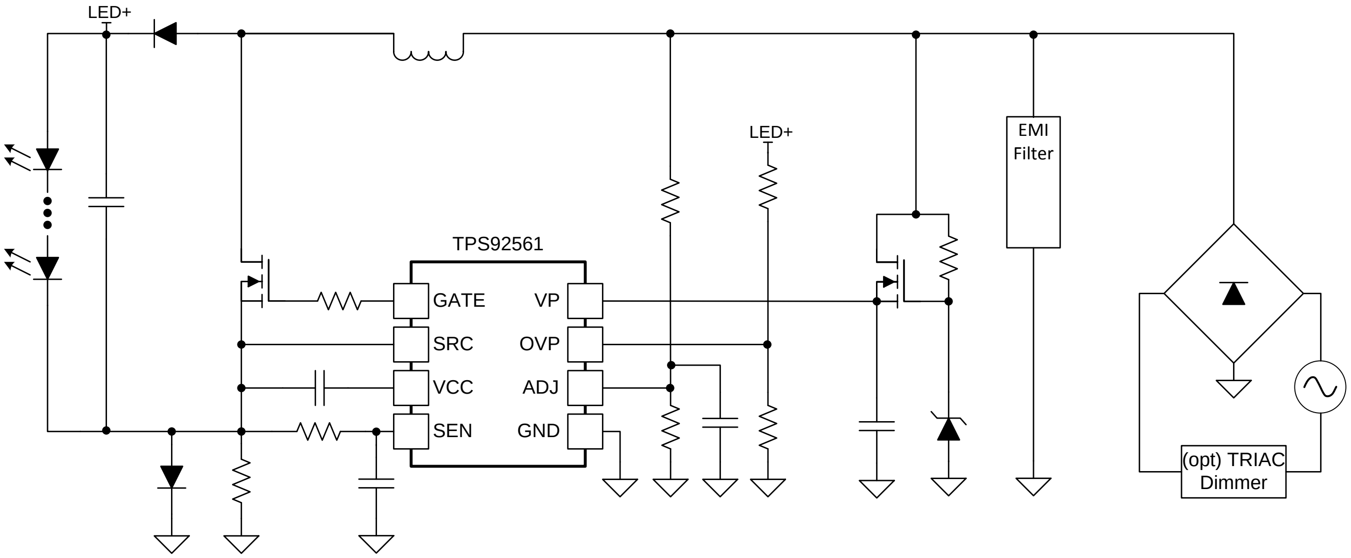
The TPS92561 device is a boost controller for LED lighting applications utilizing high-voltage, low-current LEDs. A boost converter approach to lighting applications allows the creation of the smallest volume converter possible and enables high efficiencies beyond 90%. The device incorporates a current sense comparator with a fixed offset enabling a simple hysteretic control scheme free of the loop compensation issues typically associated with a boost converter. The integrated OVP and VCC regulator further simplify the design procedure and reduce external component count.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS92561	HVSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

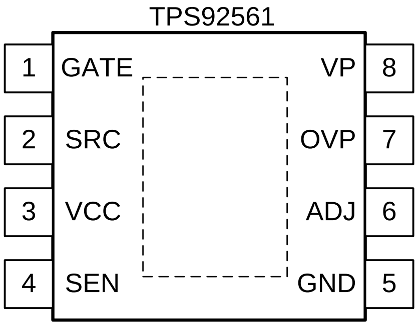
Changes from Revision B (January 2014) to Revision C	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1

Changes from Revision A (December 2013) to Revision B	Page
• Removed product preview banner	1

Changes from Original (December 2013) to Revision A	Page
• Updated figure to add AR111 lamps for closed-loop regulated e-transformer compatible, non-TRIAC dimmable boost for AR111 and MR16 lamps	16

5 Pin Configuration and Functions

DGN Package
8-Pin HVSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GATE	1	O	Gate driver output pin. Connect to the gate terminal of the low-side N-channel power FET. For off-line applications, use a gate resistance of ≥ 75 Ω.
SRC	2	I	Gate driver return. Connect to the source terminal of the low-side, N-channel power FET. By connecting SRC to the FET source, switching current spikes are not passed through the sense resistor.
VCC	3	O	Gate driver power rail. Connect a 0.47-µF minimum decoupling capacitor from this pin to SRC pin.
SEN	4	I	LED current sense pin. Current sense input. For off-line applications, connect to SEN and the current sensing resistor through an R-C filter with a time constant similar to the converter switching frequency.
GND	5	—	Ground. Connect to the system ground plane.
ADJ	6	I	LED current adjust pin. Converter reference. Can be connected to the converter rectified AC for high power factor, or to the LED output voltage for improved line regulation.
OVP	7	I	Overvoltage. Connect to resistor divider from VOUT (LED+) to detect overvoltage.
VP	8	I	Power supply of the integrated circuit (IC). Connect to an appropriate voltage source to provide power for the IC. (VP ≤ 42 V) See *Example Circuits* for example diagrams.
PowerPAD	—	—	Solder to printed circuit board (PCB) with or without thermal vias to enhance thermal performance. Although it can be left floating, TI recommends to connect the PowerPAD™ to GND.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Pin voltage range (2)	SRC, SEN, ADJ, OVP	–0.3	5	V
	VP	–1	45	
	VCC	–0.3	12	
T_{stg}	Storage temperature	–60	150	°C
T_J	Junction temperature	Internally Limited		

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1) (2)	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (3)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) ESD testing is performed according to the respective JESD22 JEDEC standard.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VP	Supply voltage	6.5		42	V
T_J	Operating junction temperature	–40		125	°C

6.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC (1)		TPS92561 DGN (HVSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	65.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	64.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	44.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	13.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over recommended operating conditions with –40°C ≤ T_J ≤ 125°C. VCC = 12 V. C_{VCC} = 0.47 µF

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_{IN}	V_P operating current	6.5 V < V_{VP} < 42 V	0.5	1	1.6	mA
VCC REGULATOR						
VCC	V_{CC} regulated voltage	I_{CC} ≤ 10 mA C_{VCC} = 0.47 µF 12 V < V_{VP} < 42 V	7.75	8.35	8.95	V
		I_{CC} = 10 mA C_{VCC} = 0.47 µF V_{VP} = 6.5 V	5.42	5.92	6.42	
		I_{CC} = 0 mA C_{VCC} = 0.47 µF V_{VP} = 2 V		2		
$I_{CC\text{-}LIM}$	V_{CC} current limit	V_{CC} = 0 V 6.5 V < V_{VP} < 42 V	20	34	56	mA
$V_{CC\text{-}UVLO\text{-}UPTH}$	V_{CC} UVLO rising threshold		5	5.44	5.85	V
$V_{CC\text{-}UVLO\text{-}LOTH}$	V_{CC} UVLO falling threshold		4.68	5.07	5.46	V
MOSFET GATE DRIVER						
$V_{GATE\text{-}HIGH}$	Gate driver output high	With respect to SRC Sinking 100 mA from GATE Force VCC = 9.5 V	8	8.71	9.41	V
$V_{GATE\text{-}LOW}$	Gate driver output low	With respect to SRC Sourcing 100 mA to GATE	10	180	350	mV
t_{RISE}	V_{GATE} rise time	C_{GATE} = 1 nF across GATE and SRC		37		ns
t_{FALL}	V_{GATE} fall time	C_{GATE} = 1 nF across GATE and SRC		30		
$t_{RISE\text{-}PG\text{-}DELAY}$	V_{GATE} low-to-high propagation delay	C_{GATE} = 1 nF across GATE and SRC		91		
$t_{FALL\text{-}PG\text{-}DELAY}$	V_{GATE} high-to-low propagation delay	C_{GATE} = 1 nF across GATE and SRC		112		
CURRENT SOURCE AT ADJ PIN						
$I_{ADJ\text{-}STARTUP}$	Output current of ADJ pin at start-up	V_{ADJ} < 90 mV	14	20	26	µA
CURRENT SENSE AMPLIFIER						
$V_{SEN\text{-}UPPER\text{-}TH}$	V_{SEN} upper threshold over V_{ADJ}	V_{SEN} – V_{ADJ} V_{ADJ} = 0.2 V V_{GATE} at falling edge	17.6	29.3	41	mV
$V_{SEN\text{-}LOWER\text{-}TH}$	V_{SEN} lower threshold over V_{ADJ}	V_{SEN} – V_{ADJ} V_{ADJ} = 0.2 V V_{GATE} at rising edge	–40.7	–29.1	–17.5	
$V_{SEN\text{-}HYS}$	V_{SEN} hysteresis	($V_{SEN\text{-}UPPER\text{-}TH}$ – $V_{SEN\text{-}LOWER\text{-}TH}$)	40.9	60	75.9	
$V_{SEN\text{-}OFFSET}$	V_{SEN} offset with respect to V_{ADJ}	($V_{SEN\text{-}UPPER\text{-}TH}$ + $V_{SEN\text{-}LOWER\text{-}TH}$) / 2	–4	–0.1	4	
OUTPUT OVERVOLTAGE PROTECTION (OVP)						
$V_{OVP\text{-}UPTH}$	Output overvoltage detection upper threshold	V_{OVP} increasing, V_{GATE} at falling edge	1.11	1.19	1.27	V
$V_{OVP\text{-}HYS}$	Output overvoltage detection hysteresis	$V_{OVP\text{-}UPTH}$ – $V_{OVP\text{-}LOTH}$	15	44	80	mV
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown temperature	T_J rising		165		°C
$T_{SD\text{-}HYS}$	Thermal shutdown temperature hysteresis	T_J falling		30		

6.6 Typical Characteristics

$V_P = V_{P\_NOM} = 12$ V

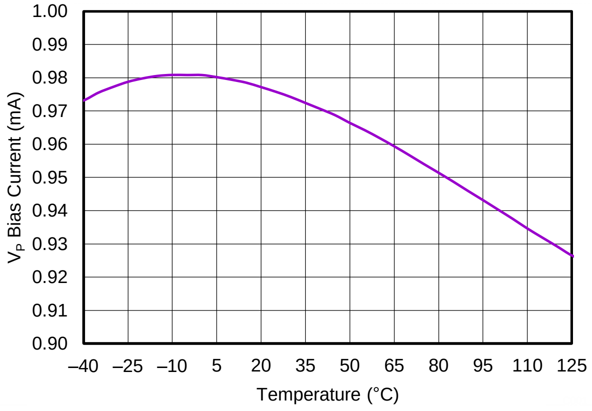


Figure 1. V_P BIAS Current (Non-Switching) vs Temperature

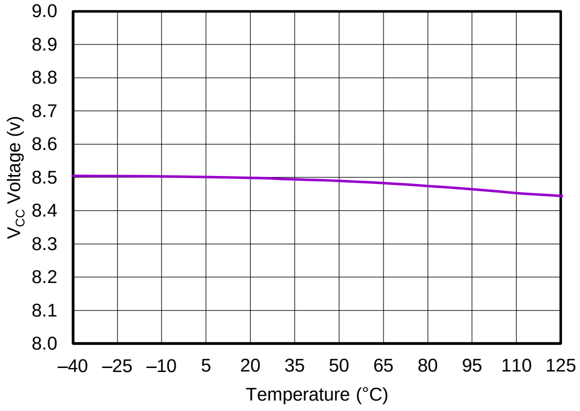


Figure 2. V_{CC} Voltage vs Temperature

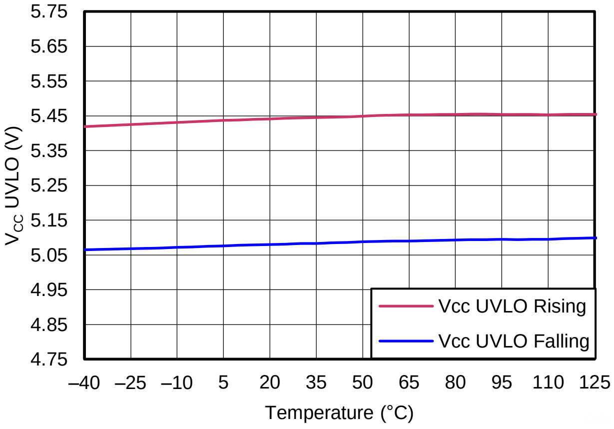


Figure 3. V_{CC} UVLO vs Temperature

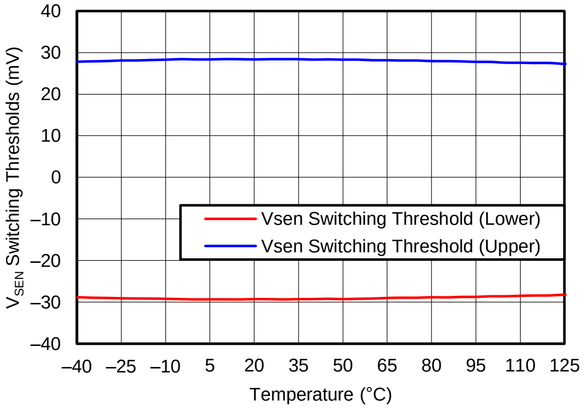


Figure 4. V_{SEN} Switching Thresholds vs Temperature

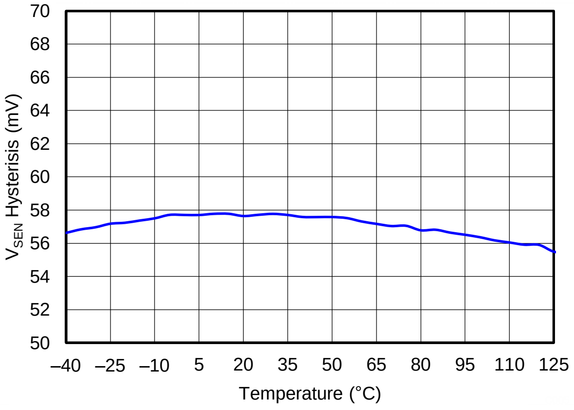


Figure 5. V_{SEN} Hysteresis vs Temperature

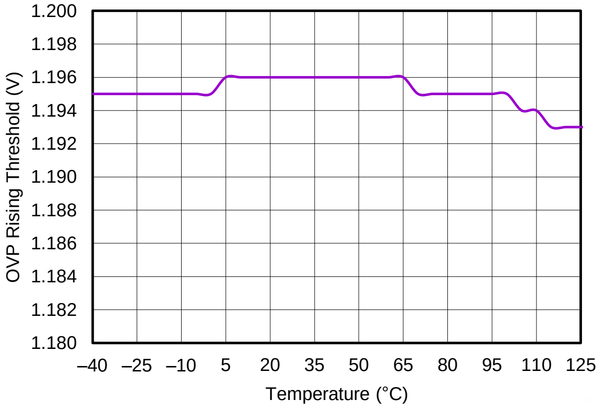


Figure 6. OVP Rising Threshold vs Temperature

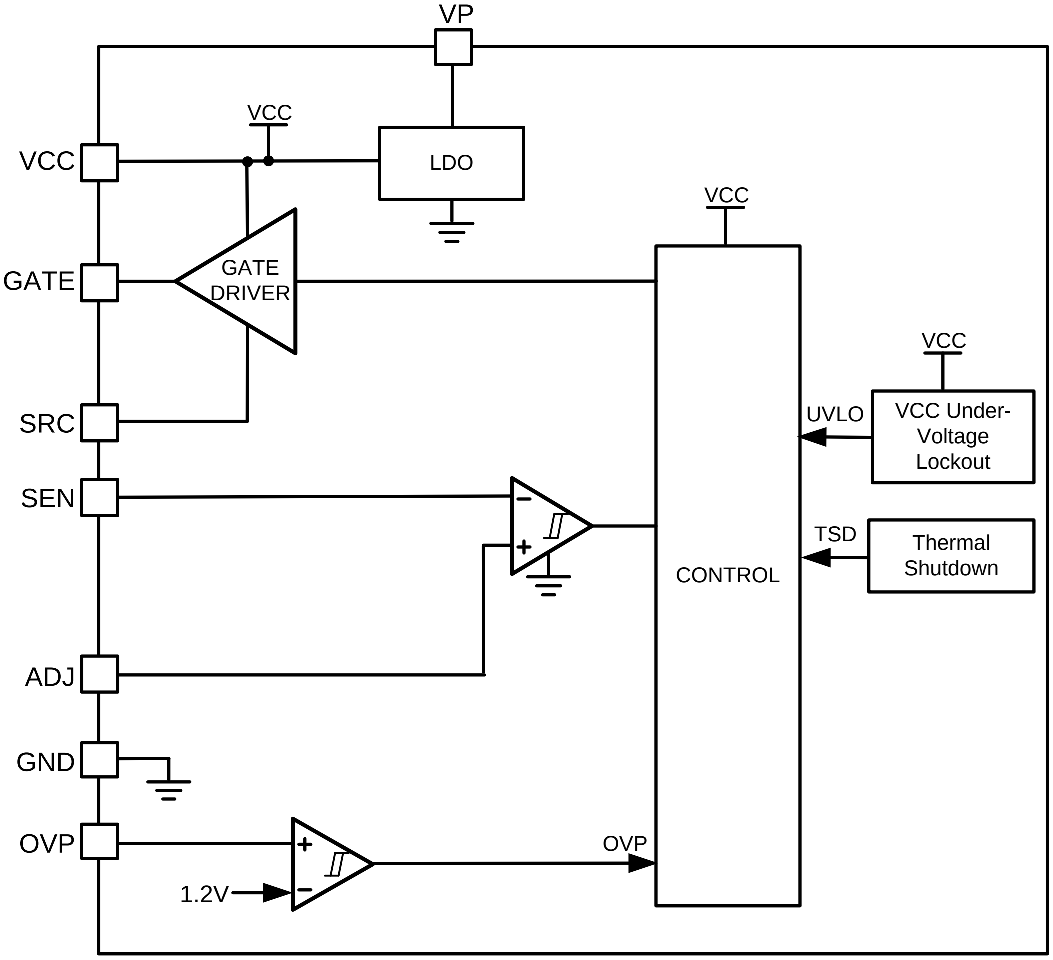
7 Detailed Description

7.1 Overview

The TPS92561 device is a boost controller for phase cut dimmer compatible LED lighting applications. The device incorporates a current sense comparator with a fixed offset, allowing the construction of a hysteretic, off-line converter suitable for driving LEDs in a wide variety of applications.

The inductor peak-to-peak current ripple follows the device reference, the ADJ pin voltage (V_{ADJ}), and is bounded by the SEN pin hysteresis ($V_{SEN\text{-}HYS}$). By using a voltage divider from the rectified AC voltage, the inductor current can be made to follow the line closely and create conversions which result in high power factor and low THD. Boost converters also have an advantage when TRIAC dimming because of their inherent ability to draw continuous current from the line. This eliminates the need for additional hold current circuitry as the converter itself can draw power until the zero crossing point is reached. The continuous input current of a boost also reduces the input EMI filter requirements.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Basics of Operation

The main switch is turned on and off when the SEN comparator reaches trip points in a window around the ADJ reference. In cycle 1, the main switch is on until the current reaches the turn off threshold. In cycle 2, the switch is kept off until the turn on threshold is reached. In Figure 7, $V_{SEN\text{-}UPPER\_TH}$ and $V_{SEN\text{-}LOWER\text{-}TH}$ are assumed to be their typical value of 30 mV.

Feature Description (continued)

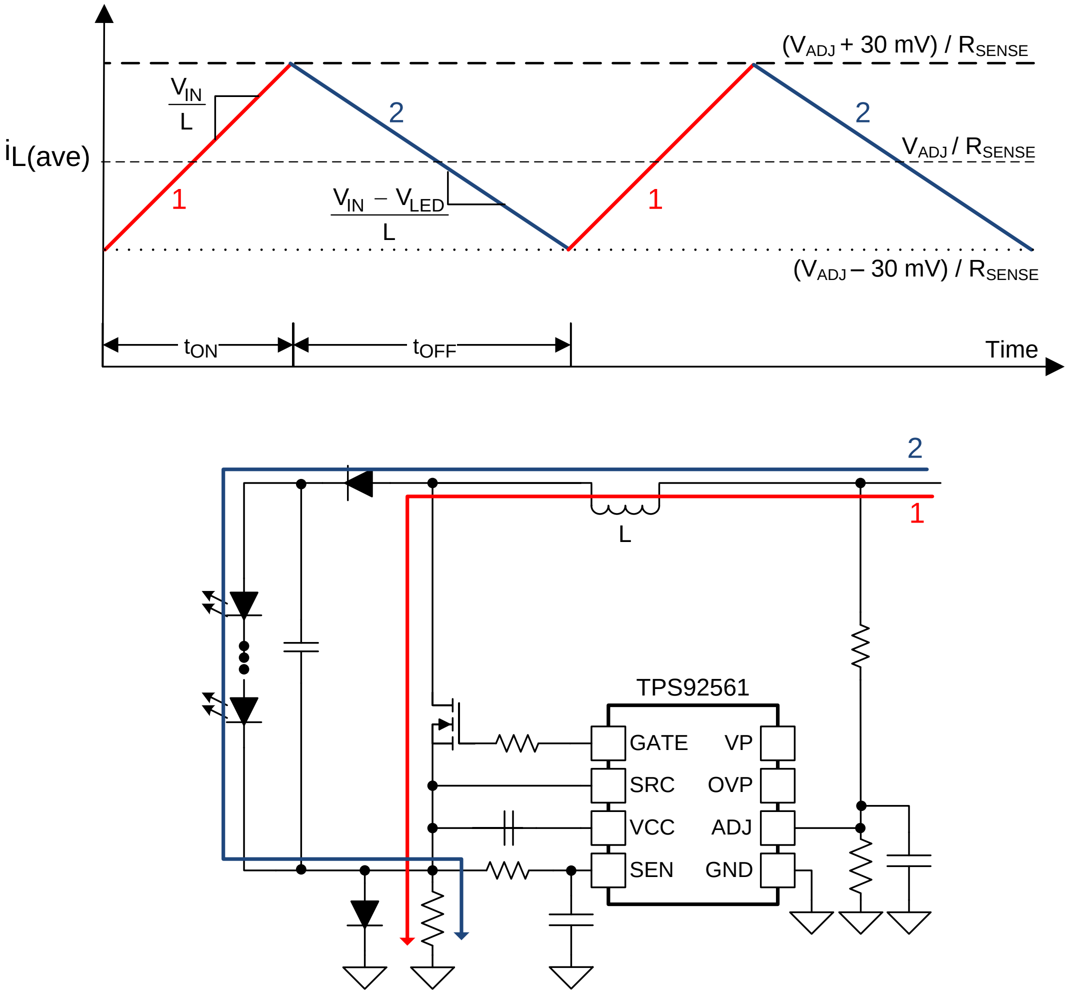


Figure 7. Basics of Hysteretic Boost Operation

Feature Description (continued)

7.3.2 Sample Scope Capture

The main inductor current varies in a window around the ADJ reference voltage:

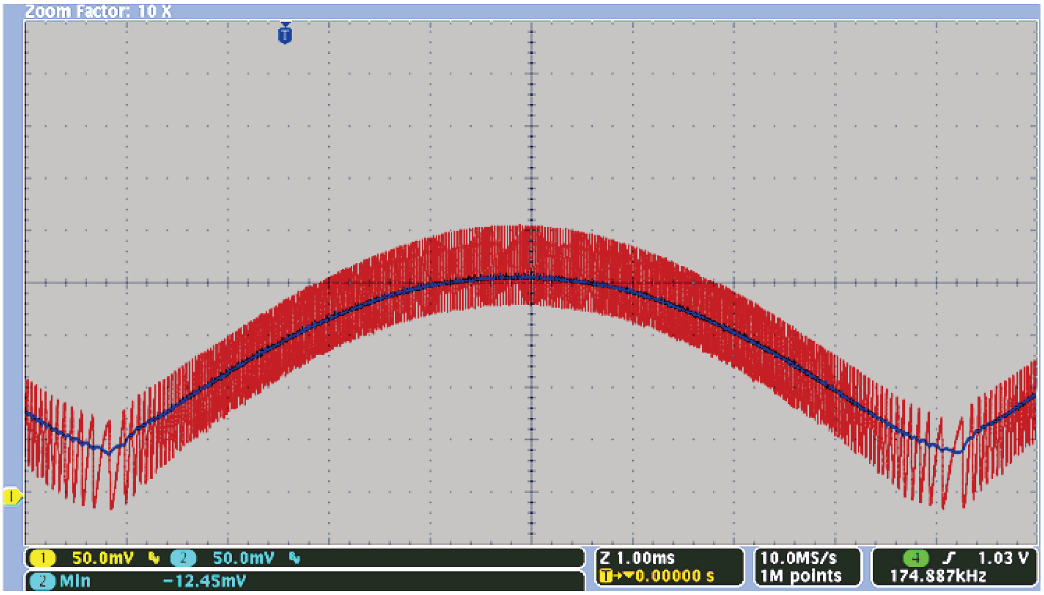


Figure 8. TPS92561 Operation Waveform (1 ms/div)
Yellow: ADJ Voltage (50 mV/div) Blue: R_{SENSE} Voltage (50 mV/div)

7.3.3 Output Current Control (ADJ, SEN)

The TPS92561 power stage design follows two rules:

1. Output current is determined by the ADJ reference voltage, the sense resistor selected, and the converter operating points, V_{IN} and V_{LED}.
2. Output frequency is determined by the inductance value and the SEN pin hysteresis V_{SEN}. For off-line applications, the effective hysteresis must be increased using an R-C filter on the SEN pin.

Because the TPS92561 device does not have leading edge blanking, the SEN pin filter must be used to obtain consistent operation. The SEN pin filter is typically set using an R-C with a corner frequency close to the desired switching frequency. Leading edge blanking was not implemented to allow high-frequency operation in other non-off-line applications.

At start up (V_{ADJ} < 90 mV) a small current is supplied to the V_{ADJ} divider to ensure a reference is available to begin converter switching. When the ADJ voltage is above 90 mV, the current source is shut off.

7.3.4 Overcurrent Protection

The TPS92561 device inherently limits the main switch current, but cannot implement output short circuit protection because of the converter (boost) topology. To implement LED short-circuit protection in a boost converter requires a blocking switch or other means to open the path to the output, which adds significant cost and complexity to the solution and is not commonly used. An input fuse should be used as output overcurrent protection.

7.3.5 Overvoltage Protection (OVP)

Overvoltage protection is implemented using a resistor voltage divider to the output. Note that the output voltage is high (> 200 V) so the resistor divider should contain a high (> 1 MΩ) value. Also use a small cap on OVP.

First pick a value for R18, for example 1.6 MΩ and select the desired overvoltage protection voltage V_{OVP}. Using the $V_{OVP\text{-}UPTH}$ value (1.19 V, typical) the trip point can then be computed using:

Feature Description (continued)

$$R19 = \frac{R18 \times V_{OVP-UPTH}}{V_{OVP} - V_{OVP-UPTH}} \quad (1)$$

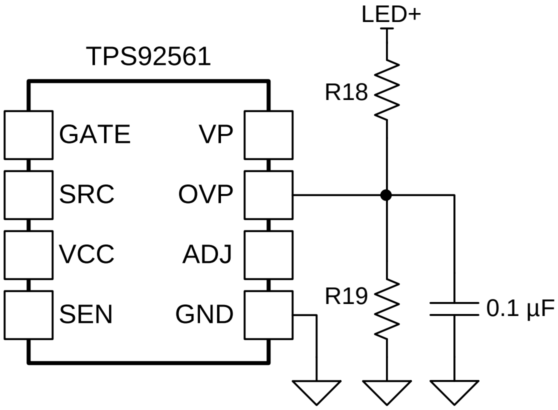


Figure 9. Overvoltage Protection Circuit

When the OVP trip point is reached the converter shuts off until the OVP voltage drops below the level controlled by the OVP hysteresis, $V_{OVP-HYS}$ (44 mV, typical). After OVP is reached, switching begins again when V_{LED} falls to the restart voltage (one $V_{OVP-HYS}$ term ignored):

$$V_{OVP\_RESTART} = V_{OVP} - \left(\frac{V_{OVP-HYS}}{R19}\right) R18 \quad (2)$$

7.3.6 VCC Bias Supply and Start-Up

The TPS92561 device can be configured to obtain bias power in several different configurations: AUX winding from the main inductor (see Figure 13), a linear regulator from the input rectified AC (see Figure 14), or a linear regulator from the output LED voltage (see Figure 15). A linear regulator can be constructed from a resistor, a Zener diode, and a N-Channel MOSFET. Each configuration has benefits and trade-offs.

Table 1. VCC Bias Power Configurations

BIAS CONFIGURATION	DESCRIPTION
Coupled inductor bias with linear regulator start-up (see Figure 13)	Highest efficiency bias choice
	Requires a custom magnetic, which can range in cost similar to an off-the-shelf single coil inductor
	Method to start the TPS92561 device (linear) still required, however, can be undersized for start-up condition only. VCC_{UVLO} has not been engineered to support resistive start-up methods.
Linear regulator from output (see Figure 14)	Lowest efficiency bias choice because output voltage is higher than input
	Ensures fast output turn off due to bias draining output capacitor
	Aids dimming performance under deep dimming, a stable bias is always available
	Lower capacitance value required at VP pin, output capacitor is doubling as VP capacitor
	Can be supplemented with charge pump bias circuit to achieve higher efficiency
Linear regulator from input (see Figure 15)	Better efficiency performance than linear regulator derived from output
	Higher VP capacitor value required

7.3.7 VCC and VP Connection

A bias voltage with a maximum of 42 V is connected to the VP pin to supply the internal 8.3 V (typical) VCC linear regulator. This voltage is also used to drive the main FET gate. Use a FET with a gate threshold at least 750 mV below the VCC voltage. The VCC capacitor ground must be placed at the SEN pin. This ensures the SEN voltage is free of switching spikes that occur at the edge of each switching cycle.

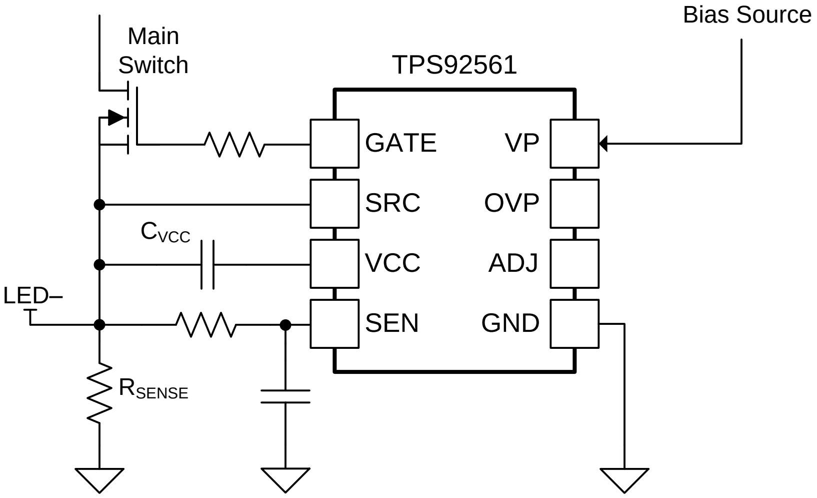


Figure 10. TPS92561 Bias, SRC, and C_{VCC} Connection

7.4 Device Functional Modes

There are no additional functional modes for this device.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Setting the Output Current

Using the desired ADJ reference voltage, the input current can be calculated using Equation 3.

$$I_{in} = \frac{V_{ADJ}}{R_{SENSE}}$$

where

- V_{ADJ} can be DC, rectified AC derived, or other source. (3)

If V_{ADJ} is derived from a voltage divider from the input rectified AC, we can solve for the R9 resistor divider value based on, for example, a V_{ADJ} voltage of 150 mV, an R17 value of 374 Ω, and the average value of the sine wave:

$$R9 = \frac{\left(VIN_{RMS} \times 0.9 \times R17\right)}{V_{ADJ}} - R17 \tag{4}$$

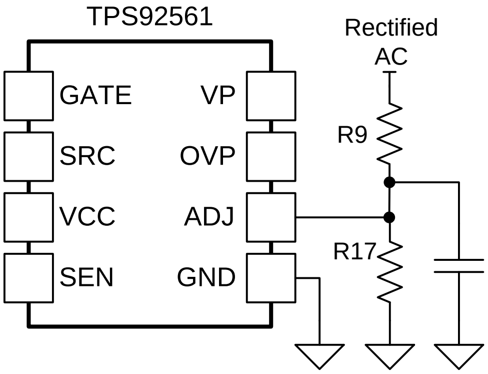


Figure 11. TPS92561 ADJ Connection

To find the R_{SENSE} value, where η is the converter efficiency, assume 0.9.

$$R_{SENSE} = \frac{V_{IN-RMS} \times V_{ADJ} \times \eta}{V_{LED} \times I_{LED}} \tag{5}$$

8.1.2 Selecting an Inductance

The TPS92561 device is hysteretic. Therefore, switching transitions are based on the sensed current in the inductor. There is no direct control of the switching frequency other then the relationship of the comparator hysteresis to the inductor ripple. A typical switching frequency of an off-line converter using a rectified AC injected reference could vary up to 50 kHz over a line cycle. This creates a spread-spectrum effect and helps reduced conducted EMI.

A typical line injected (using a divided down rectified AC as the reference) hysteretic boost converter reaches the peak switching frequency when $V_{LED} = 2 \times V_{RECTIFIED\ AC}$, or when the duty cycle D = 0.5. We call this operating point $V_{IN\text{-}FSW\text{-}PK}$. Use this voltage as the typical operating point for the design equations. Solve for the $V_{IN\text{-}FSW\text{-}PK}$ term based on Equation 6.

Application Information (continued)

$$\frac{V_{LED}}{V_{IN-FSW-PK}} = \frac{1}{1-D} \quad \text{or} \quad V_{IN-FSW-PK} = \frac{V_{LED}}{2} \tag{6}$$

Select the approximate highest desired frequency (for example, $f_{SW\text{-}PK}$ of 65 kHz could be used), then design the SEN pin filter with corner frequency equal to $f_{SW\text{-}PK}$. The filter and the internal hysteresis define the inductor ripple for a given inductance. This has the effect of increasing the SEN pin hysteresis $V_{SEN\text{-}HYS\text{-}2}$ to approximately 140 mV. Select a C12 value between 1000 and 4700 pF. Solve for the resistor R12 in the filter based on Equation 7.

$$R_{12} = \frac{1}{2\pi \times f_{SW-PK} \times C_{12}} \tag{7}$$

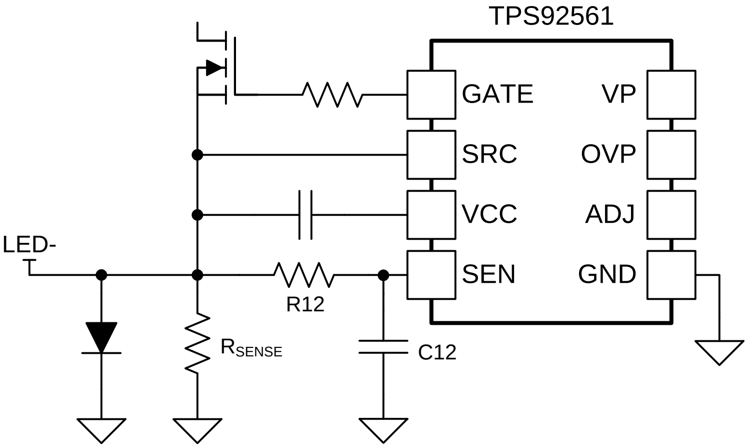


Figure 12. Current Sense

With the effective hysteresis, calculate the inductor peak-to-peak, $\Delta i_{L\text{-}PP}$ ripple current using:

$$\Delta i_{L-PP} = \frac{V_{SEN-HYS-2}}{R_{SENSE}} \tag{8}$$

To find the converter inductance, L, substitute into:

$$L = \frac{V_{IN-FSW-PK} \times D \times \left(\frac{1}{f_{SW-PK}}\right)}{\Delta i_{L-PP}} \tag{9}$$

To further aid in the converter design, see the TPS92561 design tool (SLUC517).

8.1.3 Important Design Consideration: Diode in Parallel With Sense Resistance

Figure 12 shows a diode in use in parallel with the R_{SENSE} resistor. The diode clamps the SEN pin voltage when the boost converter is first powered up. Because a boost converter utilizes a diode connected to the output, the output capacitor is charged immediately when power is applied.

CAUTION

The current charging the output capacitor when V_{IN} is applied flows through the sense resistors, and if it is not clamped by the diode, can exceed the TPS92561 SEN pin rating, which may damage the device.

8.1.4 Gate Driver Operation

An additional aid to converter operation and radiated EMI is to slow the main FET switching speed. This can be accomplished by adding a resistor in series with the FET gate. A fast turn off diode across the resistor could also be implemented to improve efficiency. For off-line designs, use a gate resistance value ≥ 75 Ω.

Application Information (continued)

As in all power converters grounding and layout are key considerations. Give careful attention to the layout of the sense resistors, GND pin, VCC, and SRC connections, as well as the FET Gate and Source connections. All should follow short and low-inductance paths. For examples, see the TPS92561 EVM User's Guide, *Using the TPS92561 Off-Line Boost LED Driver* (SLUUAU9).

8.1.5 Output Bulk Capacitor

The required output bulk capacitor, C_{BULK}, stores energy during the input voltage zero crossing interval and limits the twice the line frequency ripple component flowing through the LEDs. Equation 10 describes the calculation of the output capacitor value.

$$C_{BULK} \geq \frac{P_{IN}}{4\pi \times f_L \times R_{LED} \times V_{LED} \times I_{LED(ripple)}}$$

where

- R_{LED} is the dynamic resistance of LED string
- $I_{LED(ripple)}$ is the peak-to-peak LED ripple current
- f_L is line frequency (10)

R_{LED} is found by computing the difference in LED forward voltage divided by the difference in LED current for a given LED using the manufacturer's V_F versus I_F curve. For more details, see application report, *AN-1656 Design Challenges of Switching LED Drivers* (SNVA253).

In typical applications, the solution size becomes a limiting factor and dictates the maximum dimensions of the bulk capacitor. When selecting an electrolytic capacitor, manufacturer recommended de-rating factors should be applied based on the worst case capacitor ripple current, output voltage, and operating temperature to achieve the desired operating lifetime.

8.1.6 Phase Dimming

After following the design procedure for a TPS92561 non-dimming design, the creation of a TRIAC dimmer compatible design only requires the addition of an input snubber (R-C), as shown in Figure 15. Ideally, a capacitor value of 3× the input filter capacitance would be implemented to ensure sufficient damping of the input filter resonance. However, capacitance values as low as 2× tested successfully. If the input voltage is used to provide the converter reference, dimming occurs naturally with the decreasing ADJ set point and decreased power transfer due to shorter line-cycle conduction times.

8.1.7 Example Circuits

Target LED lamp applications include:

- A-15, A-19, A-21, A-23
- R-20, R-25, R-27, R-30, R-40
- PS-25, PS-30, PS-35
- BR-30, BR-38, BR-40
- PAR-20, PAR-30, PAR-30L
- MR-16, GU-10
- G-25, G-30, G-40

Applications also include: fluorescent replacement, recessed (canister) type lighting replacement, and new LED-specific lighting form factors.

Application Information (continued)

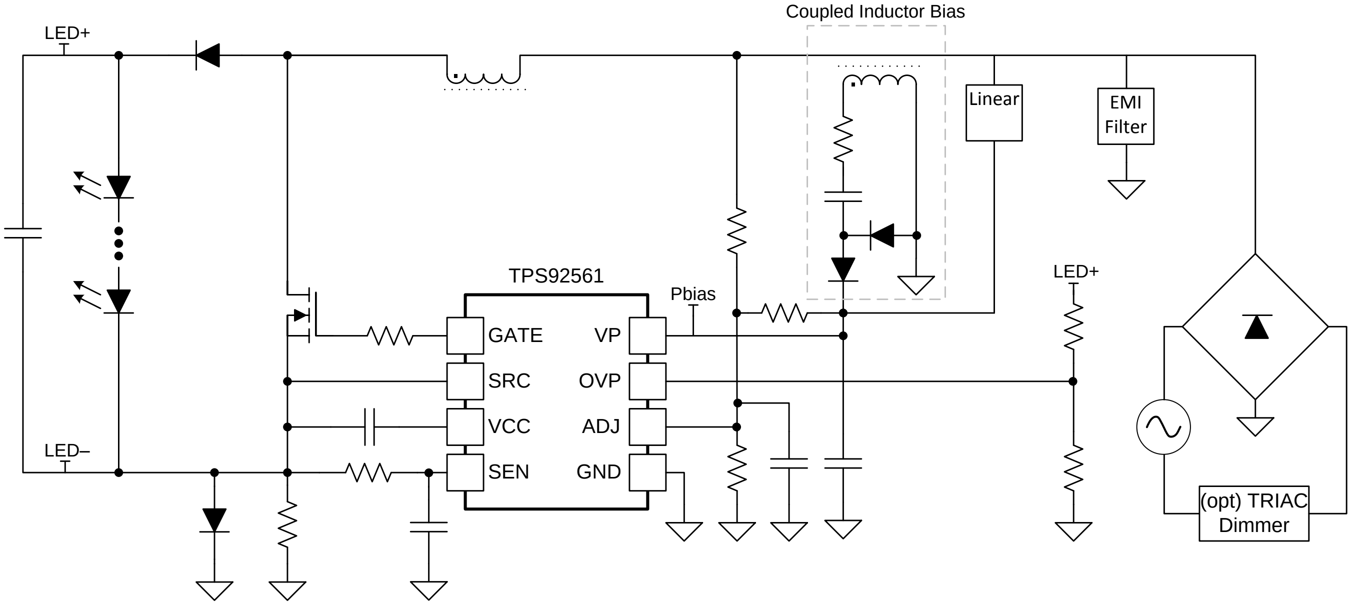


Figure 13. Offline Boost Configuration With Auxiliary Winding and Linear Regulator for Start-Up

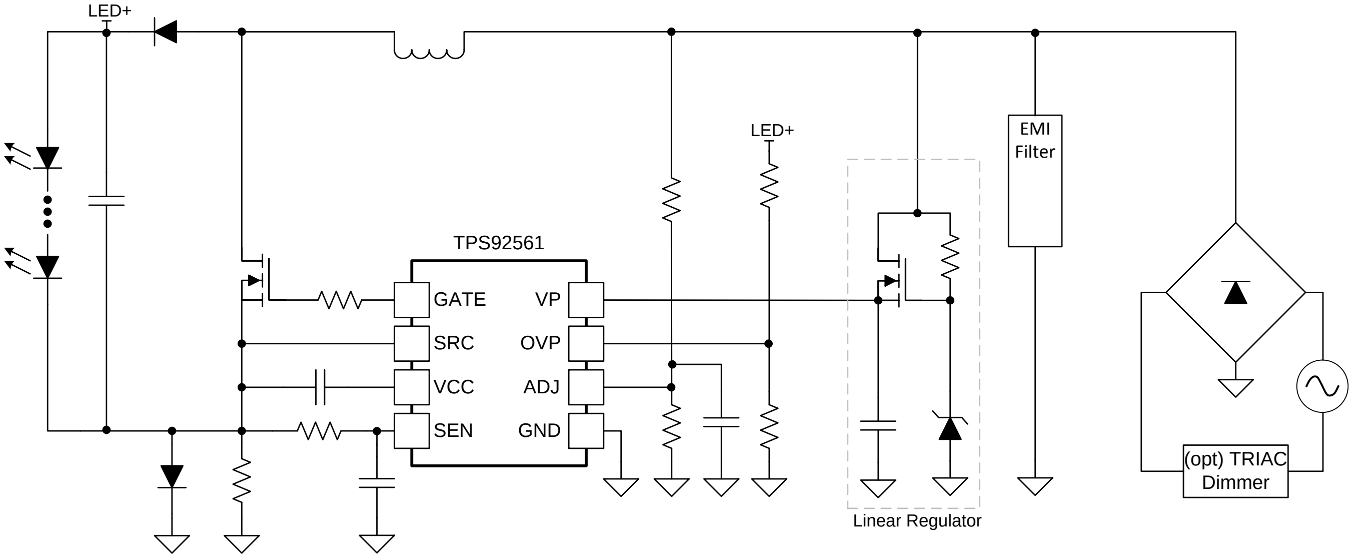


Figure 14. Offline Boost With Linear Regulator from Input Rectified AC

Application Information (continued)

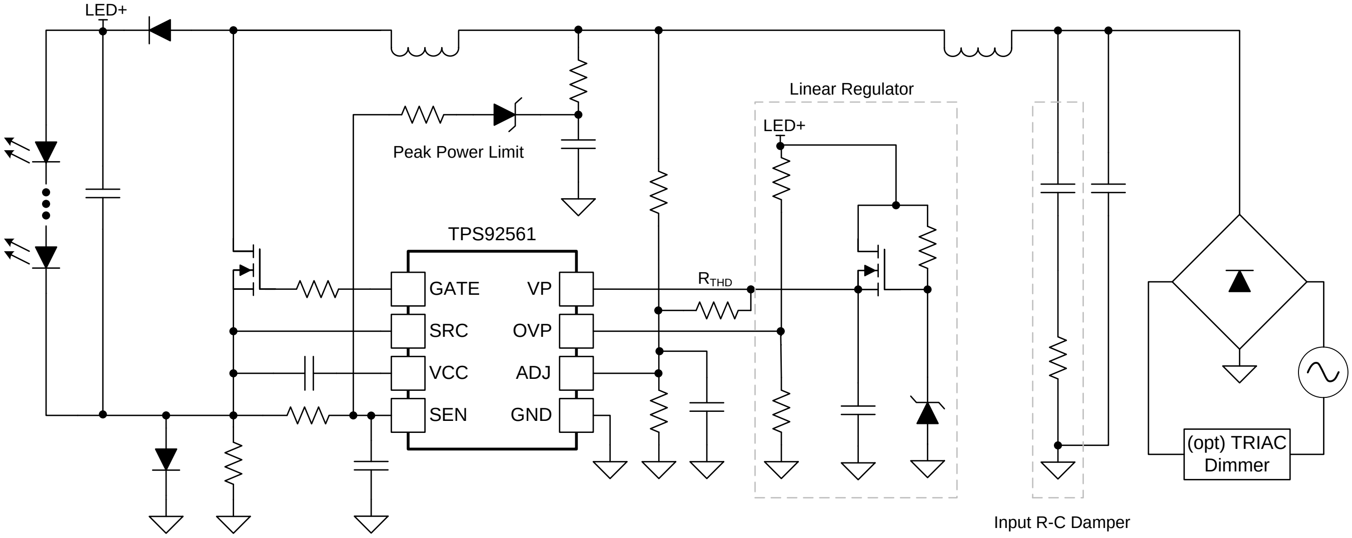


Figure 15. Offline Boost With Linear Regulator from V_{LED+},THD Improvement Resistor, Peak Power Limit Circuit, EMI Filter, and Snubber for TRIAC Dimming

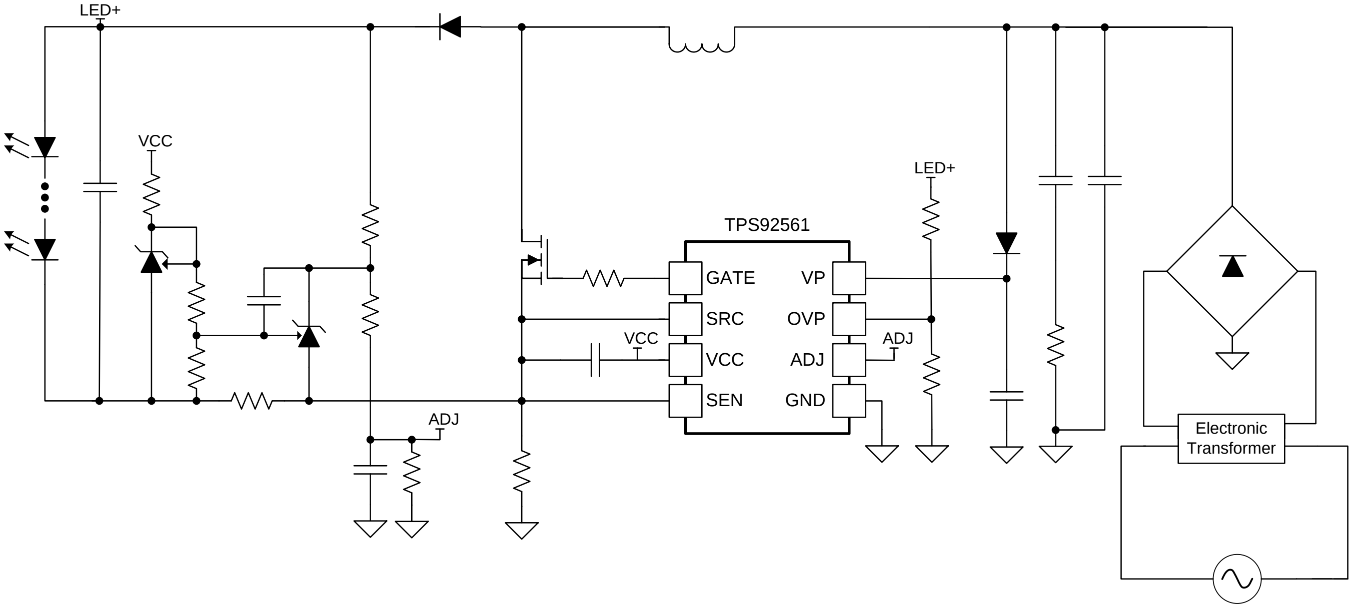


Figure 16. Closed-Loop Regulated E-Transformer Compatible, Non-TRIAC Dimmable Boost for AR111 and MR16 Lamps

8.2 Typical Applications

8.2.1 Offline Boost Schematic for Design Example

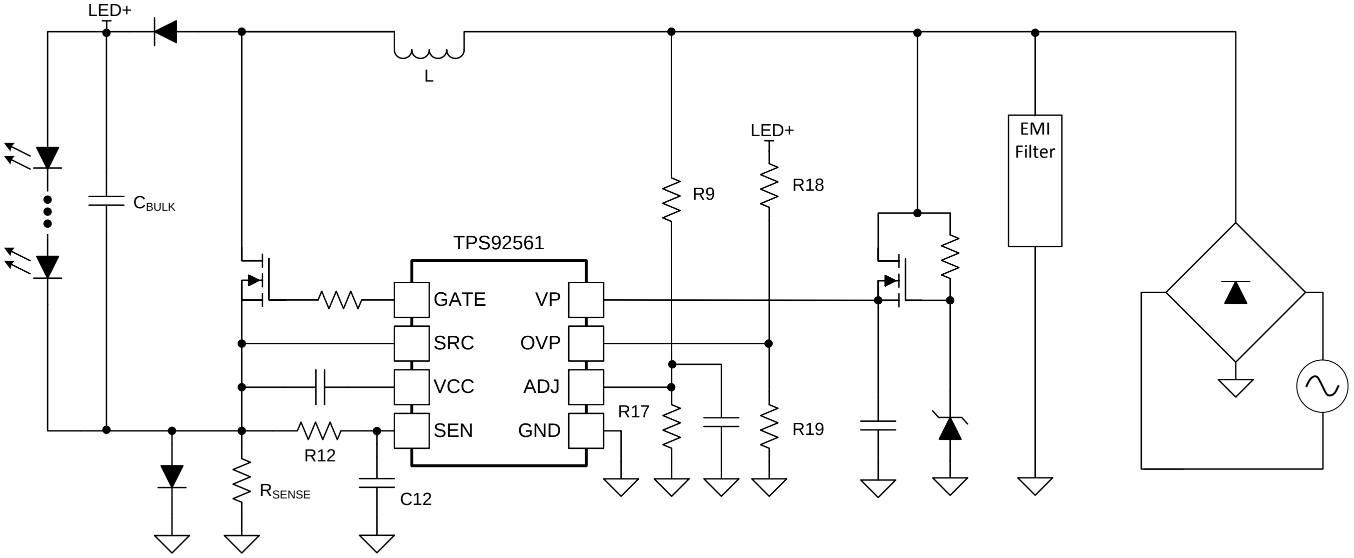


Figure 17. Offline Boost Schematic

8.2.1.1 *Design Requirements*

- RMS Input Voltage: $V_{IN\text{-}RMS}$
- LED Stack Voltage: V_{LED}
- LED Current: I_{LED}
- LED String Total Dynamic Resistance: R_{LED}
- LED Ripple Current: $I_{LED(ripple)}$
- Maximum Switching Frequency: $f_{SW\text{-}PK}$
- Over-voltage Protection Level: V_{OVP}
- Approximate Efficiency: η

8.2.1.2 *Detailed Design Procedure*

8.2.1.2.1 Set the LED Current

8.2.1.2.1.1 *Calculate ADJ Pin Resistors*

Calculate the ADJ pin resistors by choosing an ADJ voltage and a value for R17. R9 can then be calculated using Equation 11.

$$R9 = \frac{V_{IN\text{-}RMS} \times 0.9 \times R17}{V_{ADJ}} \tag{11}$$

8.2.1.2.1.2 *Calculate the Current Sense Resistor*

The current sense resistor R_{SENSE} can be calculated with Equation 12.

$$R_{SENSE} = \frac{V_{IN\text{-}RMS} \times \eta \times V_{ADJ}}{V_{LED} \times I_{LED}} \tag{12}$$

8.2.1.2.1.3 *Calculate the SEN Pin Series Resistance*

The series resistance between the SEN pin and R_{SENSE} can be calculated by choosing a value of C12 and using Equation 13.

Typical Applications (continued)

$$R12 = \frac{1}{2\pi \times f_{SW\text{-}PK} \times C12} \quad (13)$$

8.2.1.2.2 Calculate OVP Pin Resistors

The OVP pin resistor values can be calculated by choosing a high value for R18 (in the MΩ range) and calculating the value for R19 with Equation 14.

$$R19 = \frac{R18 \times 1.19V}{V_{OVP} - 1.19V} \quad (14)$$

The output voltage falling voltage level for re-start can then be calculated using Equation 15.

$$V_{OVP\_RESTART} = V_{OVP} - \frac{44mV \times R18}{R19} \quad (15)$$

8.2.1.2.3 Calculate Inductor Value and Ripple Current

The inductor ripple current is based on the value of R_{SENSE}. The ripple current can be found using Equation 16.

$$\Delta i_{L\text{-}PP} = \frac{140mV}{R_{SENSE}} \quad (16)$$

The input voltage where the maximum switching frequency occurs ($V_{IN\text{-}FSW\text{-}PK}$) is required for calculating the inductor value and can be found using Equation 17.

$$V_{IN\text{-}FSW\text{-}PK} = \frac{V_{LED}}{2} \quad (17)$$

Now the inductor value can be calculated using the simplified Equation 18.

$$L = \frac{V_{IN\text{-}FSW\text{-}PK} \times \left(\frac{1}{f_{SW\text{-}PK}}\right)}{2 \times \Delta i_{L\text{-}PP}} \quad (18)$$

8.2.1.2.4 Calculate the Output Capacitor Value

The minimum output capacitor required to meet the LED current ripple requirements can be found using Equation 19.

$$C_{BULK} \geq \frac{P_{IN}}{4\pi \times f_L \times R_{LED} \times V_{LED} \times I_{LED(ripple)}} \quad (19)$$

In this equation f_L is the rectified line frequency or double the native line frequency.

Typical Applications (continued)

8.2.2 11-W, 120-VAC Input, 225-V Output, Offline Boost Design Example

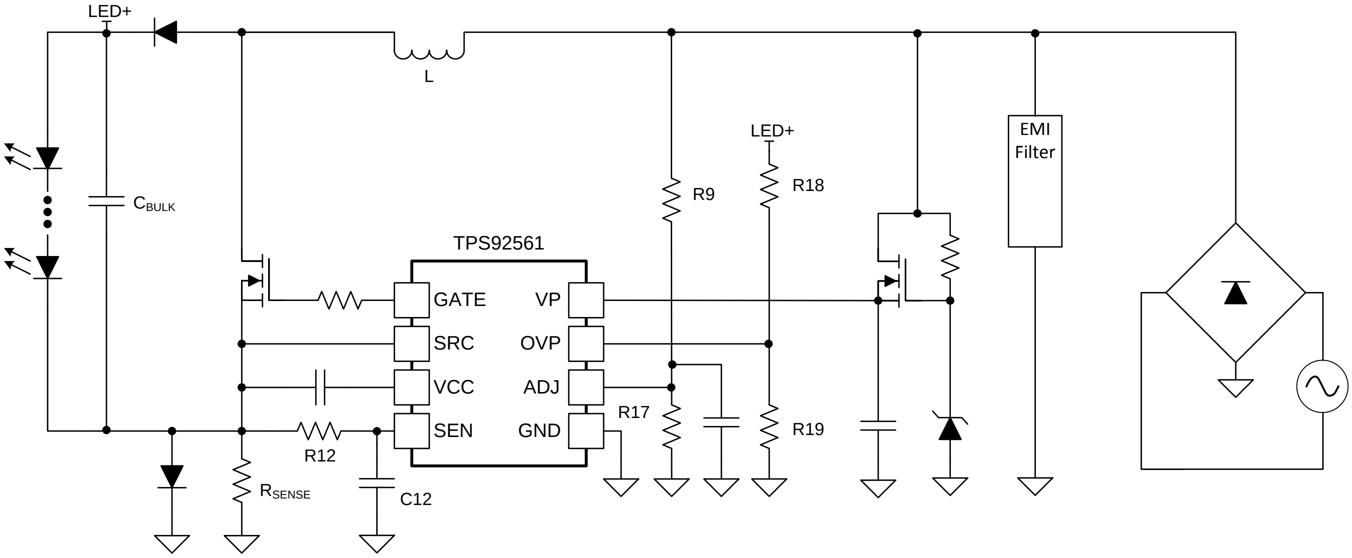


Figure 18. 11 W, 120-VAC Input, 225-V Output, Offline Boost Schematic

8.2.2.1 Design Requirements

- $V_{IN\text{-}RMS}$ = 120 V, 60 Hz
- V_{LED} = 225 V
- I_{LED} = 50 mA
- R_{LED} = 80 Ω
- $I_{LED(ripple)} \leq$ 25 mA
- $f_{SW\text{-}PK}$ = 65 kHz
- V_{OVP} = 250 V
- Approximate Efficiency: η = 0.9

8.2.2.2 Detailed Design Procedure

8.2.2.2.1 Set the LED Current

8.2.2.2.1.1 Calculate ADJ Pin Resistors

Calculate the ADJ pin resistors by choosing an ADJ voltage and a value for R17. Choose an ADJ voltage of 150 mV and a low value of 374 Ω for R17 to get a reasonable value for R9. R9 can then be calculated using Equation 20.

$$R9 = \frac{V_{IN\text{-}RMS} \times 0.9 \times R17}{V_{ADJ}} = \frac{120V \times 0.9 \times 374\Omega}{150mV} = 268.9k\Omega \tag{20}$$

Choose the nearest standard value of **R9 = 267kΩ**.

8.2.2.2.1.2 Calculate the Current Sense Resistor

The current sense resistor R_{SENSE} can be calculated with Equation 21.

$$R_{SENSE} = \frac{V_{IN\text{-}RMS} \times \eta \times V_{ADJ}}{V_{LED} \times I_{LED}} = \frac{120V \times 0.9 \times 150mV}{225V \times 50mA} = 1.44\Omega \tag{21}$$

Choose the nearest standard value of **R_{SENSE} = 1.43 Ω**.

Typical Applications (continued)

8.2.2.2.1.3 Calculate the SEN Pin Series Resistance

The series resistance between the SEN pin and R_{SENSE} can be calculated by choosing a value of 2.2 nF for C12 and using Equation 22.

$$R12 = \frac{1}{2\pi \times f_{SW\text{-}PK} \times C12} = \frac{1}{2\pi \times 65kHz \times 2.2nF} = 1113\Omega \tag{22}$$

Choose the nearest standard value of **R12 = 1.1 kΩ**.

8.2.2.2.2 Calculate OVP Pin Resistors

The OVP pin resistor values can be calculated by choosing a value for R18 of 1.6MΩ and calculating the value for R19 with Equation 23.

$$R19 = \frac{R18 \times 1.19V}{V_{OVP} - 1.19V} = \frac{1.6M\Omega \times 1.19V}{250V - 1.19V} = 7.65k\Omega \tag{23}$$

Choose the nearest standard value of **R19 = 7.68kΩ**. The output voltage falling voltage level for re-start can then be calculated using Equation 24.

$$V_{OVP\_RESTART} = V_{OVP} - \frac{44mV \times R18}{R19} = 250V - \frac{44mV \times 1.6M\Omega}{7.68k\Omega} = 240.8V \tag{24}$$

8.2.2.2.3 Calculate Inductor Value and Ripple Current

The inductor ripple current is based on the value of R_{SENSE}. The ripple current for this application can be found using Equation 25.

$$\Delta i_{L\text{-}PP} = \frac{140mV}{R_{SENSE}} = \frac{140mV}{1.43\Omega} = 97.9mA \tag{25}$$

The input voltage where the maximum switching frequency occurs ($V_{IN\text{-}FSW\text{-}PK}$) is required for calculating the inductor value and can be found using Equation 26.

$$V_{IN\text{-}FSW\text{-}PK} = \frac{V_{LED}}{2} = \frac{225V}{2} = 112.5V \tag{26}$$

Now the inductor value can be calculated using the simplified Equation 27.

$$L = \frac{V_{IN\text{-}FSW\text{-}PK} \times \left(\frac{1}{f_{SW\text{-}PK}}\right)}{2 \times \Delta i_{L\text{-}PP}} = \frac{112.5V \times \left(\frac{1}{65kHz}\right)}{2 \times 97.9mA} = 8.8mH \tag{27}$$

Choose the next highest standard inductor value of **L = 10mH**.

8.2.2.2.4 Calculate the Output Capacitor Value

The minimum output capacitor required to meet 25mA LED current ripple can be found using Equation 28.

$$C_{BULK} \geq \frac{P_{IN}}{4\pi \times f_L \times R_{LED} \times V_{LED} \times I_{LED(ripple)}} = \frac{12.5W}{4\pi \times 120Hz \times 80\Omega \times 225V \times 25mA} = 18\mu F \tag{28}$$

In this equation f_L is the rectified line frequency of 120 Hz. Choose the next highest standard capacitor value of $\mathbf{C_{BULK} = 22\mu F}$.

Typical Applications (continued)

8.2.2.3 Application Curve

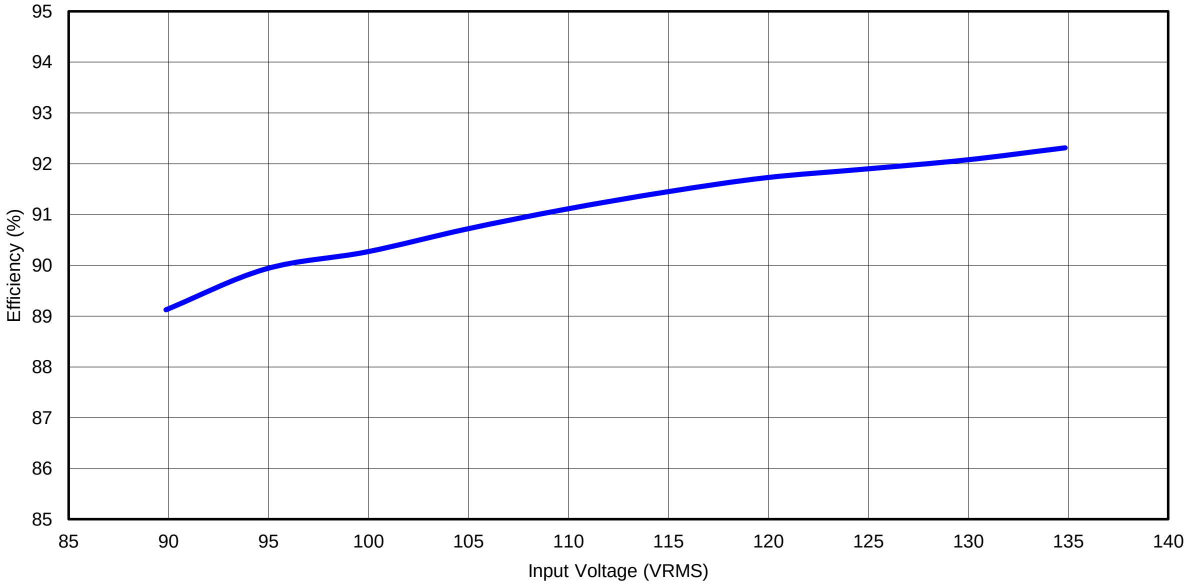


Figure 19. Efficiency vs Input Voltage

9 Power Supply Recommendations

Use an AC power supply capable of 120-VAC and at least 12 W of output power.

10 Layout

10.1 Layout Guidelines

The VP input capacitor, OVP resistors, and ADJ resistors/capacitor should be placed as close to the IC as possible. The VCC capacitor, GATE resistor, and SEN capacitor should also be placed close to the device. Minimize the switching node area (connection between Q, L, and D) and keep the discontinuous current switching path as short as possible. This includes the loop formed by Q, R_{SENSE}, and the diode D. The ground connections for the TPS92561, the SEN filter capacitor, and R_{SENSE} should all be tide closely together with a solid ground plane.

10.2 Layout Example

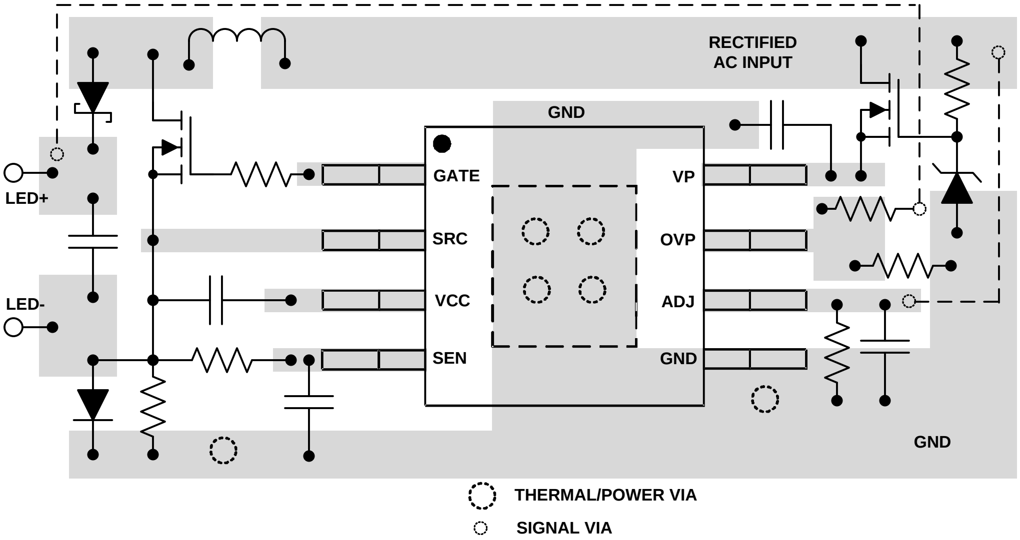


Figure 20. Layout Recommendation

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *Using the TPS92561 Off-Line Boost LED Driver*, SLUUAU9.
- *AN-1656 Design Challenges of Switching LED Drivers*, SNVA253.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

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11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS92561DGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	92561	Samples
TPS92561DGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	92561	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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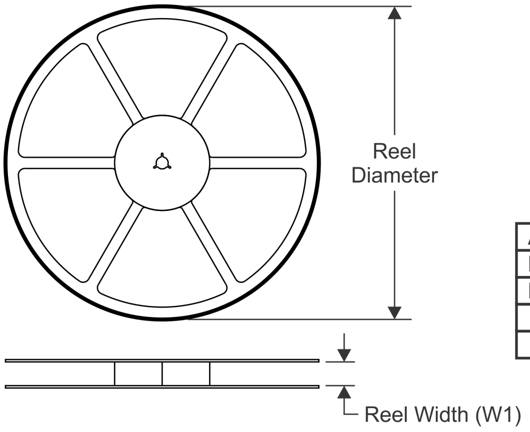
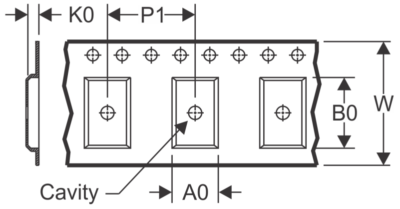
TAPE AND REEL INFORMATION

REEL DIMENSIONS

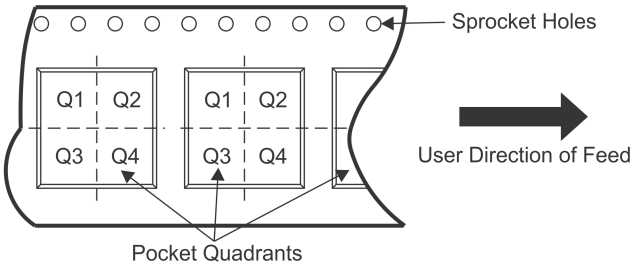


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

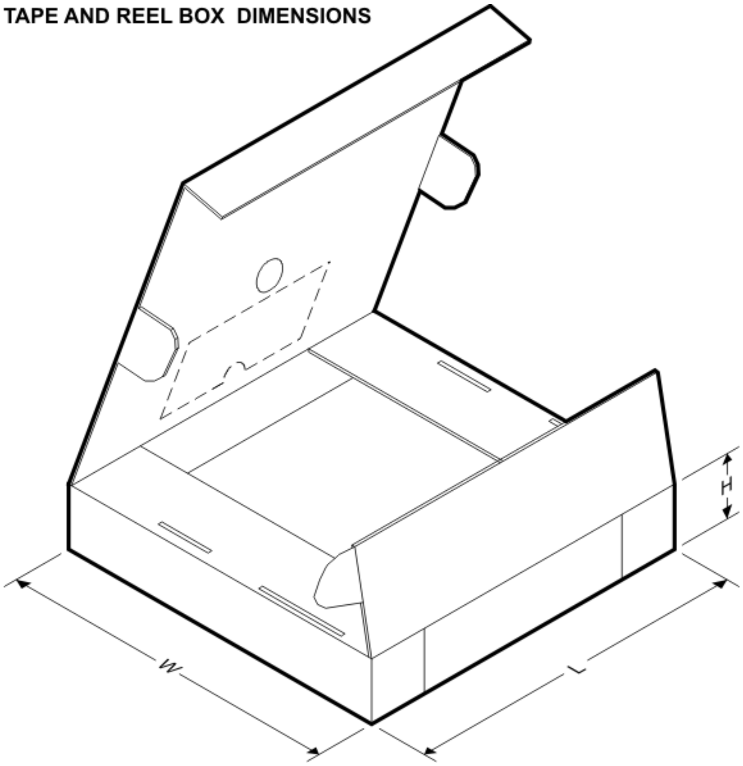
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS92561DGNR	MSOP-PowerPAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

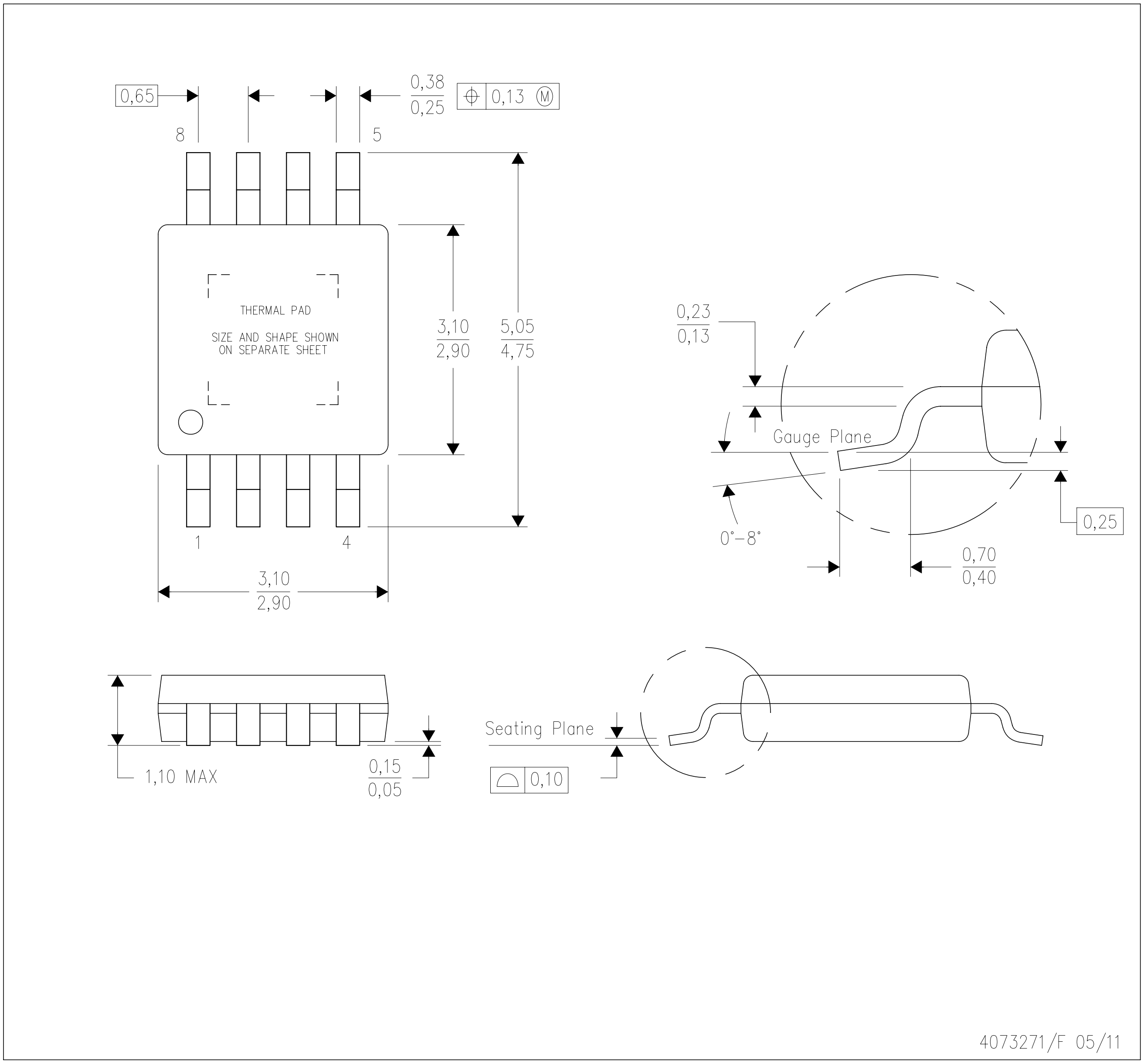
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS92561DGNR	MSOP-PowerPAD	DGN	8	2500	366.0	364.0	50.0

DGN (S-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO–187 variation AA–T

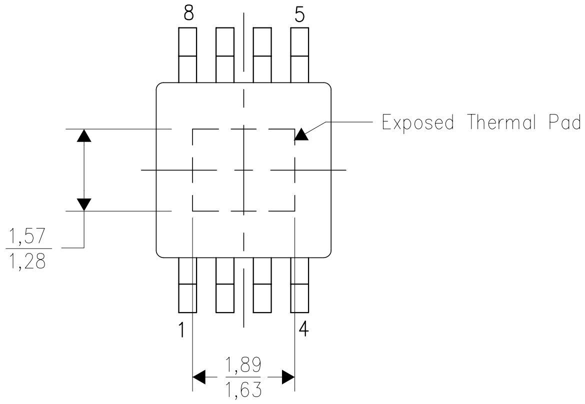
DGN (S-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



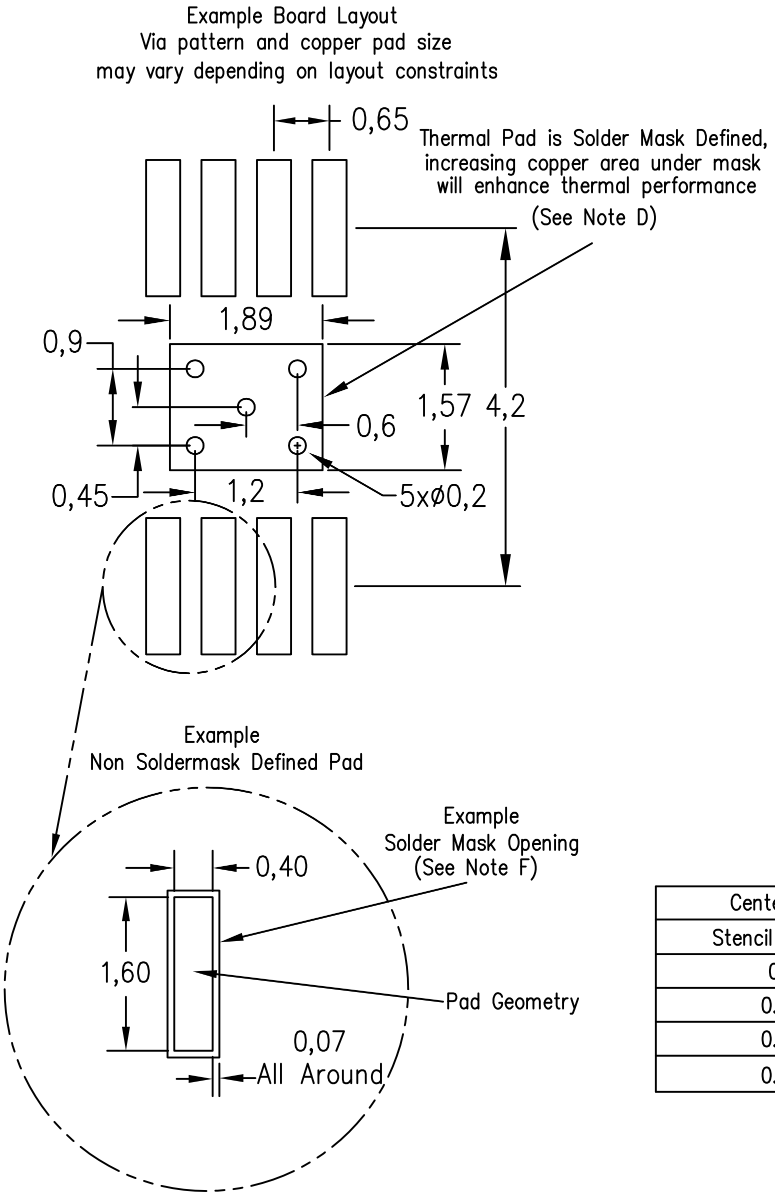
Top View

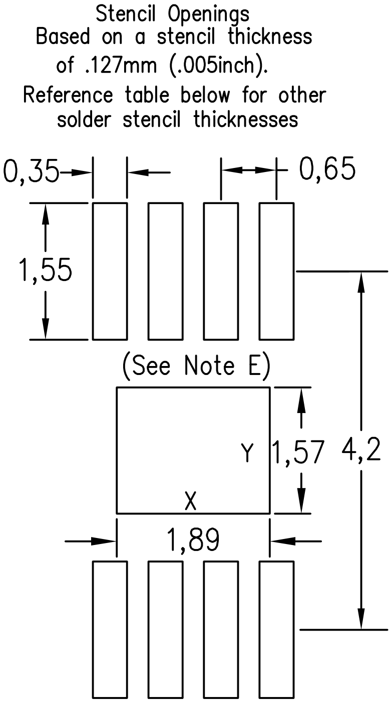
Exposed Thermal Pad Dimensions

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DGN (R-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE





Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.0	1.7
0.127mm	1.89	1.57
0.152mm	1.75	1.45
0.178mm	1.65	1.35

4207737-2/F 02/13

NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
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Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
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