CSD87351Q5D 同步降压 NexFET™ 电源块

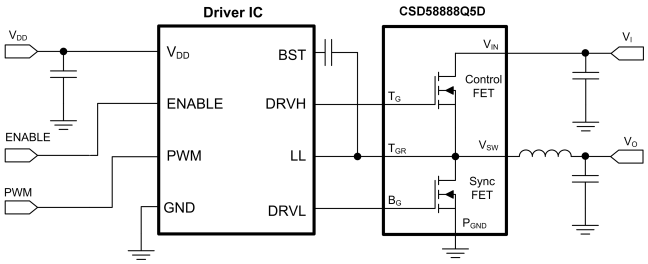
1 特性

- 半桥电源块
- 电流 20A 时，系统效率达到 90%
- 高达 32A 的运行电流
- 高频工作（高达 1.5MHz）
- 高密度 SON 5mm × 6mm 封装
- 针对 5V 栅极驱动进行了优化
- 开关损耗较低
- 超低电感封装
- 符合 RoHS 标准
- 无卤素
- 无铅引脚镀层

2 应用范围

- 同步降压转换器
  - 高频 应用
  - 高电流、低占空比 应用
- 多相位同步降压转换器
- 负载点 (POL) 直流 - 直流转换器
- IMVP、VRM 和 VRD 应用

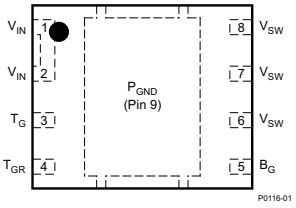
典型电路



3 说明

此CSD87351Q5D NexFET™电源块是面向同步降压应用 的优化设计方案，能够以 5mm × 6mm 的小巧外形提供高电流、高效率以及高频率性能。该产品针对 5V 栅极驱动 应用进行了优化，可提供一套灵活的解决方案，在与来自外部控制器/驱动器的任一 5V 栅极驱动配套使用时，均可提供高密度电源。

俯视图

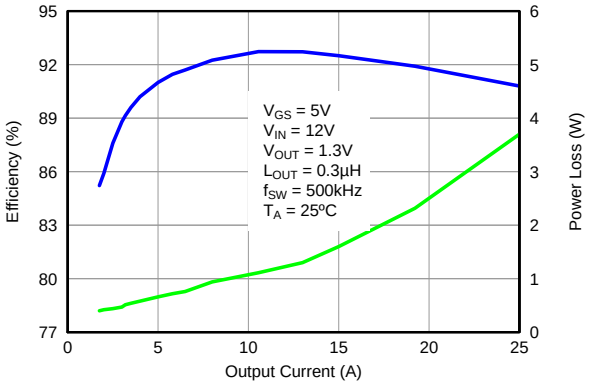


器件信息(1)

器件	包装介质	数量	封装	运输
CSD87351Q5D	13 英寸卷带	2500	SON 5.00mm × 6.00mm 塑料封装	卷带封装

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

典型电源块效率与功率损耗



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision D (January 2012) to Revision E — **Page**

- Added note for I_{DM} in the *Absolute Maximum Ratings* table ... 3
- Changed part number in Figure 32 ... 13
- 已添加 *器件和文档支持*部分 ... 17

Changes from Revision C (October 2011) to Revision D — **Page**

- 添加了特性项目：高达 32A 的运行电流 ... 1

Changes from Revision B (September 2011) to Revision C — **Page**

- 将“DIM a”以毫米为单位的最大值由 1.55 更改为 1.5，将以英寸为单位的最大值由 0.061 更改为 0.059 ... 18

Changes from Revision A (August 2011) to Revision B — **Page**

- Remove $Z_{DS(on)}$ Max ... 4
- Remove $Z_{DS(on)}$ Max ... 12
- Added Electrical Performance bullet ... 15

Changes from Original (March 2011) to Revision A — **Page**

- Replaced $R_{DS(on)}$ with $Z_{DS(on)}$ ... 4
- Added Equivalent System Performance section ... 10

5 Specifications

5.1 Absolute Maximum Ratings

T_A = 25°C (unless otherwise noted)(1)

PARAMETER		CONDITIONS	MIN	MAX	UNIT
	Voltage	V_{IN} to P_{GND}	–0.8	30	V
		T_G to T_{GR}	–8	10	
		B_G to P_{GND}	–8	10	
I_{DM}(2)	Pulsed current rating		96		A
P_D	Power dissipation		12		W
E_{AS}	Avalanche energy	Sync FET, I_D = 87 A, L = 0.1 mH	378		mJ
		Control FET, I_D = 44 A, L = 0.1 mH	87		
T_J	Operating junction		–55	150	°C
T_{STG}	Storage temperature		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Pulse duration ≤ 50 µs. Duty cycle ≤ 0.01%.

5.2 Recommended Operating Conditions

T_A = 25°C (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	MAX	UNIT
V_{GS}	Gate drive voltage		4.5	8	V
V_{IN}	Input supply voltage			27	V
f_{SW}	Switching frequency	C_{BST} = 0.1 µF (min)	200	1500	kHz
	Operating current			32	A
T_J	Operating temperature			125	°C

5.3 Power Block Performance

T_A = 25°C (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
P_{LOSS} (1)	Power loss	V_{IN} = 12 V, V_{GS} = 5 V, V_{OUT} = 1.3 V, I_{OUT} = 20 A, f_{SW} = 500 kHz, L_{OUT} = 0.3 µH, T_J = 25°C		2.5		W
I_{QVIN}	V_{IN} quiescent current	T_G to T_{GR} = 0 V, B_G to P_{GND} = 0 V		10		µA

(1) Measurement made with six 10-µF (TDK C3216X5R1C106KT or equivalent) ceramic capacitors placed across V_{IN} to P_{GND} pins and using a high-current 5-V driver IC.

5.4 Thermal Information

T_A = 25°C (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (min Cu)(1)(2)			119	°C/W
	Junction-to-ambient thermal resistance (max Cu)(1)(2)			62	
$R_{\theta JC}$	Junction-to-case thermal resistance (top of package)(2)			25	°C/W
	Junction-to-case thermal resistance (P_{GND} pin)(2)			2.3	

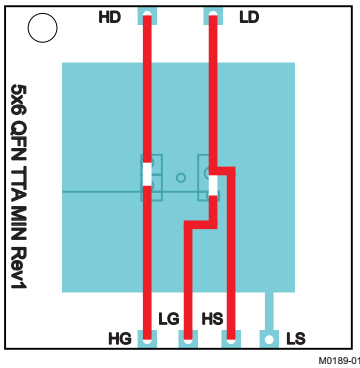
(1) Device mounted on FR4 material with 1-in^2 (6.45-cm^2) Cu.
(2) $R_{\theta JC}$ is determined with the device mounted on a 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu pad on a 1.5-in × 1.5-in (3.81-cm × 3.81-cm), 0.06-in (1.52-mm) thick FR4 board. $R_{\theta JC}$ is specified by design while $R_{\theta JA}$ is determined by the user's board design.

5.5 Electrical Characteristics

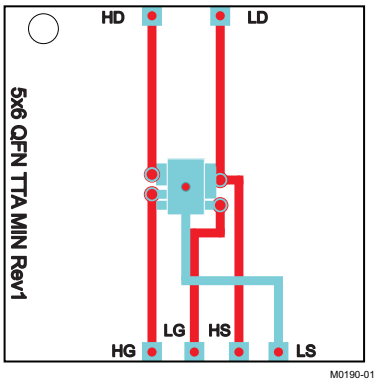
T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	Q1 Control FET			Q2 Sync FET			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
STATIC CHARACTERISTICS									
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_{DS} = 250 µA	30			30			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = 24 V			1			1	µA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = +10 / –8			100			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_{DS} = 250 µA	1.0		2.1	0.75		1.15	V
$Z_{DS(on)}$ (1)	Effective AC on-impedance	V_{IN} = 12 V, V_{GS} = 5 V, V_{OUT} = 1.3 V, I_{OUT} = 20 A, f_{SW} = 500 kHz, L_{OUT} = 0.3 µH,		7.4			1.6		mΩ
g_{fs}	Transconductance	V_{DS} = 15 V, I_{DS} = 20 A		75			142		S
DYNAMIC CHARACTERISTICS									
C_{ISS}	Input capacitance	V_{GS} = 0 V, V_{DS} = 15 V, f = 1 MHz		966	1255		2410	3133	pF
C_{OSS}	Output capacitance			382	497		1130	1469	pF
C_{RSS}	Reverse transfer capacitance			19	25		45	59	pF
R_G	Series gate resistance			0.9	1.8		1	2	Ω
Q_g	Gate charge total (4.5 V)	V_{DS} = 15 V, I_{DS} = 20 A		5.9	7.7		17	22	nC
Q_{gd}	Gate charge gate-to-drain			1.1			3.1		nC
Q_{gs}	Gate charge gate-to-source			2.1			3.7		nC
$Q_{g(th)}$	Gate charge at Vth			1.1			2		nC
Q_{OSS}	Output charge	V_{DS} = 9.8 V, V_{GS} = 0 V		6.5			23		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = 15 V, V_{GS} = 4.5 V, I_{DS} = 20 A, R_G = 2 Ω		6.1			7.7		ns
t_r	Rise time			16			10		ns
$t_{d(off)}$	Turnoff delay time			10			31		ns
t_f	Fall time			2.1			4.2		ns
DIODE CHARACTERISTICS									
V_{SD}	Diode forward voltage	I_{DS} = 20 A, V_{GS} = 0 V		0.86	1		0.78	1	V
Q_{rr}	Reverse recovery charge	V_{dd} = 9.8 V, I_F = 20 A, di/dt = 300 A/µs		8.6			23		nC
t_{rr}	Reverse recovery time			16			24		ns

(1) Equivalent system performance based on application testing. See *Application and Implementation* details.



Max $R_{\theta JA}$ = 62°C/W when mounted on 1 in^2 (6.45 cm^2) of 2-oz (0.071-mm) thick Cu.



Max $R_{\theta JA}$ = 119°C/W when mounted on minimum pad area of 2-oz (0.071-mm) thick Cu.

5.6 Typical Power Block Device Characteristics

T_J = 125°C, unless stated otherwise

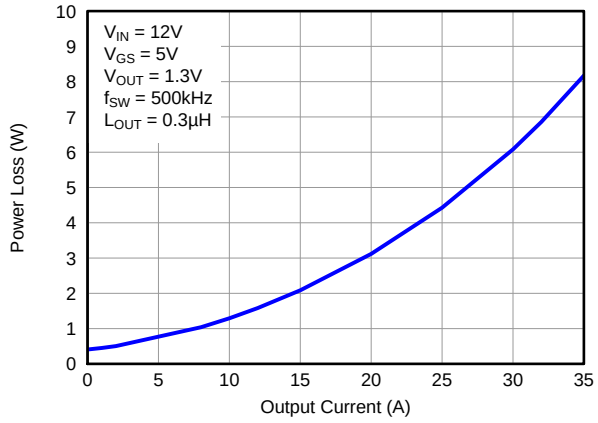


Figure 1. Power Loss vs Output Current

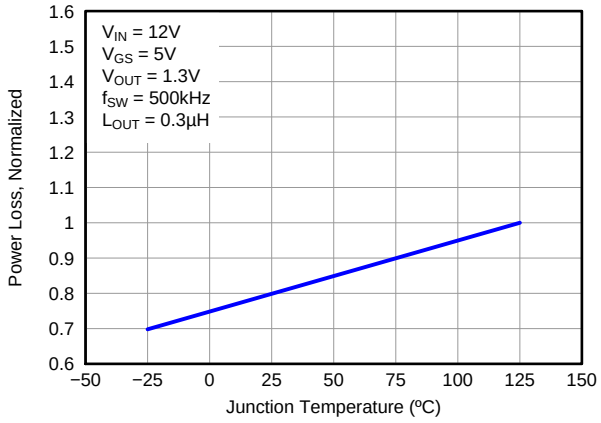


Figure 2. Normalized Power Loss vs Temperature

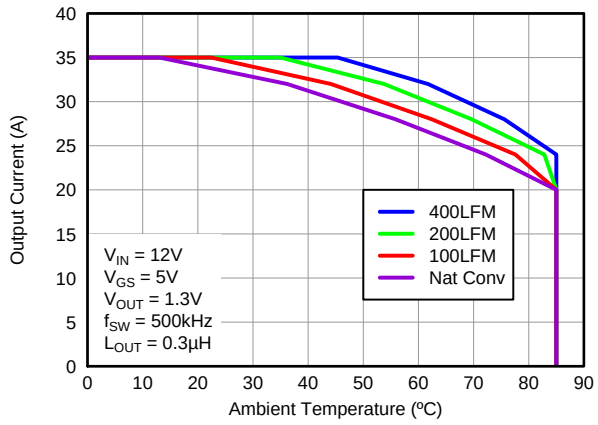


Figure 3. Safe Operating Area – PCB Vertical Mount(1)

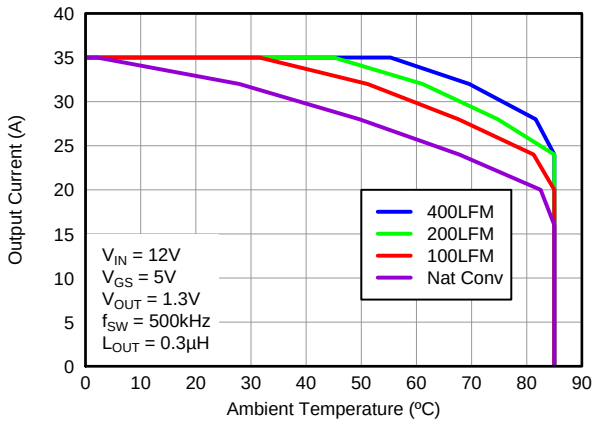


Figure 4. Safe Operating Area – PCB Horizontal Mount(1)

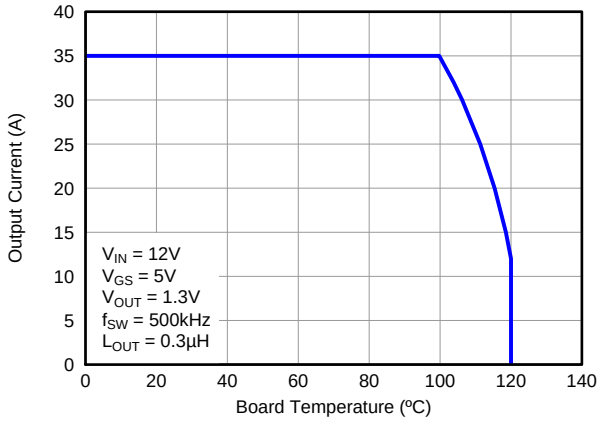


Figure 5. Typical Safe Operating Area(1)

(1) The typical power block system characteristic curves are based on measurements made on a PCB design with dimensions of 4 in (W) × 3.5 in (L) × 0.062 in (H) and 6 copper layers of 1-oz copper thickness. See *Application and Implementation* for detailed explanation.

Typical Power Block Device Characteristics (continued)

T_J = 125°C, unless stated otherwise

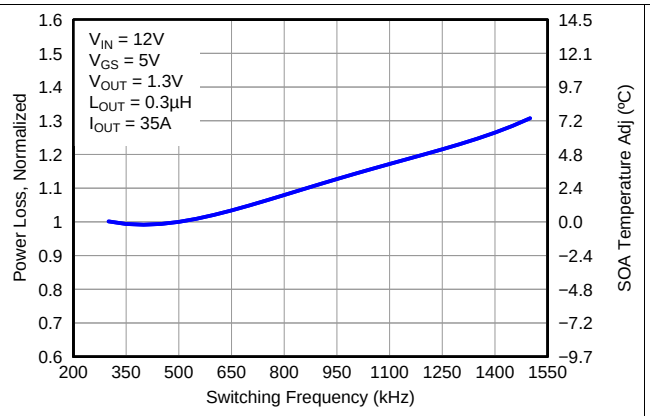


Figure 6. Normalized Power Loss vs Switching Frequency

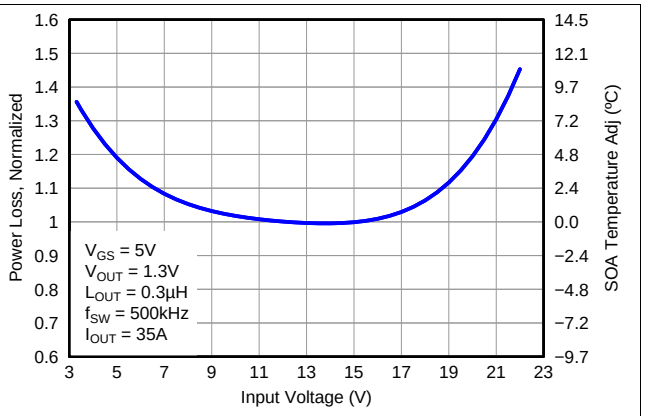


Figure 7. Normalized Power Loss vs Input Voltage

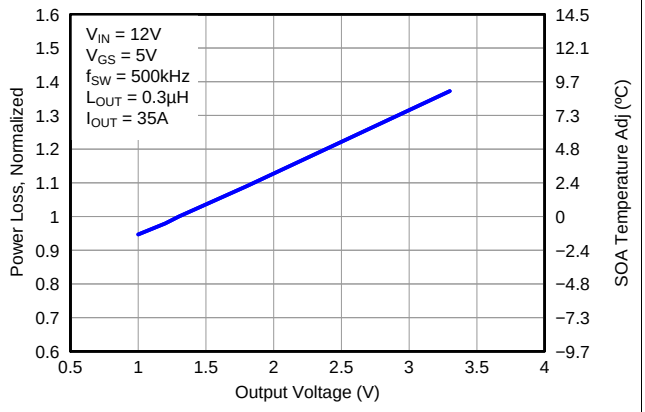


Figure 8. Normalized Power Loss vs Output Voltage

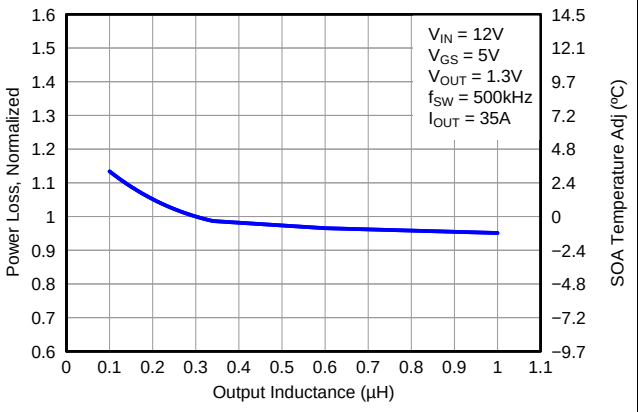


Figure 9. Normalized Power Loss vs Output Inductance

5.7 Typical Power Block MOSFET Characteristics

T_A = 25°C, unless stated otherwise

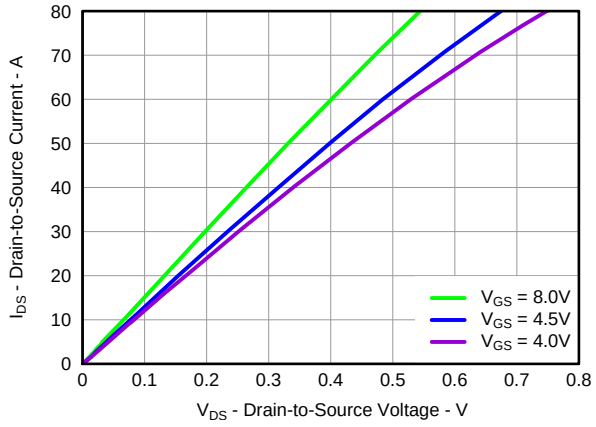


Figure 10. Control MOSFET Saturation

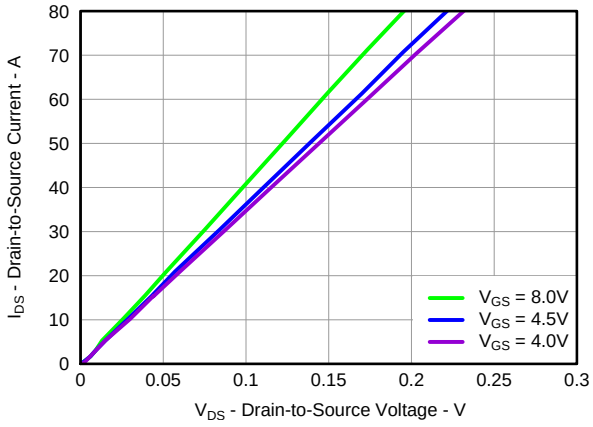


Figure 11. Sync MOSFET Saturation

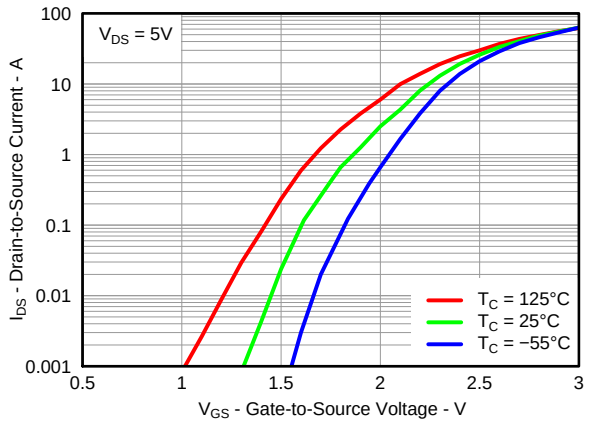


Figure 12. Control MOSFET Transfer

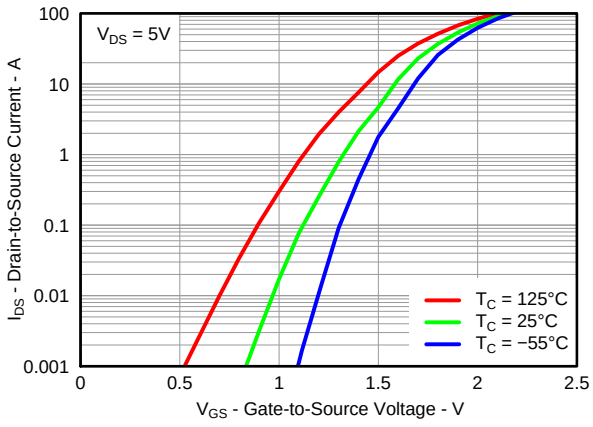


Figure 13. Sync MOSFET Transfer

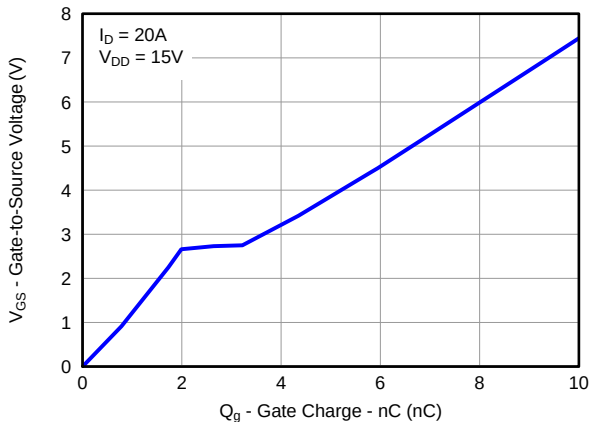


Figure 14. Control MOSFET Gate Charge

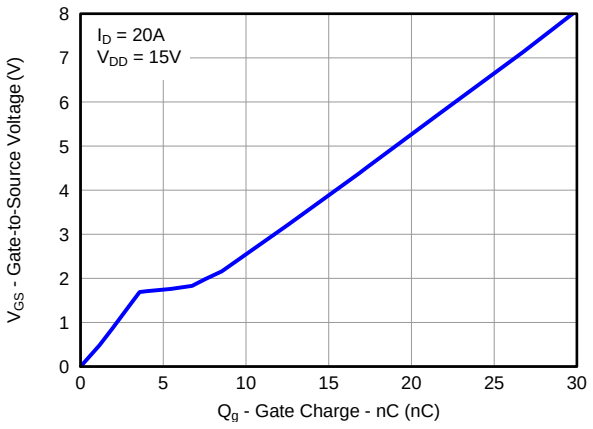


Figure 15. Sync MOSFET Gate Charge

Typical Power Block MOSFET Characteristics (continued)

T_A = 25°C, unless stated otherwise

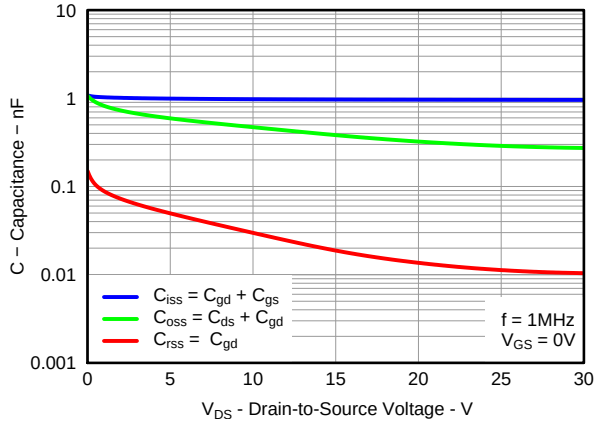


Figure 16. Control MOSFET Capacitance

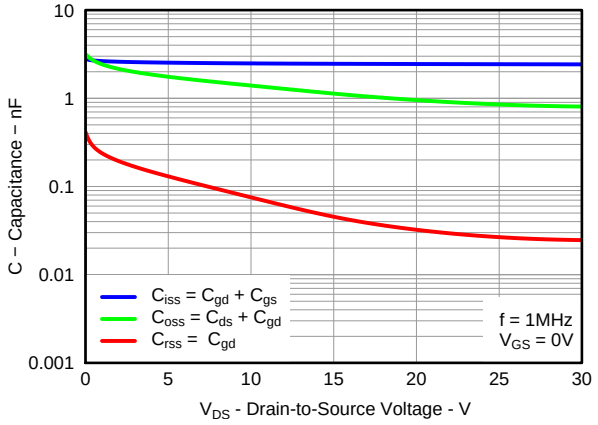


Figure 17. Sync MOSFET Capacitance

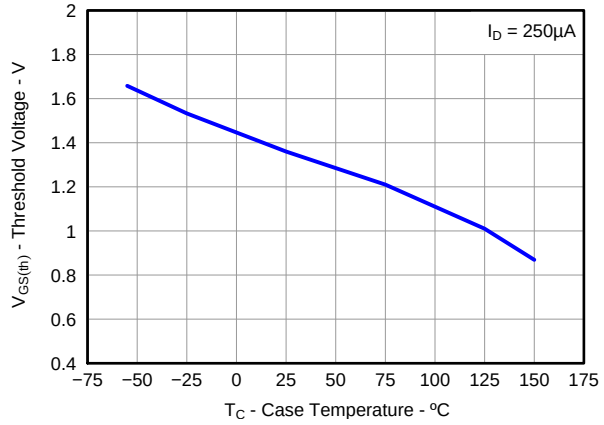


Figure 18. Control MOSFET $V_{GS(th)}$

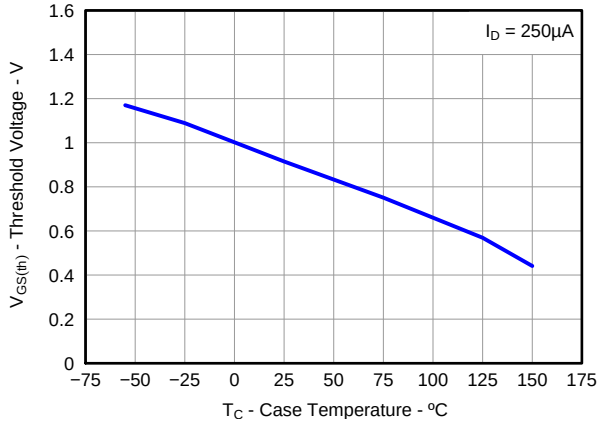


Figure 19. Sync MOSFET $V_{GS(th)}$

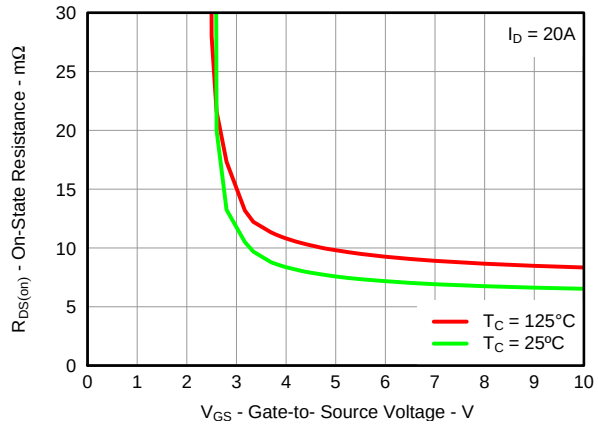


Figure 20. Control MOSFET $R_{DS(on)}$ vs V_{GS}

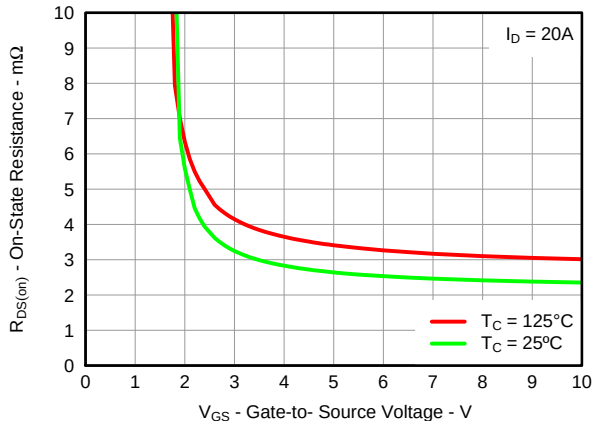


Figure 21. Sync MOSFET $R_{DS(on)}$ vs V_{GS}

Typical Power Block MOSFET Characteristics (continued)

T_A = 25°C, unless stated otherwise

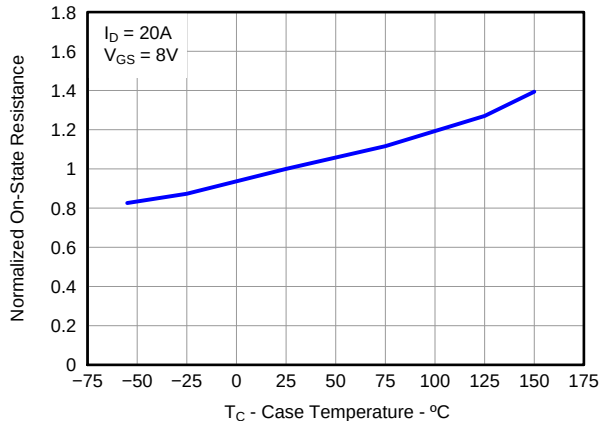


Figure 22. Control MOSFET Normalized $R_{DS(on)}$

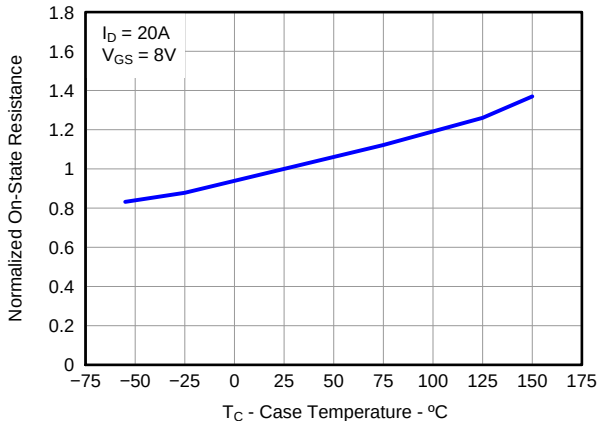


Figure 23. Sync MOSFET Normalized $R_{DS(on)}$

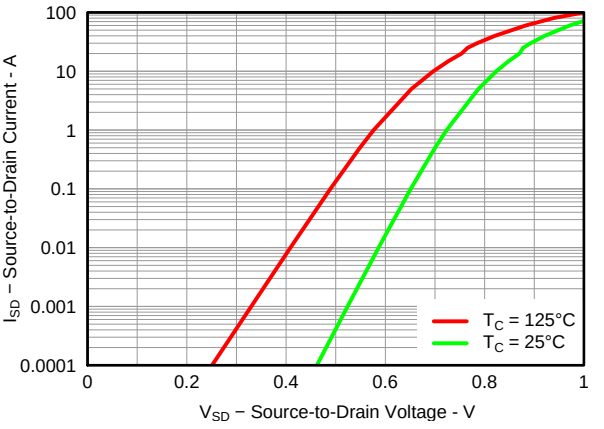


Figure 24. Control MOSFET Body Diode

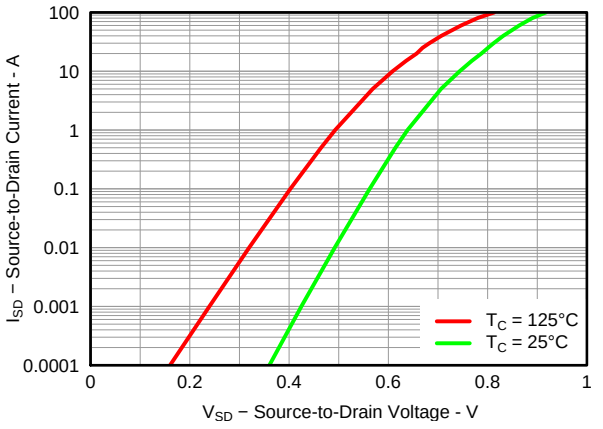


Figure 25. Sync MOSFET Body Diode

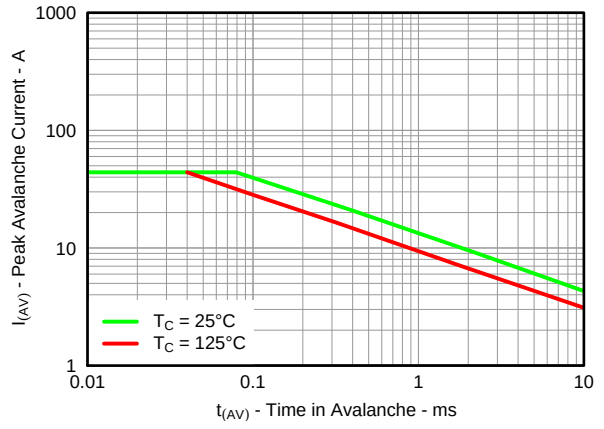


Figure 26. Control MOSFET Unclamped Inductive Switching

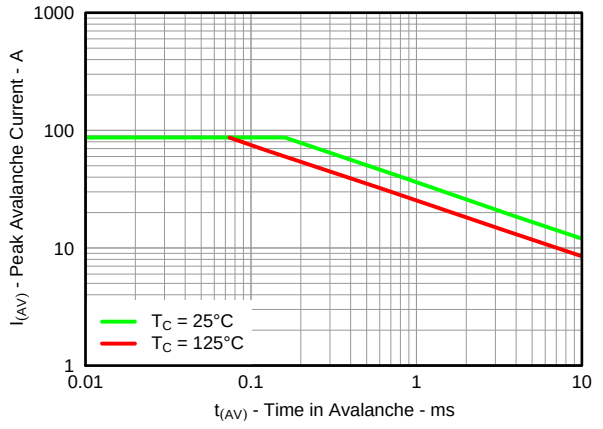


Figure 27. Sync MOSFET Unclamped Inductive Switching

6 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

6.1 Application Information

6.1.1 Equivalent System Performance

Many of today's high-performance computing systems require low-power consumption in an effort to reduce system operating temperatures and improve overall system efficiency. This has created a major emphasis on improving the conversion efficiency of today's synchronous buck topology. In particular, there has been an emphasis in improving the performance of the critical power semiconductor in the power stage of this application (see Figure 28). As such, optimization of the power semiconductors in these applications, needs to go beyond simply reducing $R_{DS(ON)}$.

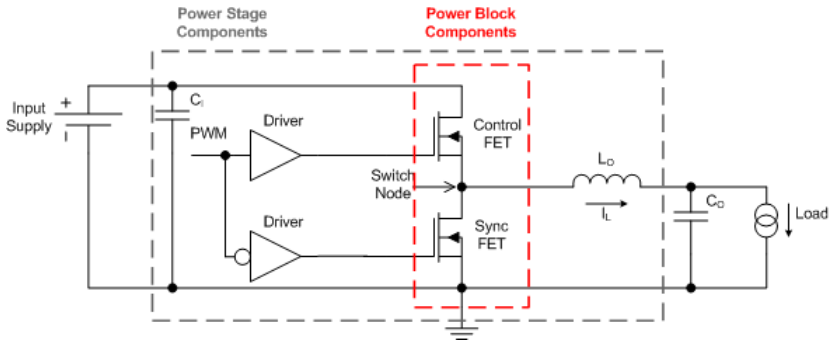


Figure 28. Equivalent System Schematic

The CSD87351Q5D is part of TI's power block product family which is a highly optimized product for use in a synchronous buck topology requiring high current, high efficiency, and high frequency. It incorporates TI's latest generation silicon which has been optimized for switching performance, as well as minimizing losses associated with Q_{GD}, Q_{GS}, and Q_{RR}. Furthermore, TI's patented packaging technology has minimized losses by nearly eliminating parasitic elements between the control FET and sync FET connections (see Figure 29). A key challenge solved by TI's patented packaging technology is the system level impact of Common Source Inductance (CSI). CSI greatly impedes the switching characteristics of any MOSFET which in turn increases switching losses and reduces system efficiency. As a result, the effects of CSI need to be considered during the MOSFET selection process. In addition, standard MOSFET switching loss equations used to predict system efficiency need to be modified in order to account for the effects of CSI. Further details behind the effects of CSI and modification of switching loss equations are outlined in *Power Loss Calculation With Common Source Inductance Consideration for Synchronous Buck Converters* (SLPA009).

Application Information (continued)

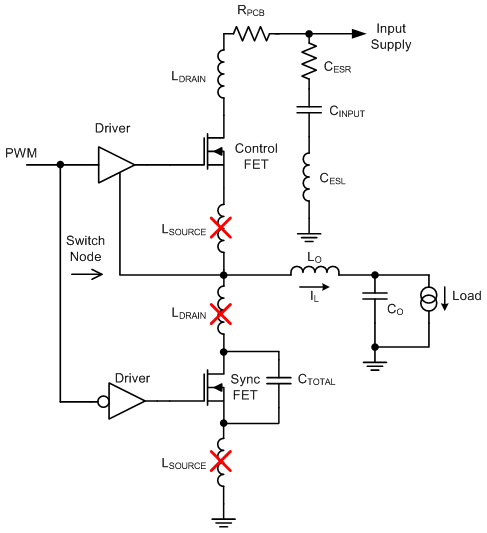


Figure 29. Elimination of Parasitic Inductances

The combination of TI's latest generation silicon and optimized packaging technology has created a bench marking solution that outperforms industry standard MOSFET chipsets of similar $R_{DS(ON)}$ and MOSFET chipsets with lower $R_{DS(ON)}$. Figure 30 and Figure 31 compare the efficiency and power loss performance of the CSD87351Q5D versus industry standard MOSFET chipsets commonly used in this type of application. This comparison purely focuses on the efficiency and generated loss of the power semiconductors only. The performance of CSD87351Q5D clearly highlights the importance of considering the effective AC on-impedance ($Z_{DS(ON)}$) during the MOSFET selection process of any new design. Simply normalizing to traditional MOSFET $R_{DS(ON)}$ specifications is not an indicator of the actual in-circuit performance when using TI's power block technology.

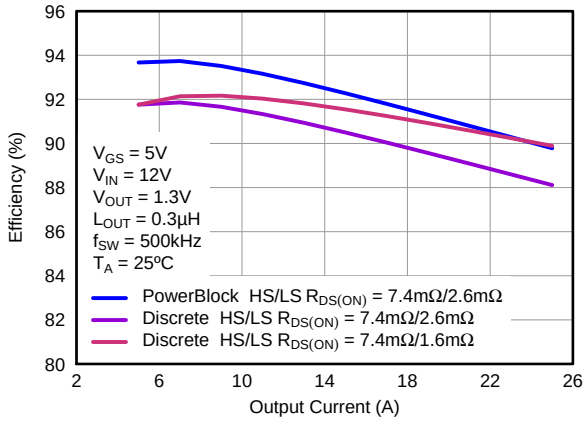


Figure 30. Efficiency

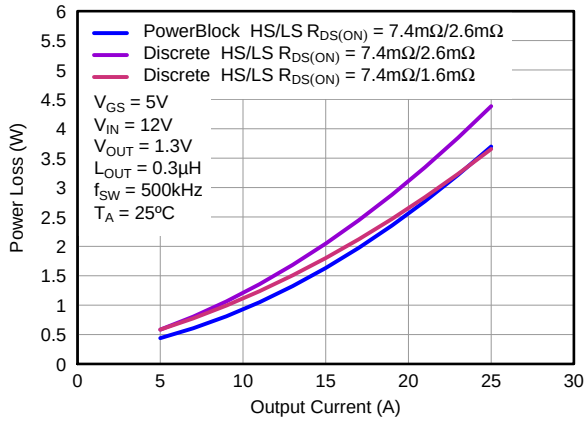


Figure 31. Power Loss

Application Information (continued)

The chart below compares the traditional DC measured $R_{DS(ON)}$ of CSD87351Q5D versus its $Z_{DS(ON)}$. This comparison takes into account the improved efficiency associated with TI's patented packaging technology. As such, when comparing TI's power block products to individually packaged discrete MOSFETs or dual MOSFETs in a standard package, the in-circuit switching performance of the solution must be considered. In this example, individually packaged discrete MOSFETs or dual MOSFETs in a standard package would need to have DC measured $R_{DS(ON)}$ values that are equivalent to CSD87351Q5D's $Z_{DS(ON)}$ value in order to have the same efficiency performance at full load. Mid to light-load efficiency will still be lower with individually packaged discrete MOSFETs or dual MOSFETs in a standard package.

Table 1. Comparison of $R_{DS(ON)}$ vs $Z_{DS(ON)}$

PARAMETER	HS		LS	
	TYP	MAX	TYP	MAX
Effective AC on-impedance $Z_{DS(ON)}$ (V_{GS} = 5 V)	7.4	–	1.6	–
DC measured $R_{DS(ON)}$ (V_{GS} = 4.5 V)	7.4	8.8	2.6	3.1

The CSD87351Q5D NexFET™ power block is an optimized design for synchronous buck applications using 5-V gate drive. The control FET and sync FET silicon are parametrically tuned to yield the lowest power loss and highest system efficiency. As a result, a new rating method is needed which is tailored towards a more systems-centric environment. System-level performance curves such as power loss, Safe Operating Area (SOA), and normalized graphs allow engineers to predict the product performance in the actual application.

6.1.2 Power Loss Curves

MOSFET centric parameters such as $R_{DS(ON)}$ and Q_{gd} are needed to estimate the loss generated by the devices. In an effort to simplify the design process for engineers, Texas Instruments has provided measured power loss performance curves. Figure 1 plots the power loss of the CSD87351Q5D as a function of load current. This curve is measured by configuring and running the CSD87351Q5D as it would be in the final application (see Figure 32).The measured power loss is the CSD87351Q5D loss and consists of both input conversion loss and gate drive loss. Equation 1 is used to generate the power loss curve.

$$\text{Power loss} = (V_{IN} \times I_{IN}) + (V_{DD} \times I_{DD}) - (V_{SW\_AVG} \times I_{OUT}) \quad (1)$$

The power loss curve in Figure 1 is measured at the maximum recommended junction temperatures of 125°C under isothermal test conditions.

6.1.3 Safe Operating Area (SOA) Curves

The SOA curves in the CSD87351Q5D data sheet provides guidance on the temperature boundaries within an operating system by incorporating the thermal resistance and system power loss. Figure 3 to Figure 5 outline the temperature and airflow conditions required for a given load current. The area under the curve dictates the safe operating area. All the curves are based on measurements made on a PCB design with dimensions of 4 in (W) × 3.5 in (L) × 0.062 in (T) and 6 copper layers of 1-oz copper thickness.

6.1.4 Normalized Curves

The normalized curves in the CSD87351Q5D data sheet provides guidance on the power loss and SOA adjustments based on their application specific needs. These curves show how the power loss and SOA boundaries will adjust for a given set of systems conditions. The primary Y-axis is the normalized change in power loss and the secondary Y-axis is the change is system temperature required in order to comply with the SOA curve. The change in power loss is a multiplier for the power loss curve and the change in temperature is subtracted from the SOA curve.

6.2 Typical Application

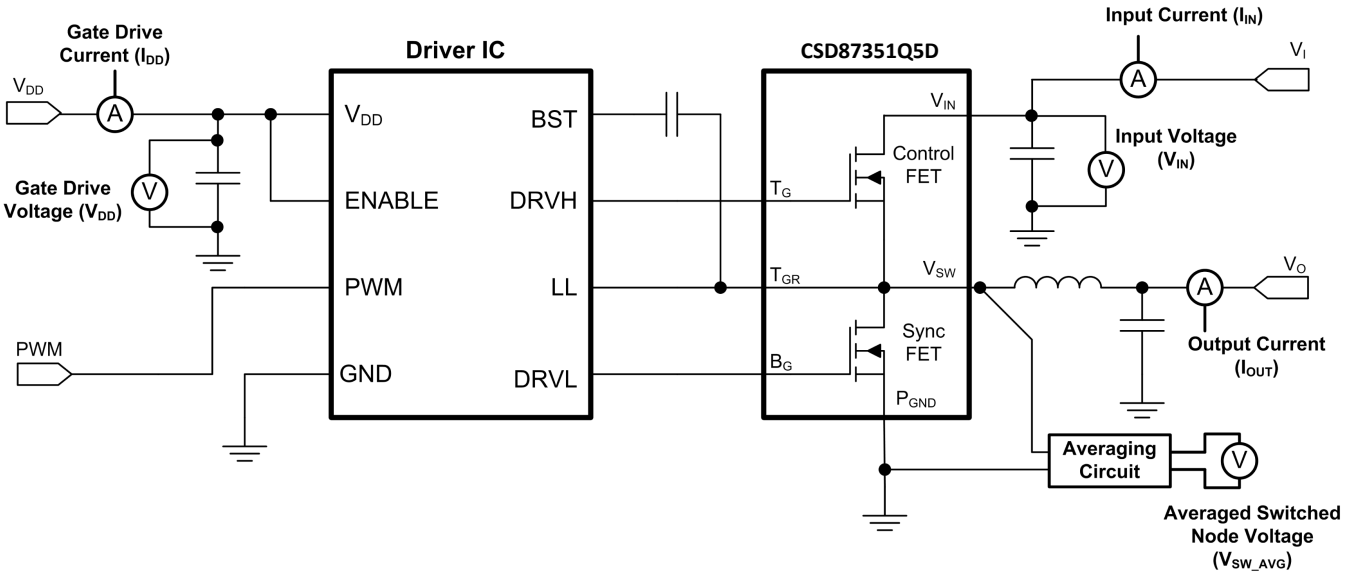


Figure 32. Typical Application

6.2.1 Calculating Power Loss and SOA

The user can estimate product loss and SOA boundaries by arithmetic means (see *Design Example*). Though the power loss and SOA curves in this data sheet are taken for a specific set of test conditions, the following procedure will outline the steps the user should take to predict product performance for any set of system conditions.

6.2.1.1 Design Example

Operating conditions:

- Output current = 25 A
- Input voltage = 7 V
- Output voltage = 1 V
- Switching frequency = 800 kHz
- Inductor = 0.2 µH

6.2.1.2 Calculating Power Loss

- Power loss at 25 A = 3.5 W (Figure 1)
- Normalized power loss for input voltage ≈ 1.07 (Figure 7)
- Normalized power loss for output voltage ≈ 0.95 (Figure 8)
- Normalized power loss for switching frequency ≈ 1.11 (Figure 6)
- Normalized power loss for output inductor ≈ 1.07 (Figure 9)
- **Final calculated power loss = 3.5 W × 1.07 × 0.95 × 1.11 × 1.07 ≈ 4.23 W**

6.2.1.3 Calculating SOA Adjustments

- SOA adjustment for input voltage ≈ 2°C (Figure 7)
- SOA adjustment for output voltage ≈ –1.3°C (Figure 8)
- SOA adjustment for switching frequency ≈ 2.8°C (Figure 6)
- SOA adjustment for output inductor ≈ 1.6°C (Figure 9)
- **Final calculated SOA adjustment = 2 + (–1.3) + 2.8 + 1.6 ≈ 5.1°C**

Typical Application (continued)

In the design example above, the estimated power loss of the CSD87351Q5D would increase to 4.23 W. In addition, the maximum allowable board and/or ambient temperature would have to decrease by 5.1°C. Figure 33 graphically shows how the SOA curve would be adjusted accordingly.

1. Start by drawing a horizontal line from the application current to the SOA curve.
2. Draw a vertical line from the SOA curve intercept down to the board/ambient temperature.
3. Adjust the SOA board/ambient temperature by subtracting the temperature adjustment value.

In the design example, the SOA temperature adjustment yields a reduction in allowable board/ambient temperature of 5.1°C. In the event the adjustment value is a negative number, subtracting the negative number would yield an increase in allowable board/ambient temperature.

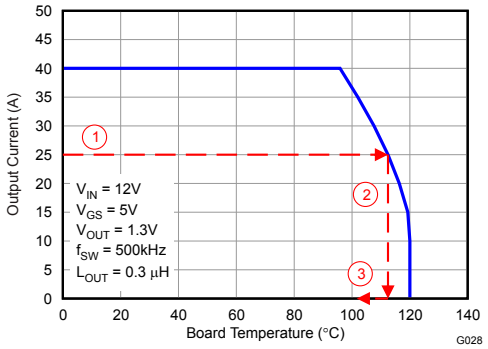


Figure 33. Power Block SOA

7 Layout

7.1 Layout Guidelines

There are two key system-level parameters that can be addressed with a proper PCB design: electrical and thermal performance. Properly optimizing the PCB layout will yield maximum performance in both areas. A brief description on how to address each parameter is provided.

7.1.1 Electrical Performance

The power block has the ability to switch voltages at rates greater than 10 kV/µs. Special care must be then taken with the PCB layout design and placement of the input capacitors, driver IC, and output inductor.

- The placement of the input capacitors relative to the power block's VIN and PGND pins should have the highest priority during the component placement routine. It is critical to minimize these node lengths. As such, ceramic input capacitors need to be placed as close as possible to the VIN and PGND pins (see Figure 34). The example in Figure 34 uses 6, 10-µF ceramic capacitors (TDK part # C3216X5R1C106KT or equivalent). Notice there are ceramic capacitors on both sides of the board with an appropriate amount of vias interconnecting both layers. In terms of priority of placement next to the power block, C5, C7, C19, and C8 should follow in order.
- The driver IC should be placed relatively close to the power block gate pins. T_G and B_G should connect to the outputs of the driver IC. The T_{GR} pin serves as the return path of the high-side gate drive circuitry and should be connected to the phase pin of the IC (sometimes called LX, LL, SW, PH, etc.). The bootstrap capacitor for the driver IC will also connect to this pin.
- The switching node of the output inductor should be placed relatively close to the power block VSW pins. Minimizing the node length between these two components will reduce the PCB conduction losses and actually reduce the switching noise level.
- The switching node of the output inductor should be placed relatively close to the power block VSW pins. Minimizing the node length between these two components will reduce the PCB conduction losses and actually reduce the switching noise level. In the event the switch node waveform exhibits ringing that reaches undesirable levels, the use of a boost resistor or RC snubber can be an effective way to reduce the peak ring level. The recommended boost resistor value will range between 1 Ω to 4.7 Ω depending on the output characteristics of driver IC used in conjunction with the power block. The RC snubber values can range from 0.5 Ω to 2.2 Ω for the R and 330 pF to 2200 pF for the C. Refer to *Snubber Circuits: Theory , Design and Application* (SLUP100) for more details on how to properly tune the RC snubber values. The RC snubber should be placed as close as possible to the Vsw node and PGND see Figure 34. (1)

7.1.2 Thermal Performance

The power block has the ability to utilize the GND planes as the primary thermal path. As such, the use of thermal vias is an effective way to pull away heat from the device and into the system board. Concerns of solder voids and manufacturability problems can be addressed by the use of three basic tactics to minimize the amount of solder attach that will wick down the via barrel:

- Intentionally space out the vias from each other to avoid a cluster of holes in a given area.
- Use the smallest drill size allowed in your design. The example in Figure 34 uses vias with a 10-mil drill hole and a 16-mil capture pad.
- Tent the opposite side of the via with solder-mask.

In the end, the number and drill size of the thermal vias should align with the end user's PCB design rules and manufacturing capabilities.

(1) Keong W. Kam, David Pommerenke, "EMI Analysis Methods for Synchronous Buck Converter EMI Root Cause Analysis", University of Missouri – Rolla

7.2 Layout Example

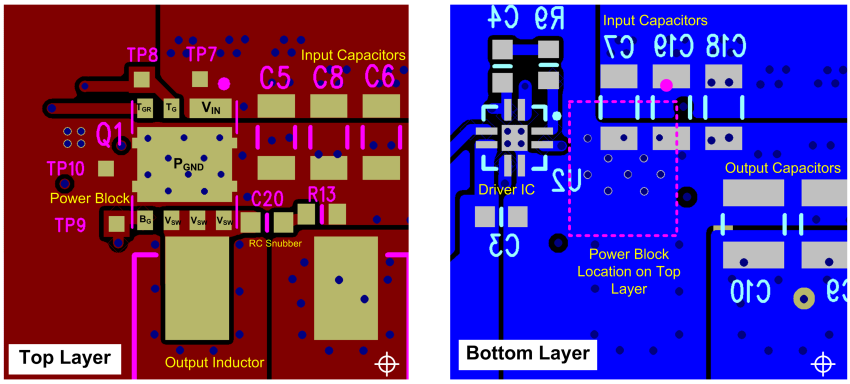


Figure 34. Recommended PCB Layout (Top Down View)

8 器件和文档支持

8.1 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

8.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

8.3 商标

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8.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

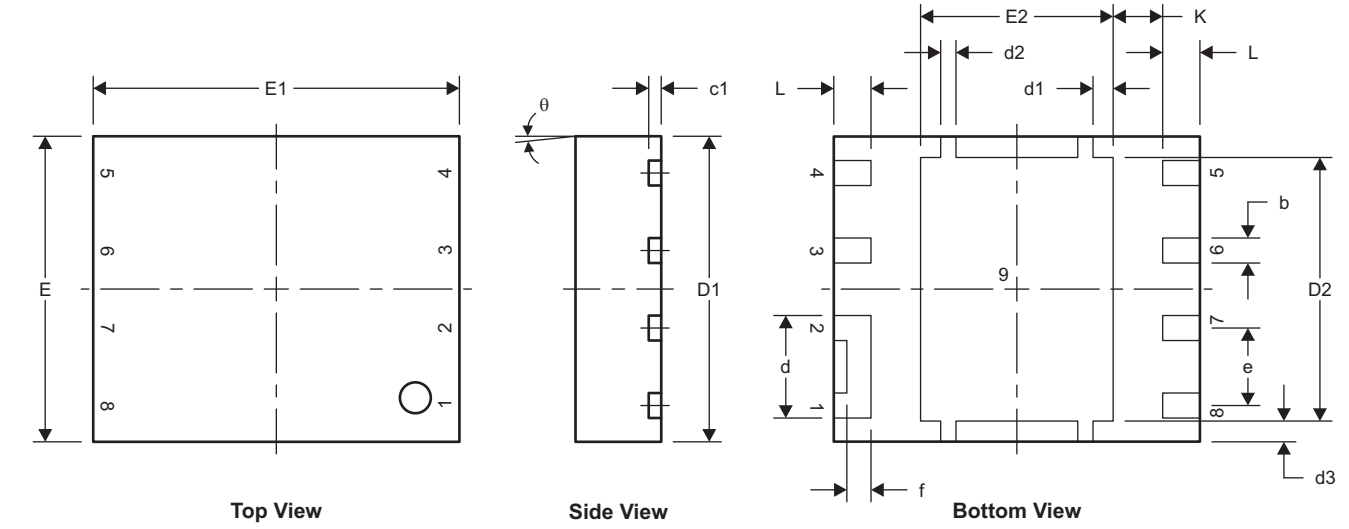
8.5 Glossary

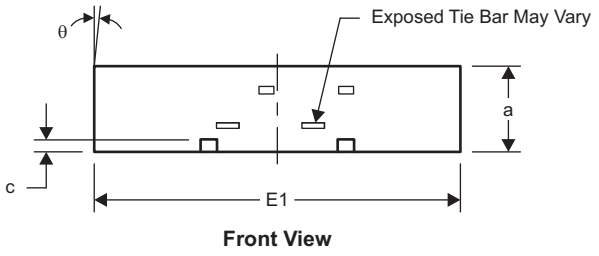
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

9 机械、封装和可订购信息

9.1 Q5D 封装尺寸



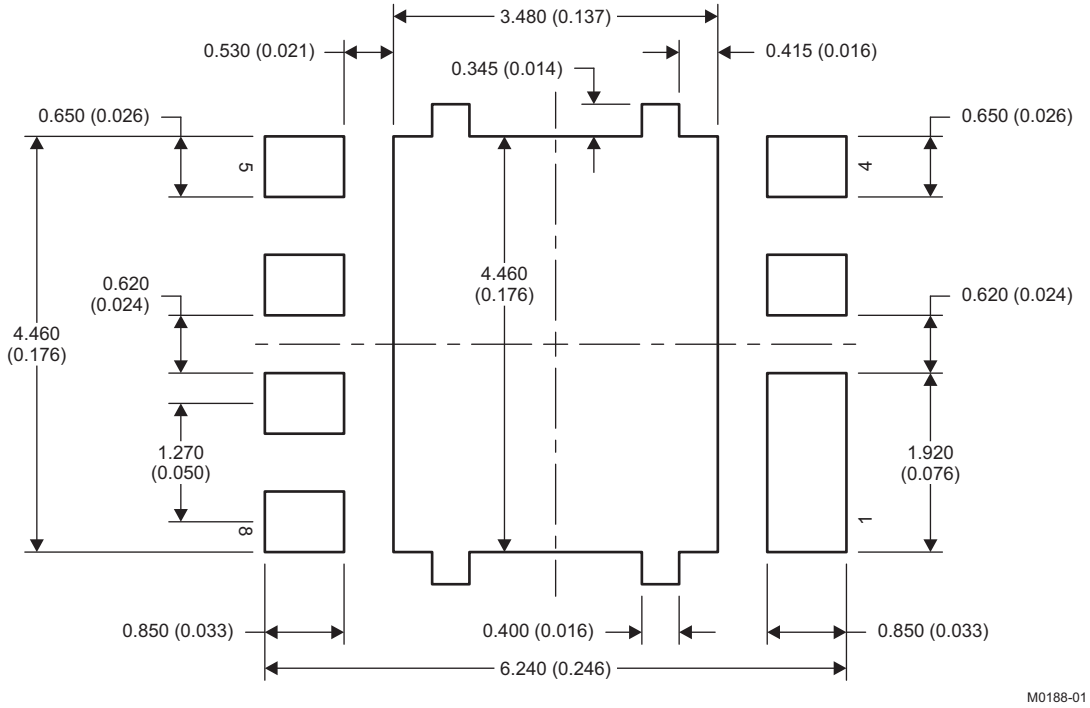


Pinout	
Position	Designation
Pin 1	V_{IN}
Pin 2	V_{IN}
Pin 3	T_G
Pin 4	T_{GR}
Pin 5	B_G
Pin 6	V_{SW}
Pin 7	V_{SW}
Pin 8	V_{SW}
Pin 9	P_{GND}

M0187-01

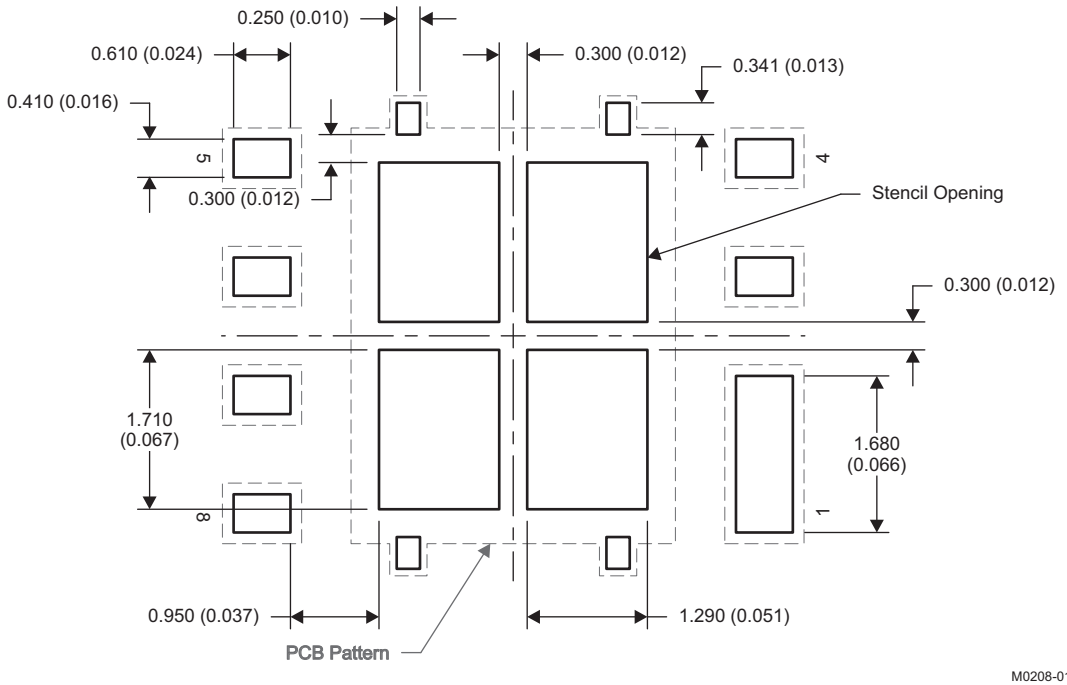
DIM	毫米		英寸	
	最小值	最大值	最小值	最大值
a	1.400	1.500	0.055	0.059
b	0.360	0.460	0.014	0.018
c	0.150	0.250	0.006	0.010
c1	0.150	0.250	0.006	0.010
d	1.630	1.730	0.064	0.068
d1	0.280	0.380	0.011	0.015
d2	0.200	0.300	0.008	0.012
d3	0.291	0.391	0.012	0.015
D1	4.900	5.100	0.193	0.201
D2	4.269	4.369	0.168	0.172
E	4.900	5.100	0.193	0.201
E1	5.900	6.100	0.232	0.240
E2	3.106	3.206	0.122	0.126
e	1.270（典型值）		0.050	
f	0.396	0.496	0.016	0.020
L	0.510	0.710	0.020	0.028
θ	0.000	—	—	—
K	0.812		0.032	

9.2 焊盘布局建议



NOTE: 尺寸单位为 mm（英寸）。

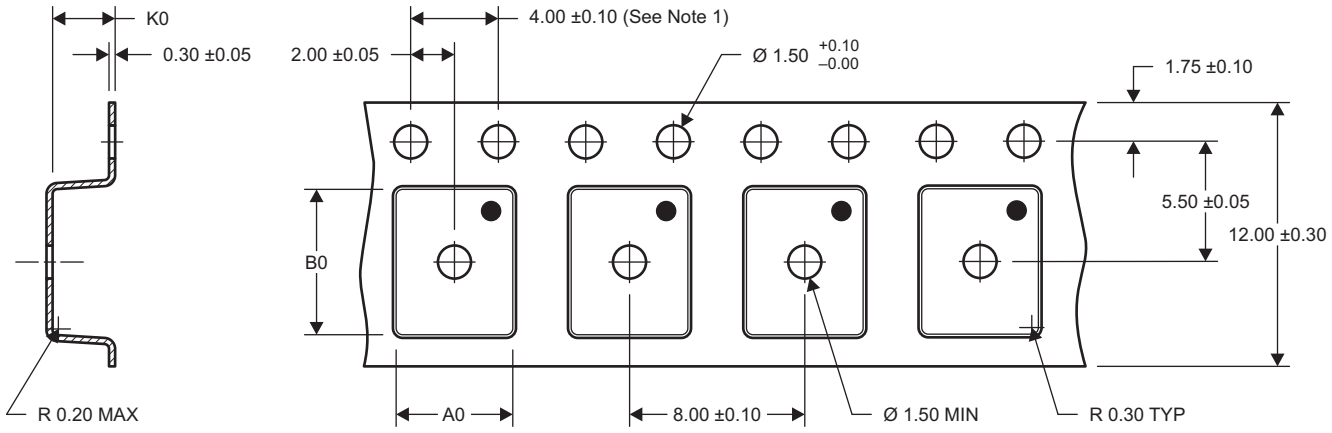
9.3 模板建议



NOTE: 尺寸单位为 mm（英寸）。

有关针对 PCB 设计的建议电路布局布线，请参见《通过 PCB 布局布线技巧来减少振铃》（文献编号：SLPA005）。

9.4 Q5D 卷带信息



NOTES: 1. 10 链轮孔距累积容差为 ±0.2

2. 每 100mm 长度的外倾角不能超过 1mm，在 250mm 长度上不累积。
3. 材料：黑色抗静电聚苯乙烯。
4. 全部尺寸单位为 mm，除非另外注明。
5. 厚度：0.3 ± 0.05mm。
6. 符合 MSL1 260°C（红外和对流）PbF 回流焊要求。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD87351Q5D	ACTIVE	LSON-CLIP	DQY	8	2500	Pb-Free (RoHS Exempt)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-55 to 150	87351D	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

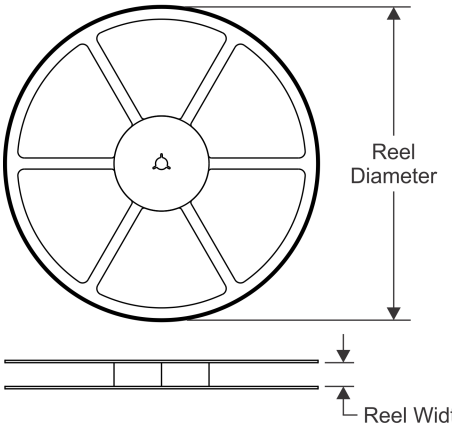
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

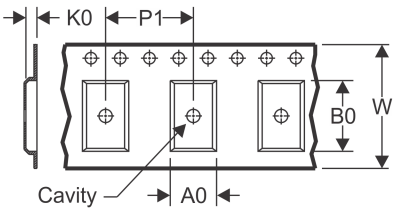
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

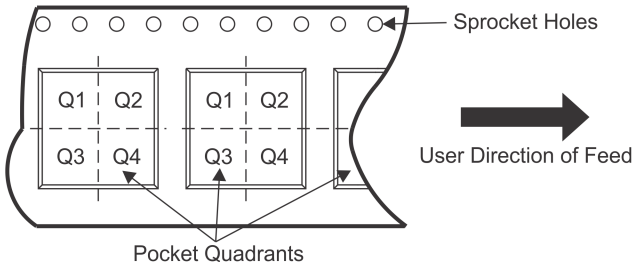


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

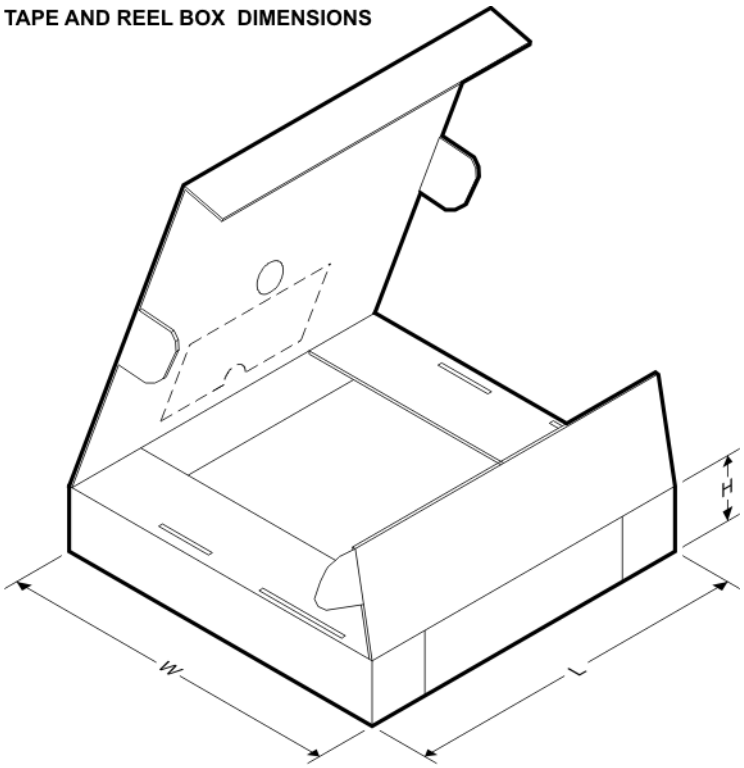
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD87351Q5D	LSON-CLIP	DQY	8	2500	330.0	15.4	5.3	6.3	1.2	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD87351Q5D	LSON-CLIP	DQY	8	2500	335.0	335.0	32.0

重要声明

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邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122