

TC74VHC157F, TC74VHC157FN, TC74VHC157FT

QUAD 2 - CHANNEL MULTIPLEXER

The TC74VHC157 is an advanced high speed CMOS QUAD 2 - CHANNEL MULTIPLEXER fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

It consists of four 2 - input digital multiplexers with common select and strobe inputs.

When the STROBE input is held "H" level, selection of data is inhibited and all the outputs become "L" level.

The SELECT decoding determines whether the A or B inputs get routed to their corresponding Y outputs.

An Input protection circuit ensures that 0 to 5.5V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and on two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

FEATURES :

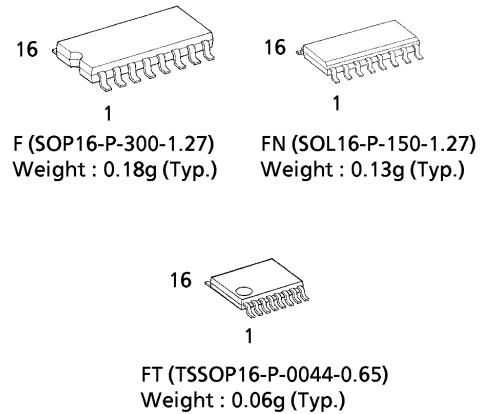
- High Speed..... $t_{pd} = 4.1ns(typ.)$ at $V_{CC} = 5V$
- Low Power Dissipation..... $I_{CC} = 4\mu A(Max.)$ at $T_a = 25^{\circ}C$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC} (Min.)$
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays..... $t_{pLH} \approx t_{pHL}$
- Wide Operating Voltage Range..... $V_{CC} (opr) = 2V \sim 5.5V$
- Low Noise $V_{OLP} = 0.8V (Max.)$
- Pin and Function Compatible with 74ALS157

TRUTH TABLE

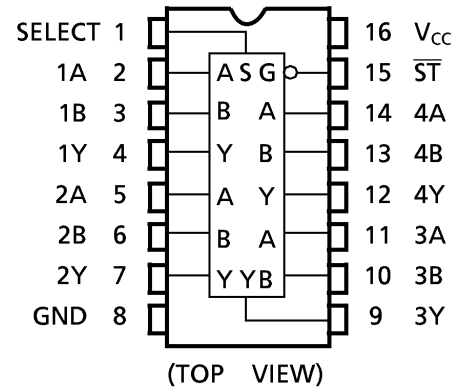
INPUTS				OUTPUT
ST	SELECT	A	B	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

X : Don't Care

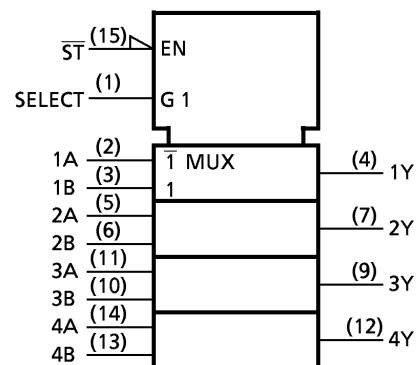
(Note) The JEDEC SOP (FN) is not available in Japan.



PIN ASSIGNMENT



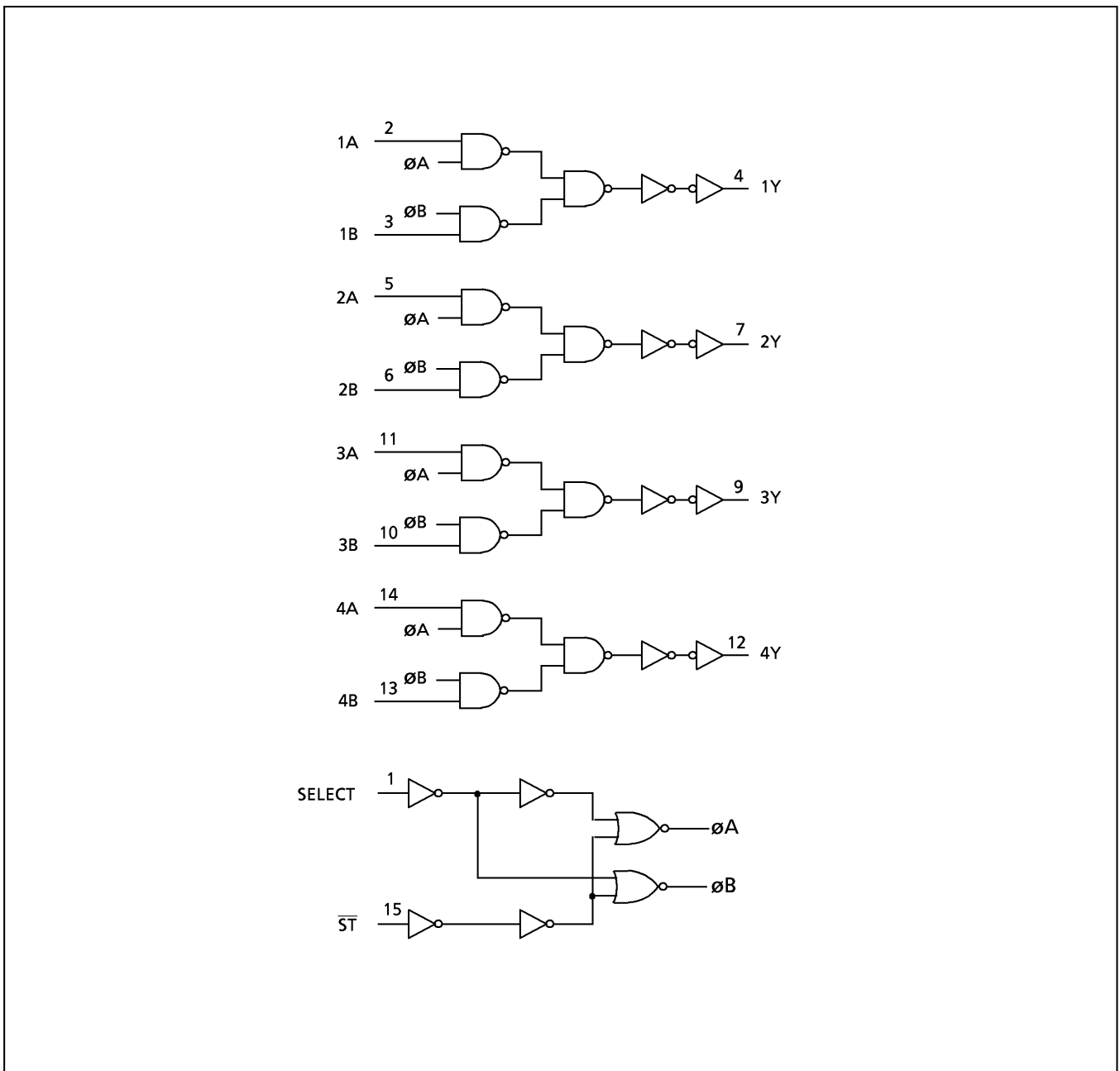
IEC LOGIC SYMBOL



980910EBA2

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SYSTEM DIAGRAM



980910EBA2'

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ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5~7.0	V
DC Input Voltage	V_{IN}	-0.5~7.0	V
DC Output Voltage	V_{OUT}	-0.5~ $V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	-20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC} /Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	-65~150	$^{\circ}C$

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~ V_{CC}	V
Operating Temperature	T_{opr}	-40~85	$^{\circ}C$
Input Rise and Fall Time	dt / dv	0~100 ($V_{CC} = 3.3 \pm 0.3V$) 0~20 ($V_{CC} = 5 \pm 0.5V$)	ns / V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	$T_a = 25^{\circ}C$			$T_a = -40 \sim 85^{\circ}C$		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.		
High - Level Input Voltage	V_{IH}		2.0 3.0~5.5	1.50 $V_{CC} \times 0.7$	- -	- -	1.50 $V_{CC} \times 0.7$	- -	V	
Low - Level Input Voltage	V_{IL}		2.0 3.0~5.5	- -	- -	0.50 $V_{CC} \times 0.3$	- -	0.50 $V_{CC} \times 0.3$	V	
High - Level Output Voltage	V_{OH}	$V_{IN} =$ V_{IH} or V_{IL}	$I_{OH} = -50\mu A$	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	- - -	1.9 2.9 4.4	- - -	V
			$I_{OH} = -4mA$	3.0	2.58	-	-	2.48	-	
			$I_{OH} = -8mA$	4.5	3.94	-	-	3.80	-	
Low - Level Output Voltage	V_{OL}	$V_{IN} =$ V_{IH} or V_{IL}	$I_{OL} = 50\mu A$	2.0 3.0 4.5	- - -	0.0 0.0 0.0	0.1 0.1 0.1	- - -	0.1 0.1 0.1	V
			$I_{OL} = 4mA$	3.0	-	-	0.36	-	0.44	
			$I_{OL} = 8mA$	4.5	-	-	0.36	-	0.44	
Input Leakage Current	I_{IN}	$V_{IN} = 5.5V$ or GND	0~5.5	-	-	± 0.1	-	± 1.0	μA	
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND	5.5	-	-	4.0	-	40.0		

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = -40~85°C		UNIT
		V _{CC} (V)	CL (pF)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (A, B - Y)	t _{pLH} t _{pHL}	3.3 ± 0.3	15	—	6.2	9.7	1.0	11.5	ns
			50	—	8.7	13.2	1.0	15.0	
		5.0 ± 0.5	15	—	4.1	6.4	1.0	7.5	
			50	—	5.6	8.4	1.0	9.5	
Propagation Delay Time (SELECT - Y)	t _{pLH} t _{pHL}	3.3 ± 0.3	15	—	8.4	13.2	1.0	15.5	
			50	—	10.9	16.7	1.0	19.0	
		5.0 ± 0.5	15	—	5.3	8.1	1.0	9.5	
			50	—	6.8	10.1	1.0	11.5	
Propagation Delay Time (\overline{ST} - Y)	t _{pLH} t _{pHL}	3.3 ± 0.3	15	—	8.7	13.6	1.0	16.0	
			50	—	11.2	17.1	1.0	19.5	
		5.0 ± 0.5	15	—	5.6	8.6	1.0	10.0	
			50	—	7.1	10.6	1.0	12.0	
Input Capacitance	C _{I N}			—	4	10	—	10	pF
Power Dissipation Capacitance	C _{PD}	(Note 1)		—	20	—	—	—	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

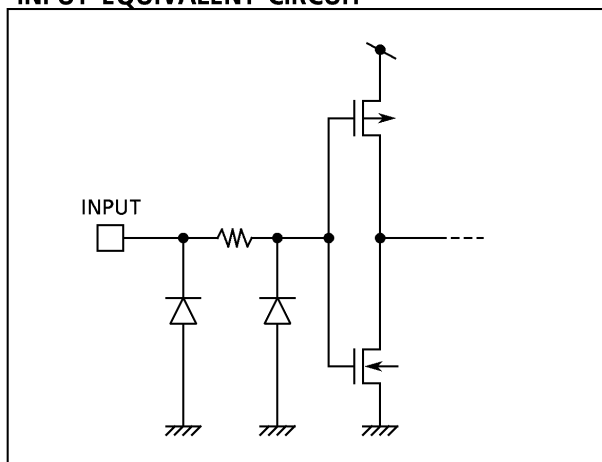
Average operating current can be obtained by the equation :

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 4 \text{ (per bit)}$$

NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$)

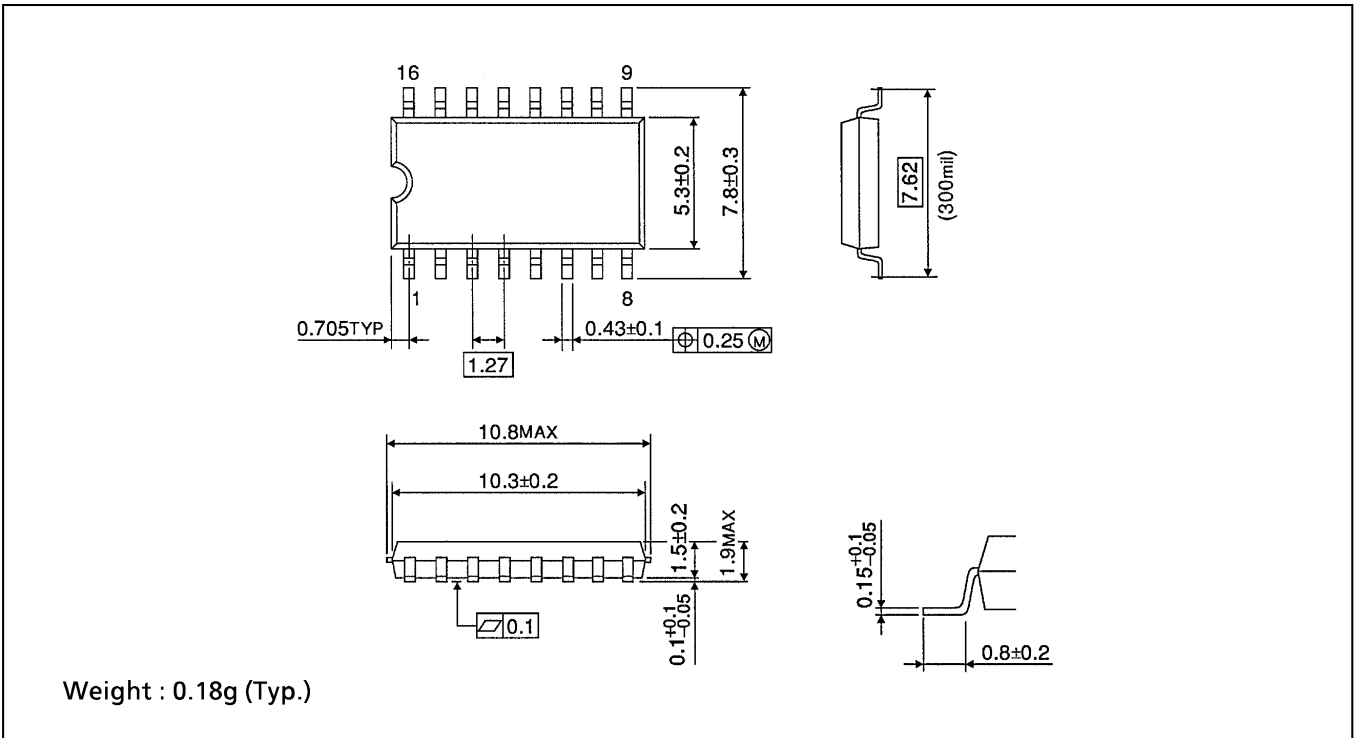
PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			UNIT
			V _{CC} (V)	TYP.	LIMIT	
Quiet Output Maximum Dynamic V _{OL}	V _{OLP}	C _L = 50pF	5.0	0.3	0.8	V
Quiet Output Minimum Dynamic V _{OL}	V _{OLV}	C _L = 50pF	5.0	-0.3	-0.8	V
Minimum High Level Dynamic Input Voltage	V _{IHD}	C _L = 50pF	5.0	—	3.5	V
Maximum Low Level Dynamic Input Voltage	V _{ILD}	C _L = 50pF	5.0	—	1.5	V

INPUT EQUIVALENT CIRCUIT



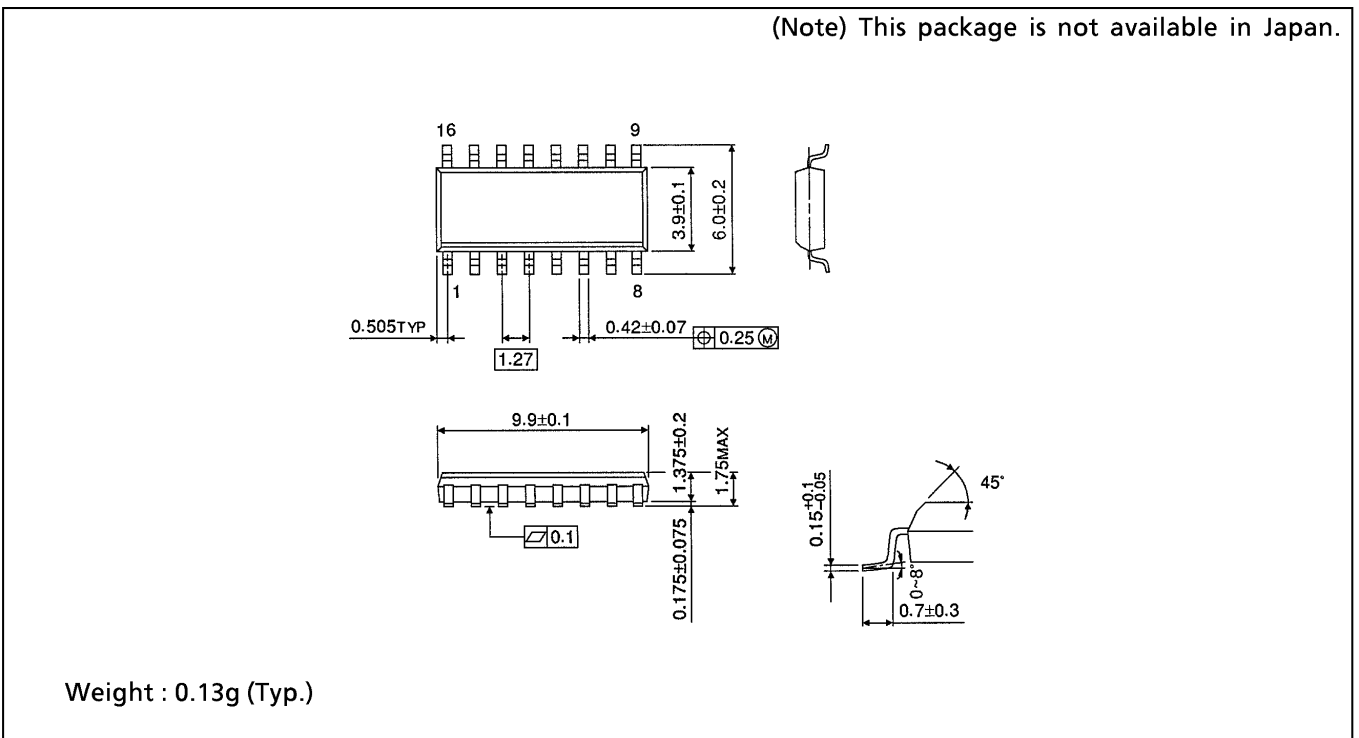
SOP 16PIN (200mil BODY) PACKAGE DIMENSIONS (SOP16-P-300-1.27)

Unit in mm



SOP 16PIN (150mil BODY) PACKAGE DIMENSIONS (SOP16-P-150-1.27)

Unit in mm



TSSOP 16PIN PACKAGE DIMENSIONS (TSSOP16-P-0044-0.65)

Unit in mm

