

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

## TC74HCT574AP, TC74HCT574AF

### Octal D-Type Flip-Flop with 3-State Output

The TC74HCT574A is a high speed CMOS OCTAL FLIP-FLOP with 3-STATE OUTPUT fabricated with silicon gate C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Its inputs are compatible with TTL, NMOS, and CMOS output voltage levels.

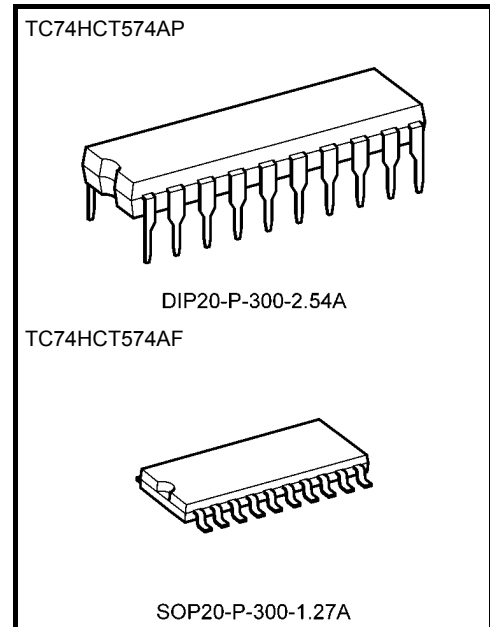
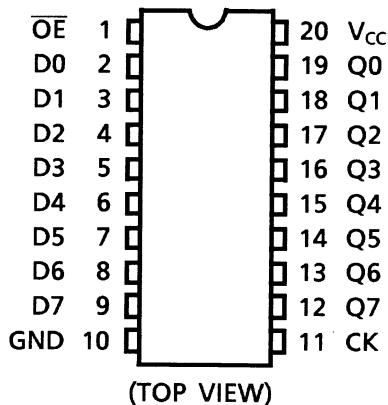
Its 8-bit D-type flip-flops is controlled by a clock input (CK) and an output enable input ( $\overline{OE}$ ).

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

### Features

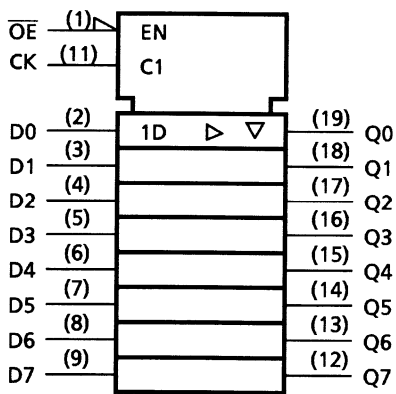
- High speed:  $f_{max} = 62$  MHz (typ.) at  $V_{CC} = 5$  V
- Low power dissipation:  $I_{CC} = 4$   $\mu$ A (max) at  $T_a = 25^\circ$ C
- Compatible with TTL outputs:  $V_{IL} = 0.8$  V (min)  
 $V_{IH} = 2.0$  V (max)
- Output drive capability: 15 LSTTL loads
- Symmetrical output impedance:  $|I_{OH}| = I_{OL} = 6$  mA (min)
- Balanced propagation delays:  $t_{pLH} \approx t_{pHL}$
- Pin and function compatible with 74LS574

### Pin Assignment



Weight	
DIP20-P-300-2.54A	: 1.30 g (typ.)
SOP20-P-300-1.27A	: 0.22 g (typ.)

## IEC Logic Symbol



## Truth Table

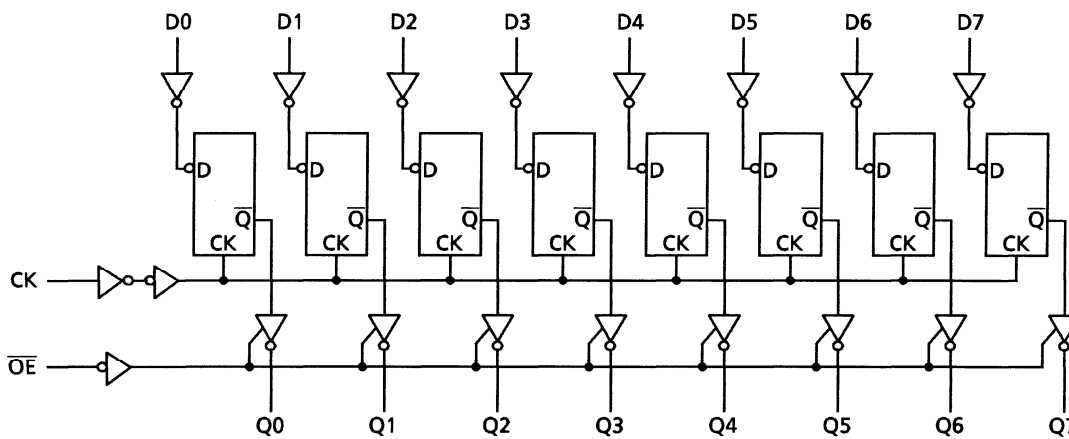
Inputs			Output
$\overline{OE}$	CK	D	Q
H	X	X	Z
L		X	$Q_n$
L		L	L
L		H	H

X: Don't care

Z: High impedance

$Q_n$ : No change

## System Diagram



## Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V <sub>CC</sub>	-0.5~7	V
DC input voltage	V <sub>IN</sub>	-0.5~V <sub>CC</sub> + 0.5	V
DC output voltage	V <sub>OUT</sub>	-0.5~V <sub>CC</sub> + 0.5	V
Input diode current	I <sub>IK</sub>	±20	mA
Output diode current	I <sub>OK</sub>	±20	mA
DC output current	I <sub>OUT</sub>	±35	mA
DC V <sub>CC</sub> /ground current	I <sub>CC</sub>	±75	mA
Power dissipation	P <sub>D</sub>	500 (DIP) (Note 2)/180 (SOP)	mW
Storage temperature	T <sub>stg</sub>	-65~150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of Ta = -40 to 65°C. From Ta = 65 to 85°C a derating factor of -10 mW/°C shall be applied until 300 mW.

## Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V <sub>CC</sub>	4.5~5.5	V
Input voltage	V <sub>IN</sub>	0~V <sub>CC</sub>	V
Output voltage	V <sub>OUT</sub>	0~V <sub>CC</sub>	V
Operating temperature	T <sub>opr</sub>	-40~85	°C
Input rise and fall time	t <sub>r</sub> , t <sub>f</sub>	0~500	ns

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either V<sub>CC</sub> or GND.

## Electrical Characteristics

### DC Characteristics

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40~85°C		Unit	
			V <sub>CC</sub> (V)	Min	Typ.	Max	Min		Max
High-level input voltage	V <sub>IH</sub>	—	4.5~5.5	2.0	—	—	2.0	—	V
Low-level input voltage	V <sub>IL</sub>	—	4.5~5.5	—	—	0.8	—	0.8	V
High-level output voltage	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OH</sub> = -20 μA	4.5	4.4	4.5	—	4.4	—	V
			4.5	4.18	4.31	—	4.13	—	
Low-level output voltage	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OL</sub> = 20 μA	4.5	—	0.0	0.1	—	0.1	V
			4.5	—	0.17	0.26	—	0.33	
3-state output off-state current	I <sub>OZ</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = V <sub>CC</sub> or GND	5.5	—	—	±0.5	—	±5.0	μA
Input leakage current	I <sub>IN</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND	5.5	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND	5.5	—	—	4.0	—	40.0	μA
	I <sub>C</sub>	Per input: V <sub>IN</sub> = 0.5 V or 2.4 V Other input: V <sub>CC</sub> or GND	5.5	—	—	2.0	—	2.9	mA

## Timing Requirements (input: $t_r = t_f = 6 \text{ ns}$ )

Characteristics	Symbol	Test Condition	Ta = 25°C		Ta = -40~85°C		Unit
			V <sub>CC</sub> (V)	Typ.	Limit	Limit	
Minimum pulse width (CK)	$t_W$ (H)	—	4.5	—	15	19	ns
	$t_W$ (L)		5.5	—	14	17	
Minimum set-up time (Dn)	$t_s$	—	4.5	—	15	19	ns
			5.5	—	14	17	
Minimum hold time (Dn)	$t_h$	—	4.5	—	0	0	ns
			5.5	—	0	0	
Clock frequency	f	—	4.5	—	31	25	MHz
			5.5	—	34	27	

## AC Characteristics (input: $t_r = t_f = 6 \text{ ns}$ )

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40~85°C		Unit		
			CL (pF)	V <sub>CC</sub> (V)	Min	Typ.	Max		Min	Max
Output transition time	$t_{TLH}$	—	50	4.5	—	7	12	—	15	ns
	$t_{THL}$			5.5	—	6	11	—	14	
Propagation delay time (CK-Q)	$t_{pLH}$	—	50	4.5	—	19	30	—	38	ns
				5.5	—	16	27	—	34	
	$t_{pHL}$		4.5	—	24	40	—	48		
			5.5	—	21	35	—	44		
Output enable time	$t_{pZL}$	$R_L = 1 \text{ k}\Omega$	50	4.5	—	19	30	—	38	ns
				5.5	—	16	27	—	34	
	$t_{pZH}$		4.5	—	24	40	—	48		
			5.5	—	21	35	—	44		
Output disable time	$t_{pLZ}$	$R_L = 1 \text{ k}\Omega$	50	4.5	—	19	30	—	38	ns
				5.5	—	16	27	—	34	
$t_{pHZ}$	4.5		—	24	40	—	48			
	5.5		—	21	35	—	44			
Maximum clock frequency	$f_{max}$	—	50	4.5	31	50	—	25	—	MHz
				5.5	34	60	—	27	—	
Input capacitance	$C_{IN}$	—	—	—	—	5	10	—	10	pF
Output capacitance	$C_{OUT}$	—	—	—	—	10	—	—	—	pF
Power dissipation capacitance	$C_{PD}$ (Note)	—	—	—	—	62	—	—	—	pF

Note:  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per bit)}$$

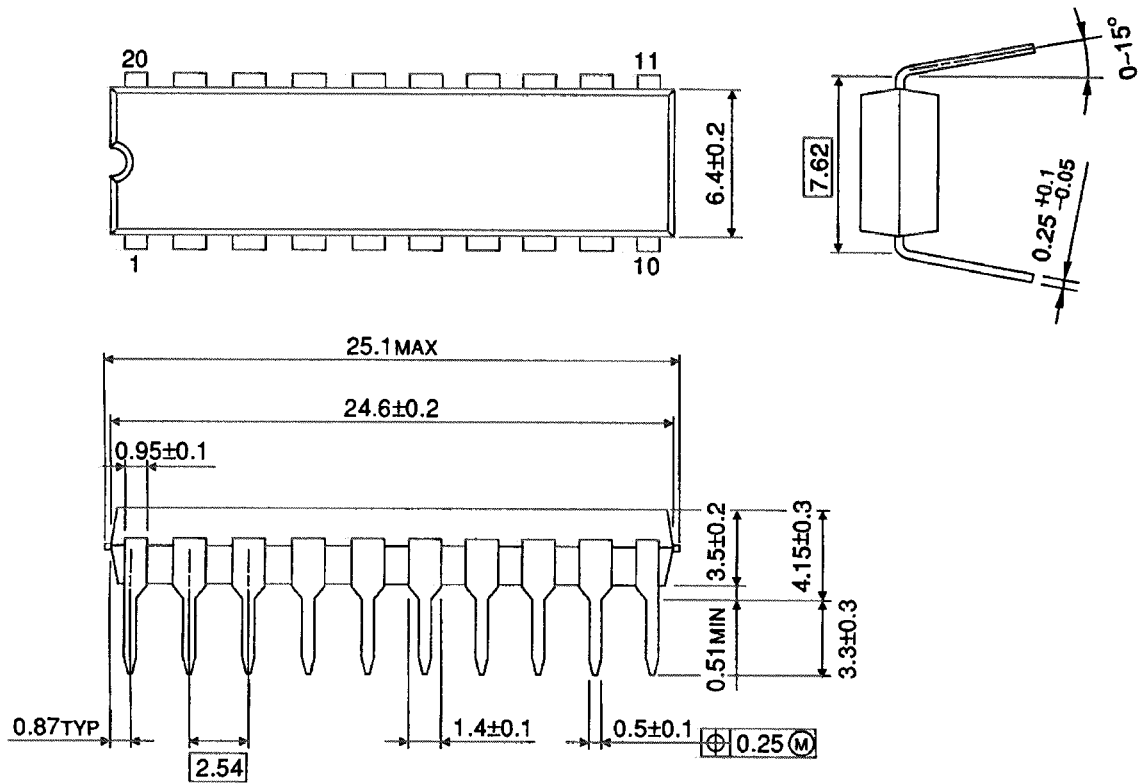
And the total  $C_{PD}$  when n pcs. of flip flop operate can be gained by the following equation:

$$C_{PD}(\text{total}) = 47 + 15 \cdot n$$

## Package Dimensions

DIP20-P-300-2.54A

Unit : mm

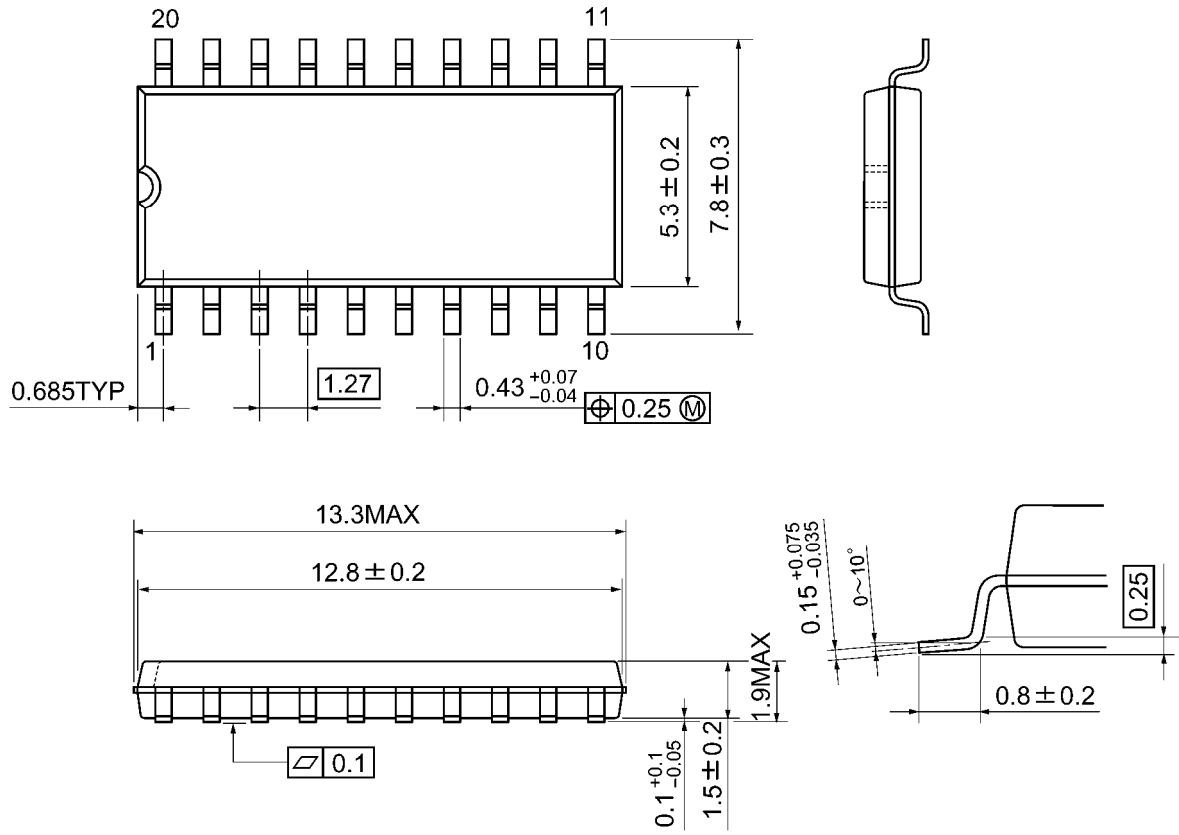


Weight: 1.30 g (typ.)

## Package Dimensions

SOP20-P-300-1.27A

Unit: mm



Weight: 0.22 g (typ.)

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