

Features

- Precision supply-voltage monitor
 - 4.63V (PT7M7xxxL)
 - 4.38V (PT7M7xxxM)
 - 3.08V (PT7M7xxxT)
 - 2.93V (PT7M7xxxS)
 - 2.63V (PT7M7xxxR)
 - 2.32V (PT7M7xxxZ)
 - 2.20V (PT7M7xxxY)
- 200ms reset pulse width
- Debounced CMOS-compatible manual-reset input (7811, 7812, 7823, 7825, 7342-7344)
- Reset Output Signal for Watchdog and Power Abnormal, Manual Reset
- Reset Push-Pull output (PT7M7809,7811,7823, 7824,7825,7342,7345)
- Reset Open-Drain output (PT7M7803/7343)
- Voltage monitor for power-fail or low battery warning
- Guaranteed $\overline{\text{RESET}}/\text{RESET}$ valid at $V_{CC} = 1.0V$

Introduction

The PT7M7xxx family microprocessor (μP) supervisory circuits are targeted to improve reliability and accuracy of power-supply circuitry in μP systems. These devices reduce the complexity and number of components required to monitor power-supply and battery functions.

The main functions are:

1. Asserting reset output during power-up, power-down and brownout conditions for μP system;
2. Detecting power failure or low-battery conditions with a 1.25V threshold detector;
3. Watchdog functions;
4. Manual reset.

Applications

- Power-supply circuitry in μP systems

Ordering Information

	Part No.	$\overline{\text{RESET}}$ output		RESET output (push-pull)	Manual Reset Input	Power Fail Detector (1.25V)	Watchdog Input	Package
		Push-Pull	Open-Drain					
1	PT7M7803XT	-	√	-	-	-	-	SOT23-3
2	PT7M7809XT	√	-	-	-	-	-	
3	PT7M7810XT	-	-	√	-	-	-	
4	PT7M7811XT	√	-	-	√	-	-	SOT23-5
5	PT7M7812XT	-	-	√	√	-	-	
6	PT7M7823XT	√	-	-	√	-	√	
7	PT7M7824XT	√	-	√	-	-	√	
8	PT7M7825XT	√	-	√	√	-	-	
9	PT7M7342XT	√	-	-	√	√	-	SOT23-6
10	PT7M7343XT	-	√	-	√	√	-	
11	PT7M7344XT	-	-	√	√	√	-	
12	PT7M7345XT	√	-	√	-	√	-	

Suffix: X -- Monitored Voltage

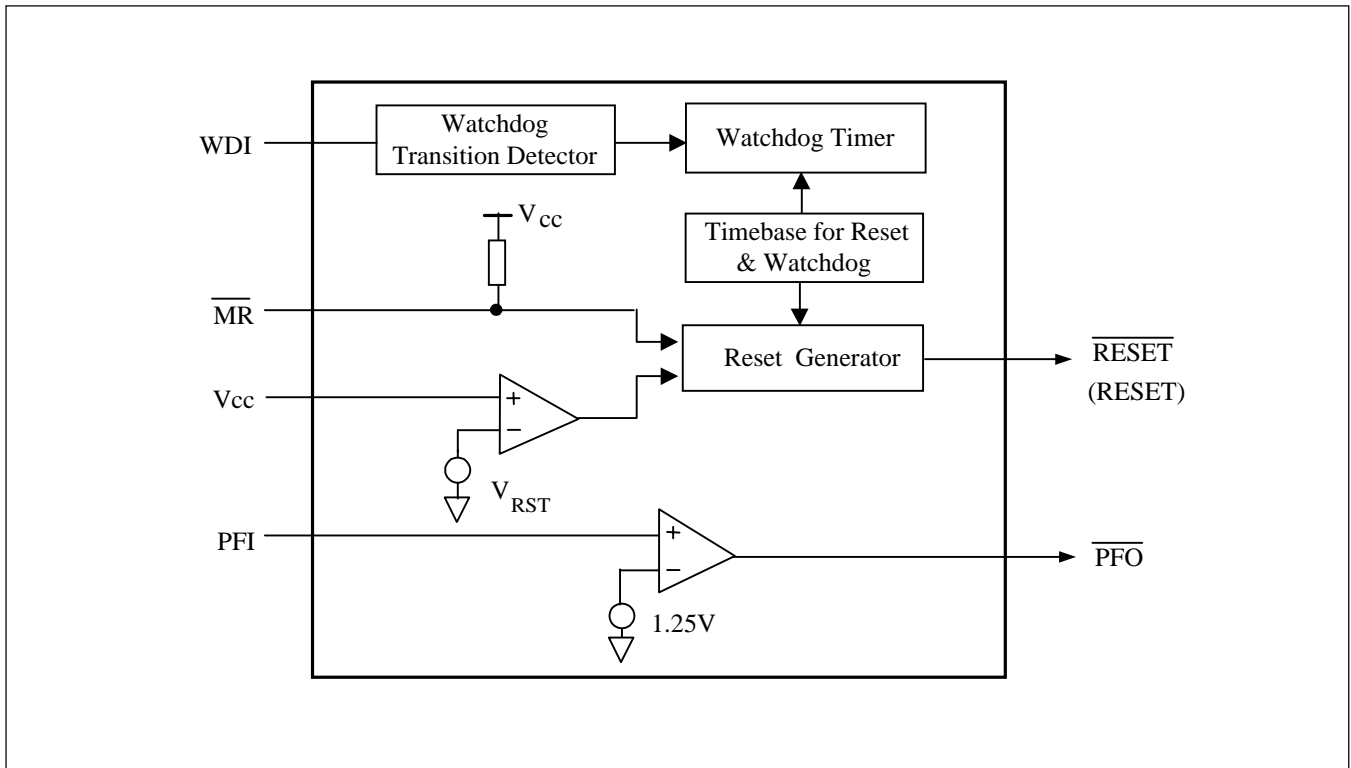
Suffix X	L	M	T	S	R	Z	Y
Reset threshold (V)	4.63	4.38	3.08	2.93	2.63	2.32	2.20

Contents

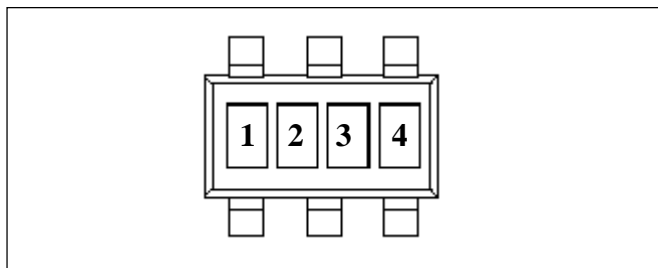
Features	1
Ordering Information	1
Introduction	1
Block Diagram	3
Marking Information	4
Pin Information	5
Pin Configuration	5
Pin Description	6
Functional Description	7
Reset Output	7
Watchdog Timer	7
Manual Reset	7
Power-Fail Comparator	7
Recommended Operation Condition	8
Detailed Specifications	8
Absolute Maximum Ratings	8
DC Electrical Characteristics	9
AC Electrical Characteristics	10
Mechanical Information	11
Notes	14

Block Diagram

Figure 1. Block Diagram



Marking Information



Code	Description
1 2	Part Number
3	Year
4	Work Week

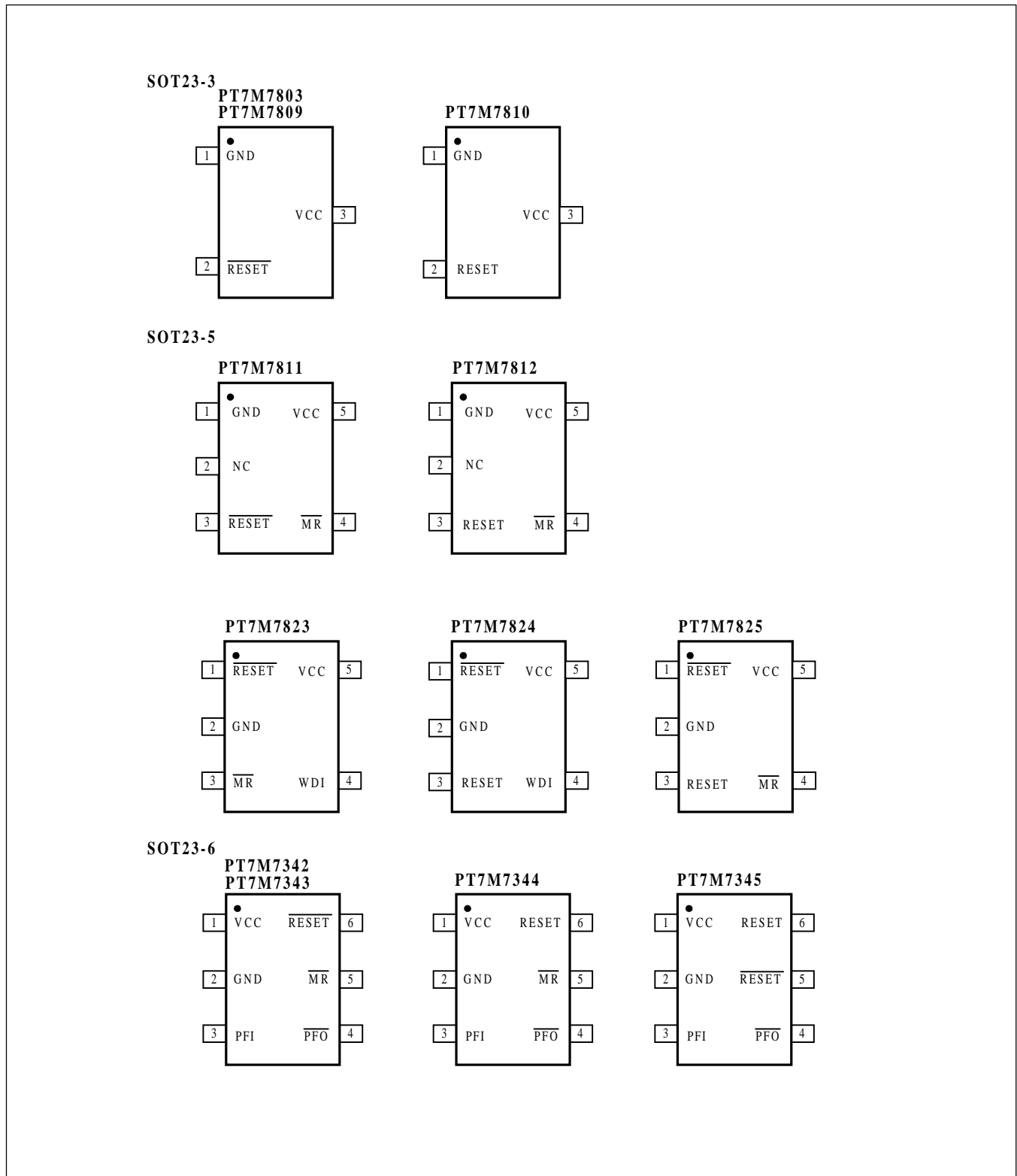
Part Number Code

Code 1 2	Part No.	Code 1 2	Part No.	Code 1 2	Part No.
AA	PT7M7809L	BC	PT7M7803L	CE	PT7M7342L
AB	PT7M7809M	BD	PT7M7803M	CF	PT7M7342M
AC	PT7M7809T	BE	PT7M7803T	CG	PT7M7342T
AD	PT7M7809S	BF	PT7M7803S	CH	PT7M7342S
AE	PT7M7809R	BG	PT7M7803R	CI	PT7M7342R
AF	PT7M7809Z	BH	PT7M7803Z	CJ	PT7M7342Z
AG	PT7M7809Y	BI	PT7M7803Y	CK	PT7M7342Y
AH	PT7M7810L	BJ	PT7M7823L	CL	PT7M7343L
AI	PT7M7810M	BK	PT7M7823M	CM	PT7M7343M
AJ	PT7M7810T	BL	PT7M7823T	CN	PT7M7343T
AK	PT7M7810S	BM	PT7M7823S	CO	PT7M7343S
AL	PT7M7810R	BN	PT7M7823R	CP	PT7M7343R
AM	PT7M7810Z	BO	PT7M7823Z	CQ	PT7M7343Z
AN	PT7M7810Y	BP	PT7M7823Y	CR	PT7M7343Y
AO	PT7M7811L	BQ	PT7M7824L	CS	PT7M7344L
AP	PT7M7811M	BR	PT7M7824M	CT	PT7M7344M
AQ	PT7M7811T	BS	PT7M7824T	CU	PT7M7344T
AR	PT7M7811S	BT	PT7M7824S	CV	PT7M7344S
AS	PT7M7811R	BU	PT7M7824R	CW	PT7M7344R
AT	PT7M7811Z	BV	PT7M7824Z	CX	PT7M7344Z
AU	PT7M7811Y	BW	PT7M7824Y	CY	PT7M7344Y
AV	PT7M7812L	BX	PT7M7825L	CZ	PT7M7345L
AW	PT7M7812M	BY	PT7M7825M	DA	PT7M7345M
AX	PT7M7812T	BZ	PT7M7825T	DB	PT7M7345T
AY	PT7M7812S	CA	PT7M7825S	DC	PT7M7345S
AZ	PT7M7812R	CB	PT7M7825R	DD	PT7M7345R
BA	PT7M7812Z	CC	PT7M7825Z	DE	PT7M7345Z
BB	PT7M7812Y	CD	PT7M7825Y	DF	PT7M7345Y

Pin Information

Pin Configuration

Figure 2. Pin Configuration



Pin Description

Table 2. Pin Description

Pin Name	Type	Description
$\overline{\text{MR}}$	I	Manual-Reset: (CMOS). Active low. Pull low to force a reset. Reset remains asserted for the duration of the Reset Timeout Period after $\overline{\text{MR}}$ transitions from low to high. Leave unconnected or connected to VCC if not used.
Vcc	Power	Power Supply: Reset is asserted when V_{CC} drops below the Reset Threshold Voltage (V_{RST}). Reset remains asserted until V_{CC} rises above V_{RST} and keep asserted for the duration of the Reset Timeout Period (t_{RS}) once V_{CC} rises above V_{RST} .
GND	Ground	Ground Reference for all signals
PFI	I	Power-Fail Voltage Monitor Input. When $\text{PFI} < V_{\text{PFT}}$, $\overline{\text{PFO}}$ goes low. Connect PFI to GND or Vcc when not used.
$\overline{\text{PFO}}$	O	Power-Fail Output: it gets low and sinks current when PFI is less than 1.25V; otherwise PFO stays high.
WDI	I	Watchdog Input (CMOS). If WDI remains high or low for the duration of the watchdog timeout period (t_{WD}), the internal watchdog timer trigger a reset output. Floating WDI or connecting WDI to a high-impedance three-state buffer disables the watchdog feature. The internal watchdog timer clears whenever reset is asserted or WDI occurs a rising or falling edge.
$\overline{\text{RESET}}$	O	Active-Low Reset Output (Push-Pull or Open-Drain). It goes low when Vcc is below the reset threshold. It remains low for about 200ms after one of the following occurs: Vcc rises above the reset threshold (V_{RST}), the watchdog triggers a reset, or $\overline{\text{MR}}$ goes from low to high.
RESET	O	The inverse of $\overline{\text{RESET}}$, active high. Whenever $\overline{\text{RESET}}$ is high, RESET is low.
NC	-	No connection

Functional Description

Reset Output

A microprocessor's (μP's) reset input starts the μP in a known state. Whenever the μP is in an unknown state, it should be held in reset. The supervisory circuits assert reset during power-up and prevent code execution errors during power-down or brownout conditions.

On power-up, once Vcc reaches about 1.0V, $\overline{\text{RESET}}$ is a guaranteed logic low of 0.4V or less. As Vcc rises, $\overline{\text{RESET}}$ stays low. When Vcc rises above the reset threshold, an internal timer releases $\overline{\text{RESET}}$ after about 200ms. $\overline{\text{RESET}}$ pulses low whenever Vcc drops below the reset threshold, i.e. brownout condition. If brownout occurs in the middle of a previously initiated reset pulse, the pulse continues for at least another 200ms. On power-down, once Vcc falls below the reset threshold, $\overline{\text{RESET}}$ stays low and is guaranteed to be 0.4V or less until Vcc drops below 1.0V. Fig 4 shows the timing relationship.

The active-high RESET output is simply the inverse of the $\overline{\text{RESET}}$ output, and is guaranteed to be valid with Vcc down to 1.0V.

Watchdog Timer

The PT7M7xxx watchdog circuit monitors the μP's activity. If the μP does not toggle the watch-dog input (WDI) within 1.6s, reset asserts. As long as reset is asserted or the WDI input is toggled, the watchdog timer will stay clear and will not count. As soon as reset is released, the timer will start counting. WDI input pulses as short as 50ns can be detected. Disable the watchdog function by leaving WDI unconnected or by three-stating driver connected to WDI.

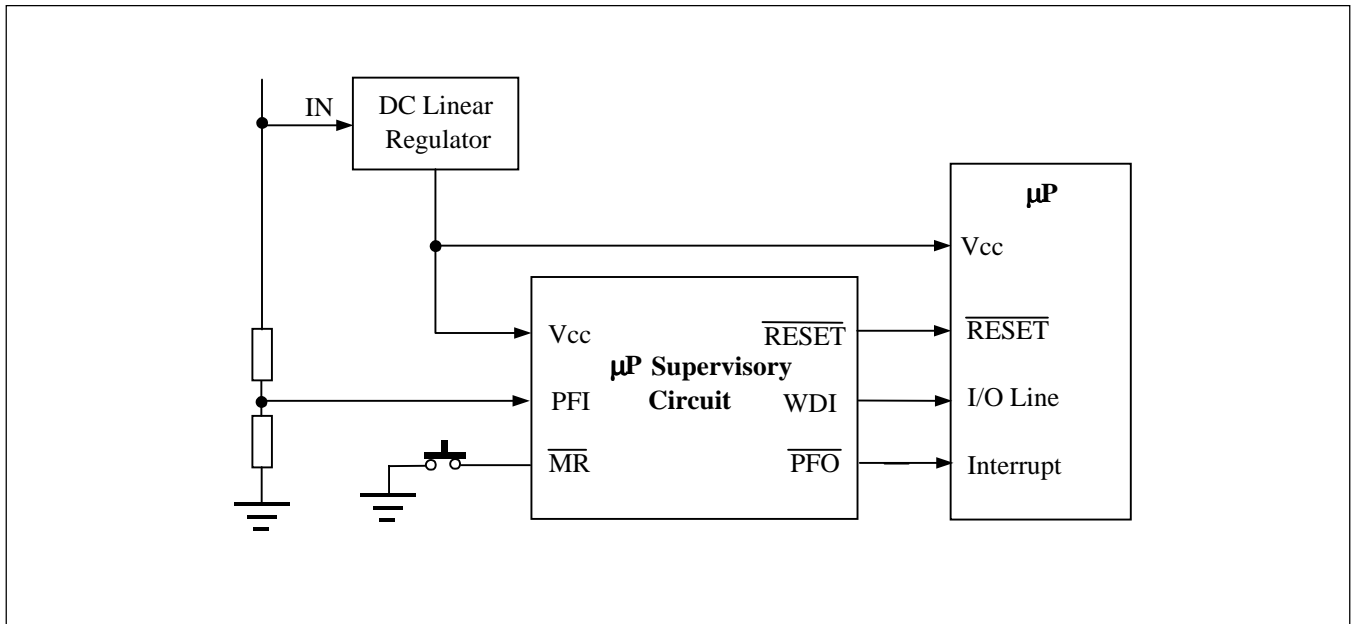
Manual Reset

The manual-reset input ($\overline{\text{MR}}$) allows reset to be triggered by a push button switch. $\overline{\text{MR}}$ has an internal pullup resistor, so it can be left open when not used.

Power-Fail Comparator

The power-fail comparator can be used for various purposes because its output and noninverting input are not internally connected. The inverting input is internally connected to a 1.25V reference.

Figure 3. Typical Application Circuit



Detailed Specifications

Absolute Maximum Ratings

Storage Temperature	-65°C to +150°C	Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
Ambient Temperature with Power Applied	-40°C to +85°C	
Supply Voltage to Ground Potential (V _{cc} to GND)	-0.3V to +7.0V	
DC Input Voltage (All inputs except V _{cc} and GND)	-0.3V to V _{cc} +0.3V	
DC Output Current (All outputs)	20mA	
Power Dissipation	320mW (Depend on package)	

Recommended Operation Condition

Table 3. DC Electrical Characteristics

Sym	Description	Test Conditions	Min	Typ	Max	Unit
V _{cc}	Supply Voltage for 7xxxL, 7xxxM		4.5	5.0	5.5	V
	Supply Voltage for 7xxxT, 7xxxS		3.0	3.3	5.5	V
	Supply Voltage for 7xxxR		2.7	3.0	5.5	V
	Supply Voltage for 7xxxZ, 7xxxY		2.4	2.5	5.5	V
V _{IH}	Input High Voltage		0.7V _{cc}			V
V _{IL}	Input Low Voltage				0.3V _{cc}	V
T _A	Operating Temperature		-40		85	°C

DC Electrical Characteristics

Table 4. DC Electrical Characteristics

($V_{CC}=V_{RN}+5\%$ to 5.5V, $T_A=-40\sim 85^\circ\text{C}$, unless otherwise noted)

Symbol	Description	Test Conditions	Min	Typ	Max	Unit	
V_{CC}	Operating Voltage Range		1.0		5.5	V	
I_{CC}	Supply Current	$V_{CC} = 5V$, No load		20	50	μA	
V_{IH}	Input High Voltage	Pin: \overline{MR} , WDI	0.7 V_{CC}			V	
V_{IL}	Input Low Voltage	Pin: \overline{MR} , WDI			0.3 V_{CC}	V	
V_{RST}	Reset Threshold Voltage (Note 1)	$T_A = -40 \sim 85^\circ\text{C}$	$V_{RN}-2.5\%$	V_{RN}	$V_{RN}+2.5\%$	V	
			PT7M7xxxL	4.514	4.63		4.746
			PT7M7xxxM	4.271	4.38		4.490
			PT7M7xxxT	3.003	3.08		3.157
			PT7M7xxxS	2.857	2.93		3.003
			PT7M7xxxR	2.564	2.63		2.696
			PT7M7xxxZ	2.262	2.32		2.378
			2.145	2.20	2.255		
V_{RTH}	Reset Threshold Hysteresis(Note 1)	V_{CC} varies between $V_{RN}\pm 5\%$		70		mV	
V_{OH}	Output High Voltage	$V_{CC} \geq 4.5V$ $I_{source}=800\mu A$	$V_{CC}-1.5$			V	
		$V_{CC} \geq 2.7V$ $I_{source}=500\mu A$	0.8 V_{CC}				
		$V_{CC} \geq 1.8V$ $I_{source}=150\mu A$	0.8 V_{CC}				
V_{OL}	Output Low Voltage	$V_{CC} \geq 4.5V$ $I_{sink}=3.2mA$			0.4	V	
		$V_{CC} \geq 2.7V$ $I_{sink}=1.2mA$			0.3		
		$V_{CC} \geq 1.2V$ $I_{sink}=100\mu A$			0.3		
I_{LKG}	Open-Drain Output Leakage Current	$V_{CC} > V_{TH(MAX)}$ for PT7M7803 and PT7M7345			1	μA	
V_{PFI}	PFI Input Threshold	V_{PFI} varies from 1.5V and 1.0V	1.20	1.25	1.30	V	
I_{PFI}	PFI Input Leakage Current				±25	nA	
I_{WDI}	Average WDI Input Current (Note 2)	WDI connected to V_{CC} : 5.5V		120	160	μA	
		WDI connected to GND	-20	-15			
r	MR pull-up resistor (internal)	PT7M7811/7812	10	20	30	kΩ	
		PT7M7823/7824/7825	35	52	75		
		PT7M7342/7343/7344	60				

* Valid for both RESET and RESET. V_{RN} is nominal reset threshold voltage.

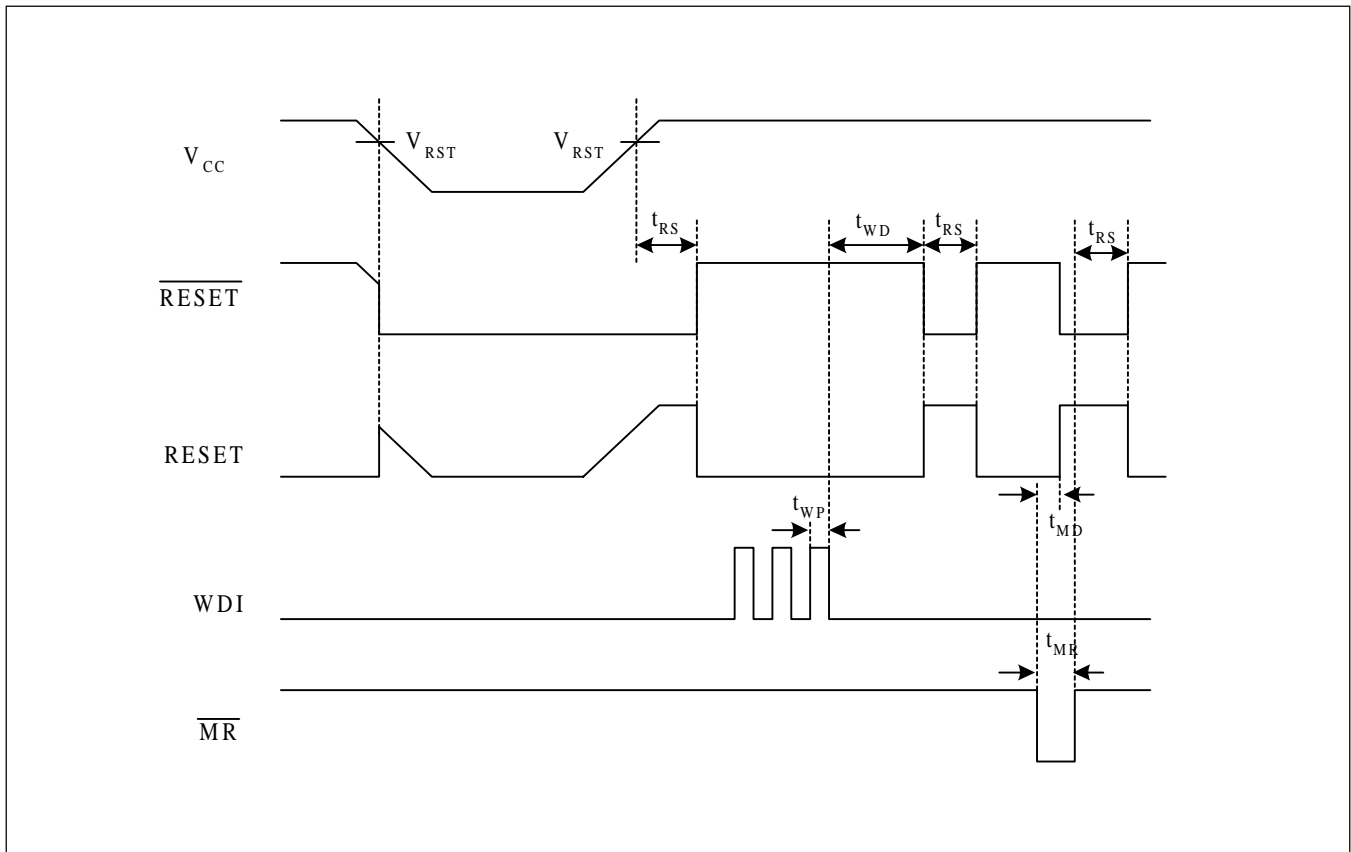
** WDI is internally serviced within the watchdog period if WDI is left unconnected.

AC Electrical Characteristics

Table 5. AC Electrical Characteristics

Sym	Description	Test Conditions	Min	Typ	Max	Units
t_{RS}	Reset Pulse Width	\overline{MR} from low to High	140	200	280	ms
t_{WD}	Watchdog Timeout Period	WDI and \overline{MR} tied to V_{CC} , $V_{CC} > V_{RN} + 5\%$	1.12	1.6	2.25	s
t_{MR}	\overline{MR} Pulse Width		1			μs
t_{MD}	\overline{MR} to RESET Delay	$V_{CC} = 5.0V$			250	ns
t_{WP}	WDI Pulse Width		50			ns

Figure 4. Watchdog Timing Diagram



Mechanical Information

Figure 5. SOT23-3

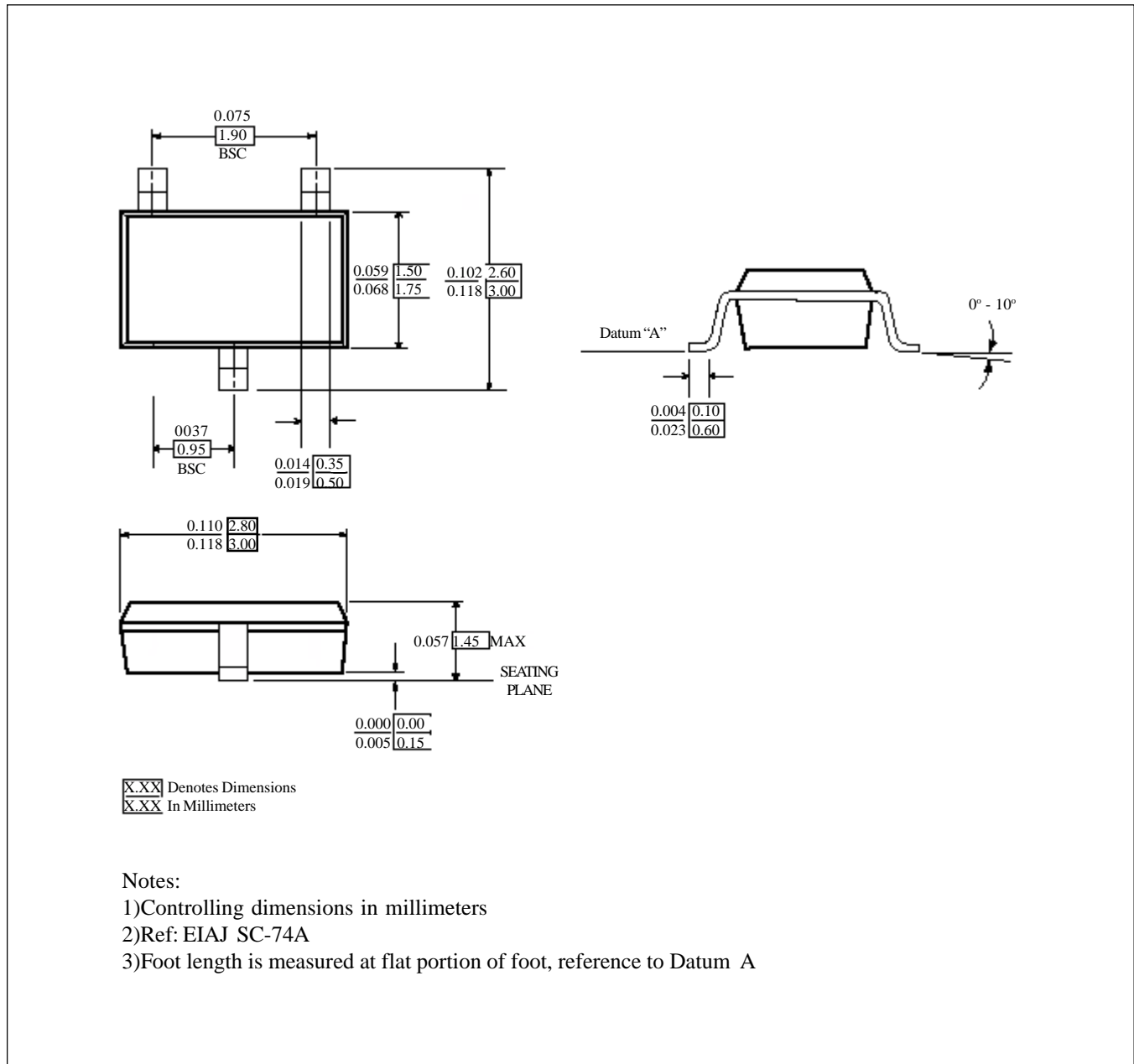


Figure 6. SOT23-5

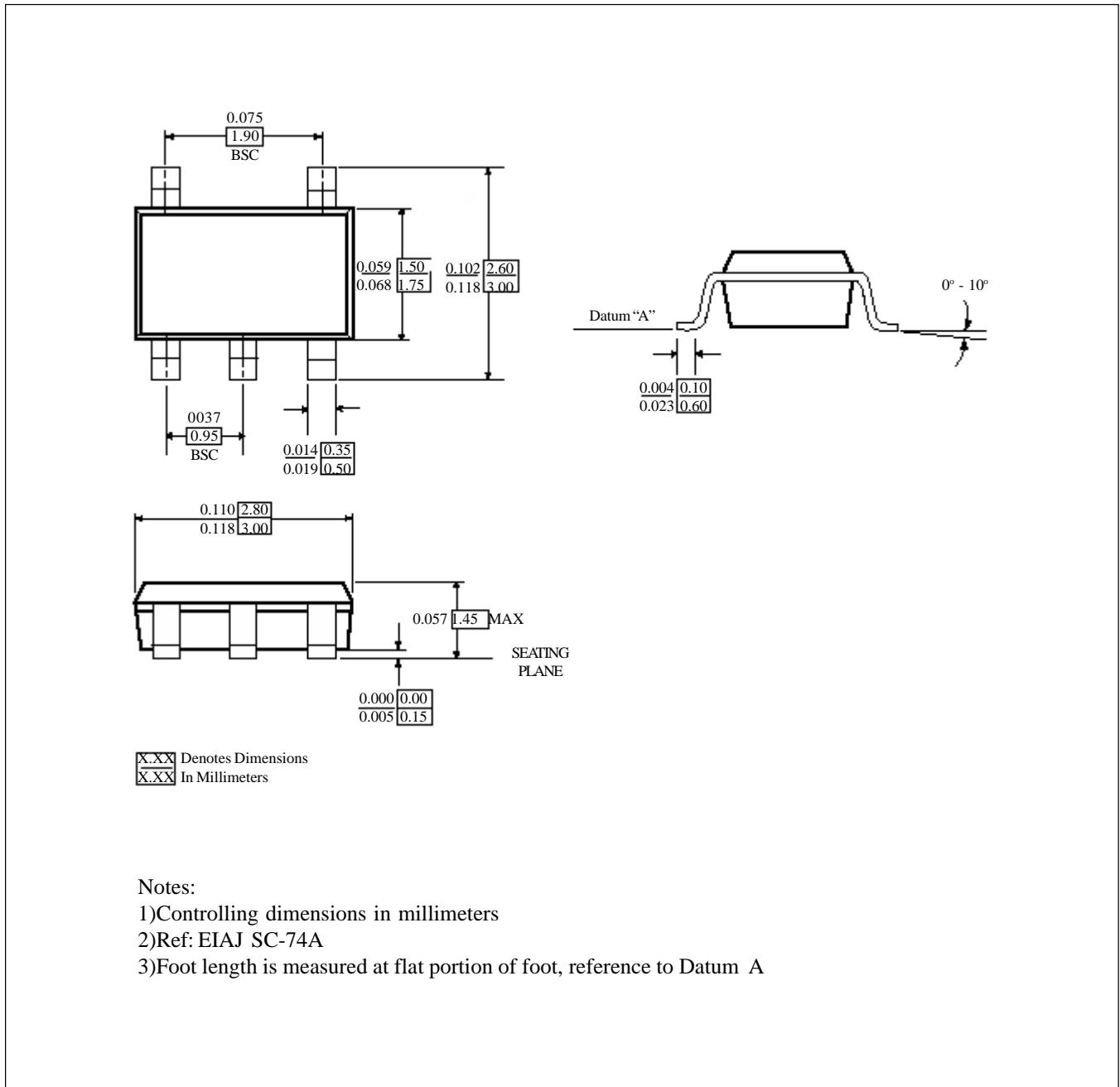
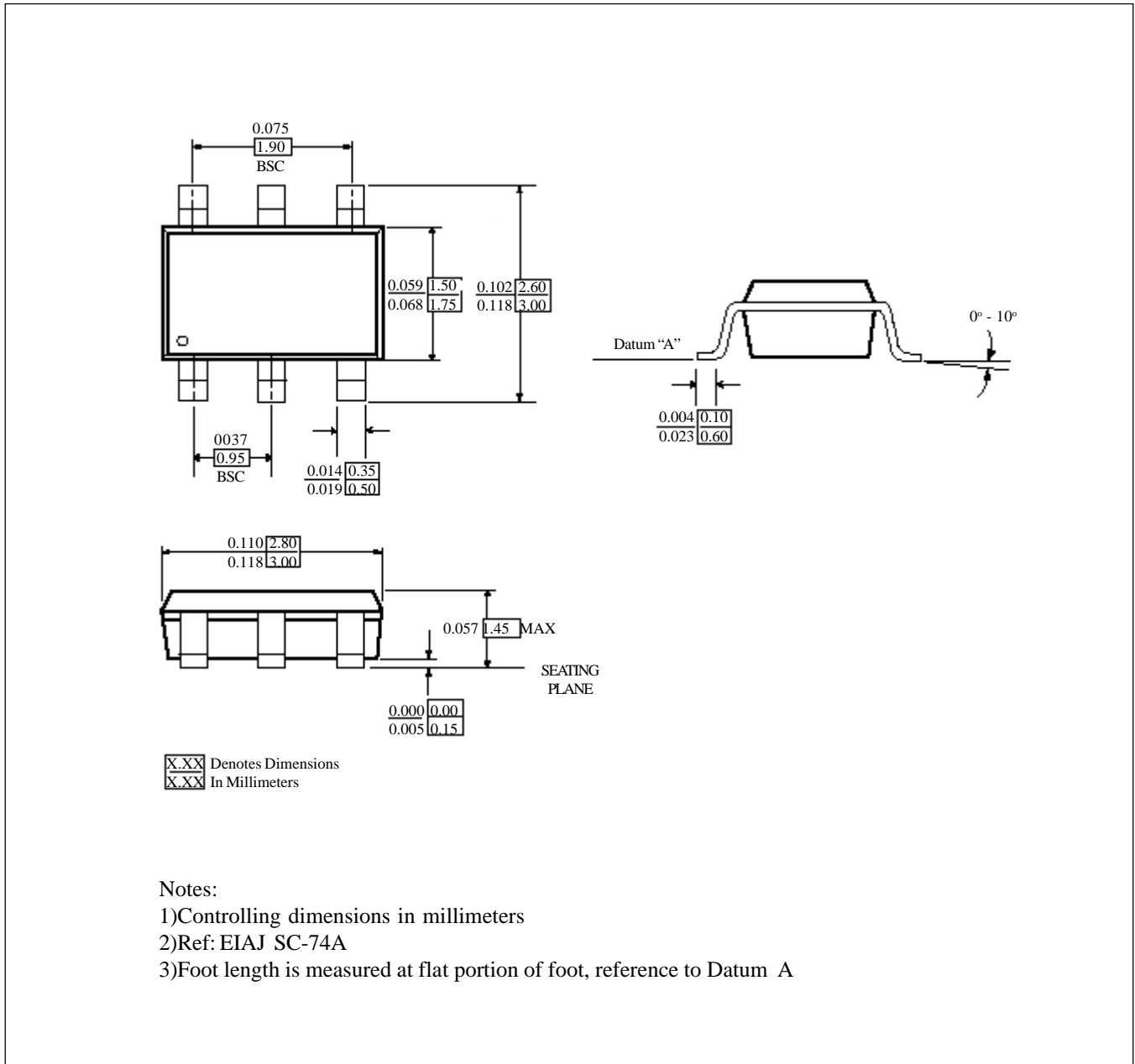


Figure 7. SOT23-6



Notes

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