TPS61176 High-Efficiency 6-Channel WLED Driver Supporting Single-Cell Li-Ion Battery Input

1 Features

- 2.7-V to 6.5-V V_{IN} Voltage Range
- 2.7-V to 24-V Boost Input Voltage Range
- Integrated 2-A/40-V MOSFET
- 1-MHz Switching Frequency
- Adaptive Boost Output to WLED Voltages
- Six Current Sinks of 35 mA Capability Each
- ±2% (Maximum) Current Accuracy
- 1.3% (Typical) Current Matching
- 100-Hz to 22-kHz Input PWM Frequency
- Mixed Dimming Mode: Automatic Switch Between Analog Dimming and PWM Dimming
  - Programmable Switch Point: 25% or 12.5%
  - Programmable PWM Dimming Mode: 22-kHz PWM Dimming, Direct PWM Dimming
- Up to 14-bit Dimming Resolution
- Support Down to 1% Dimming Duty Cycle
- Input PWM Glitch Filter
- Up to 90% Efficiency
- Driver for Input and Output Isolation PFET for True Shutdown
- Built-in WLED Open and Short Protection
- Thermal Shutdown

2 Applications

Backlight for Small and Media Form Factor LCD Display with Single-Cell or Multi-Cell Battery Input

3 Description

The TPS61176 is an integrated WLED backlight driver for tablets or notebook PCs using single-cell batteries. It comprises a high-efficiency boost converter with an integrated 2-A, 40-V power MOSFET, and six current sink regulators. The device can drive up to 60 WLEDs. The boost output voltage automatically adjusts to the WLED forward voltage to improve efficiency.

The TPS61176 supports mixed dimming mode. The automatic switch between PWM dimming and analog dimming increases the overall electrical-to-optical efficiency, reducing power of the backlight significantly. The switch point can be programmed to 12.5% or 25%. PWM dimming mode can also be programmed to fixed frequency dimming or direct PWM dimming. The device supports up to 14-bit dimming resolution to avoid potential flickering during low brightness dimming.

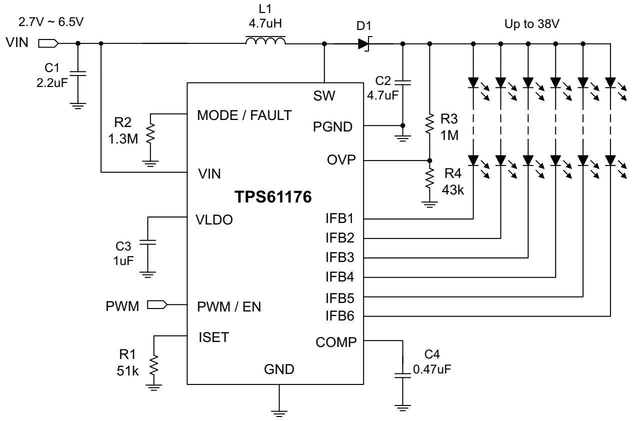
True shutdown is supported with a driver for an external isolation P-channel MOSFET. When the device is disabled or the boost output is shorted to ground, the isolation PFET is turned off to cut off the power path from battery preventing any leakage current from the battery. The device also integrates soft start, thermal shutdown, WLED open and short protection. Its 16-pin WQFN package provides a space-saving and high-performance WLED driver solution.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS61176	WQFN (16)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



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4 Revision History

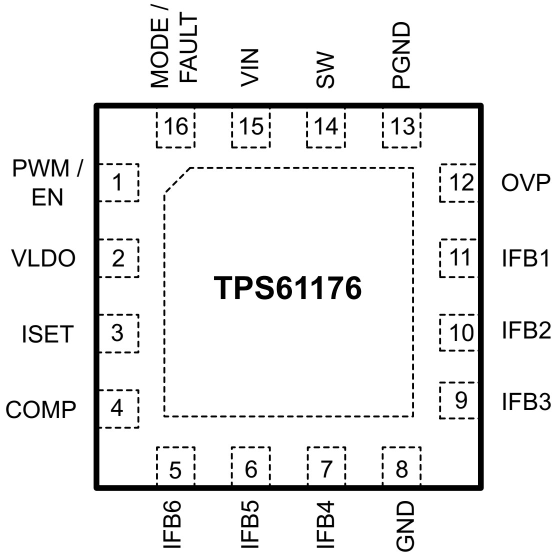
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (August 2013) to Revision B	**Page**
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1

Changes from Original (December 2012) to Revision A	**Page**
• Aligned package description throughout datasheet.	1

5 Pin Configuration and Functions

RTE Package
16-Pin WQFN with Exposed Thermal Pad
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NUMBER		
COMP	4	Analog	Connect an external 0.47-μF ceramic capacitor to this pin for the boost loop compensation.
GND	8	Ground	Analog ground
IFB4 to IFB6, IFB1 to IFB3	5, 6, 7, 9, 10, 11	Analog	Regulated current sinks input pins
ISET	3	Analog	Full-scale LED current setting pin. Connect a resistor to the pin to program the full-scale LED current.
MODE/FAULT	16	Input	Multi-function pin. Use this pin to program the dimming mode. It also functions as a driver for external isolation P-channel MOSFET.(1)
OVP	12	Analog	This pin monitors the output voltage of the boost converter through external resistor divider.
PGND	13	Ground	Power ground
PWM/EN	1	Input	PWM dimming signal input and device enable / disable control.(1)
SW	14	Analog	Drain of the internal power MOSFET.
VIN	15	Power	Supply input pin, provides power supply to the device.
VLDO	2	Analog	Internal pre-regulator output. Connect a 1-μF ceramic capacitor to this pin.
Thermal Pad	—	—	The GND pin should be connected to the exposed thermal pad for proper operation. This thermal pad should be connected to any internal PCB ground plan using multiple vias for good thermal performance.

(1) See *Detailed Description* for details.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage range(2)	VIN, PWM/EN, MODE/FAULT	–0.3	7	V
	SW	–0.3	40	V
	IFB1 to IFB6	–0.3	20	V
	All other pins	–0.3	3.6	V
Continuous power dissipation		See *Thermal Information*		
Operating junction temperature		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±2000	
		Machine model	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Bias voltage to device (see Figure 18)	2.7		6.5	V
	Input voltage to inductor (see Figure 18)	2.7		24	V
V_{OUT}	Output voltage range	V_{IN}		38	V
L	Inductor	4.7	6.8	10	µH
C_I	Input capacitor	1.0	2.2		µF
C_O	Output capacitor	2.2	4.7	10	µF
C_{COMP}	COMP capacitor	0.47		1	µF
F_{PWM_I}	Input PWM signal frequency	0.1		22	kHz
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS61176 RTE (WQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	43	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	44.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	14.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

V_{IN} = 3.6 V, PWM/EN = high, IFB current = 20 mA, IFB voltage = 450 mV, T_A = –40°C to +85°C, typical values are at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{IN}	Input voltage range		2.7		6.5	V
V_{IN_UVLO}	VIN undervoltage lockout threshold	V_{IN} ramp down		2.4	2.5	V
		V_{IN} ramp up		2.65	2.7	
V_{IN_HYS}	VIN undervoltage lockout hysteresis			250		mV
I_{q_VIN}	Operating quiescent current into VIN	Device enable, switching 1 MHz and no load			3	mA
I_{SD}	Shutdown current	PWM/EN = low		1	4	µA
		PWM/EN = low, T_A = 25°C		1	2	
V_{LDO}	VLDO pin output voltage	V_{IN} = 3.6 V	3	3.3	3.5	V
PWM/EN						
V_H	PWM/EN logic high		1.2			V
V_L	PWM/EN logic Low				0.4	V
R_{PD}	PWM/EN pin internal pull-down resistor		400	800	1600	kΩ
t_{SD}	PWM/EN logic low width to shutdown	PWM/EN from high to low	20			ms
CURRENT REGULATION						
V_{ISET}	ISET pin voltage	PWM/EN logic high	1.02	1.04	1.06	V
K_{ISET}	Current multiplier	I_{ISET} = 20 µA		1024		
I_{FBx}	Current accuracy	I_{ISET} = 20 µA, 0°C to 70°C	–2%		2%	
		I_{ISET} = 20 µA, –40°C to 85°C	–2.3%		2.3%	
K_m	$(I_{MAX} – I_{MIN}) / (2 \times I_{AVG})$	I_{ISET} = 20 µA		0.65%		
I_{IFBx_leak}	IFBx pin leakage current	V_{IFBx} = 10 V, each pin		1.5	5	µA
		V_{IFBx} = 5 V, each pin		0.5	2	
I_{IFBx_max}	Current sink max output current	I_{ISET} = 35 µA, each pin	35			mA
T_{FBx_MINON}	Current sink minimum on time	I_{ISET} = 20 µA, each pin		0.5		µs
f_{dim}	PWM dimming frequency	Mode 1 / Mode 3, 0°C to 70°C	20	22	27	kHz
BOOST OUTPUT REGULATION						
V_{IFBx_min}	IFBx regulation voltage	Measured on $V_{IFB(MIN)}$, I_{ISET} = 20 µA		450		mV
POWER SWITCH						
$R_{DS(on)}$	Switch MOSFET on-resistance	V_{IN} = 3.6 V		0.25	0.4	Ω
I_{LEAK_SW}	Switch MOSFET leakage current	V_{SW} = 40 V			2	µA
OSCILLATOR						
f_{SW}	Oscillator frequency		0.8	1	1.2	MHz
D_{max}	Maximum boost switch duty cycle			93%		
MODE/FAULT						
V_{MODE}	MODE/FAULT pin voltage during mode detection period	Tested as V_{IN} – V_{MODE} when mode resistor is connected between VIN pin and MODE/FAULT pin; Tested as V_{MODE} when mode resistor is connected between MODE/FAULT pin and GND		0.6	0.9	V
I_{MODE_PD}	MODE/FAULT pin pulldown current after mode detection	V_{MODE} = 0.5 V, mode resistor is connected between VIN pin and MODE/FAULT pin	50	80		µA

Electrical Characteristics (continued)

V_{IN} = 3.6 V, PWM/EN = high, IFB current = 20 mA, IFB voltage = 450 mV, T_A = –40°C to +85°C, typical values are at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OC, SC, OVP and SS						
I_{LIM}	Switch MOSFET current limit		2	2.5	3	A
V_{OVP_clamp}	Output overvoltage clamp threshold		1.47	1.5	1.53	V
V_{OVP_sd}	Output overvoltage shutdown threshold	OVP ramp up	1.568	1.6	1.632	V
		OVP ramp down	1.519	1.55	1.581	
V_{OVP_SC}	Output short to GND detection threshold	OVP ramp up		90		mV
		OVP ramp down	50	70		
V_{OVP_IFB}	1st level IFB overvoltage threshold	IFBx current sink on	7	8.5	10	V
V_{OVP2_IFB}	2nd level IFB overvoltage threshold	IFBx current sink on or off	16	18	20	V
THERMAL SHUTDOWN						
$T_{shutdown}$	Thermal shutdown threshold			160		°C
T_{hys}	Thermal shutdown hysteresis			15		°C

6.6 Typical Characteristics

Table 1. Table Of Graphs

TITLE	DESCRIPTION	FIGURE
Dimming Efficiency	V_{BAT} = 3 V, 3.6 V, 4.2 V, 5 V; V_O = 18 V, 6s6p, 20 mA/string; PWM Freq = 200 Hz; Mode 1; L = 6.8 µH	Figure 1
Dimming Efficiency	V_{BAT} = 3 V, 3.6 V, 4.2 V, 5 V; V_O = 21 V, 7s6p, 20 mA/string; PWM Freq = 200 Hz; Mode 1; L = 6.8µH	Figure 2
Dimming Efficiency	V_{BAT} = 3 V, 3.6 V, 4.2 V, 5 V; V_O = 24 V, 8s5p, 20 mA/string; PWM Freq = 200 Hz; Mode 1; L = 6.8 µH	Figure 3
Dimming Efficiency	V_{BAT} = 3 V, 3.6 V, 4.2 V, 5 V; V_O = 27 V, 9s4p, 20 mA/string; PWM Freq = 20 0Hz; Mode 1; L = 6.8µH	Figure 4
Dimming Efficiency	V_{IN} = 5 V; V_{BAT} = 3 V, 3.6 V, 4.2 V, 5 V, 7.2 V, 9 V, 12 V, 15 V; V_O = 18 V, 6s6p, 20 mA/string; PWM Freq = 200 Hz; Mode 1; L = 6.8 µH (refer to Figure 18)	Figure 5
Dimming Linearity	V_{BAT} = 3 V, 3.6 V, 4.2 V, 5 V; V_O = 21 V, 7s6p; R_{ISET} = 53 kΩ ; PWM Freq = 200 Hz; Mode 1	Figure 6
Current Limit vs Input Voltage	V_O = 30 V; T_A = 25°C	Figure 7
Switching Waveform	V_{BAT} = 3.6 V; V_O = 18 V, 6s6p; R_{ISET} = 53 kΩ; Duty = 100%; L = 6.8 µH	Figure 11
Switching Waveform	V_{BAT} = 3.6 V; V_O = 18 V, 6s6p; R_{ISET} = 53 kΩ; PWM Freq = 200 Hz; Duty = 50%; L = 6.8 µH; Mode 1	Figure 12
Switching Waveform	V_{BAT} = 3.6 V; V_O = 18 V, 6s6p; R_{ISET} = 53 kΩ; PWM Freq = 200 Hz; Duty = 10%; L = 6.8 µH; Mode 1	Figure 13
Switching Waveform	V_{BAT} = 3.6 V; V_O = 18 V, 6s6p; R_{ISET} = 53 kΩ; PWM Freq = 200 Hz; Duty = 50%; L = 6.8 µH; Mode 2	Figure 14
Switching Waveform	V_{BAT} = 3.6 V; V_O = 18 V, 6s6p; R_{ISET} = 53 kΩ; PWM Freq = 200Hz; Duty = 10%; L = 6.8 µH; Mode 2	Figure 15
Start-up Waveform	V_{BAT} = 3.6 V; V_O = 18 V, 6s6p; R_{ISET} = 53 kΩ; Duty = 100%; L = 6.8 µH	Figure 16
Start-up Waveform	V_{BAT} = 3.6 V; V_O = 18 V, 6s6p; R_{ISET} = 53 kΩ; PWM Freq = 200 Hz; Duty = 10%; L = 6.8 µH; Mode 1	Figure 17

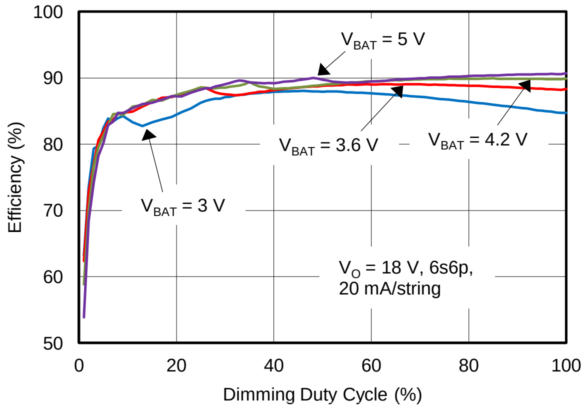


Figure 1. Efficiency vs Dimming Duty Cycle

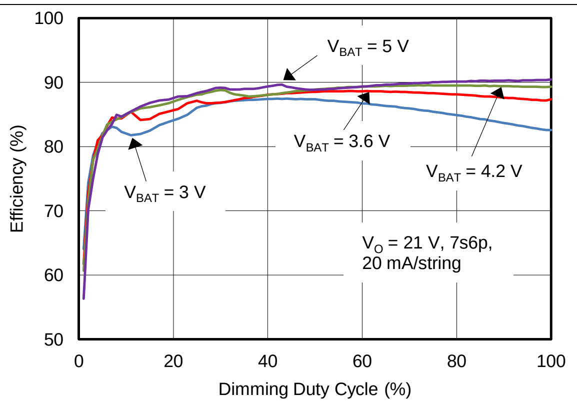


Figure 2. Efficiency vs Dimming Duty Cycle

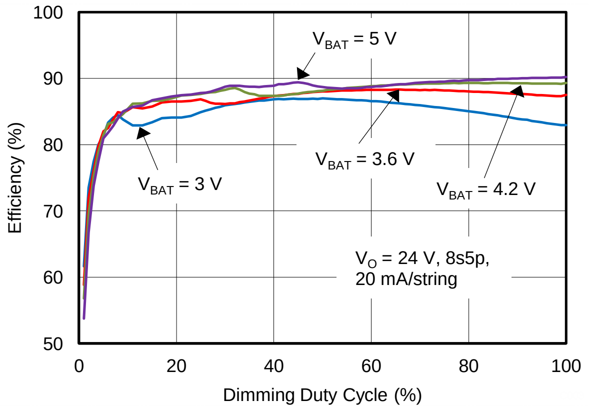


Figure 3. Efficiency vs Dimming Duty Cycle

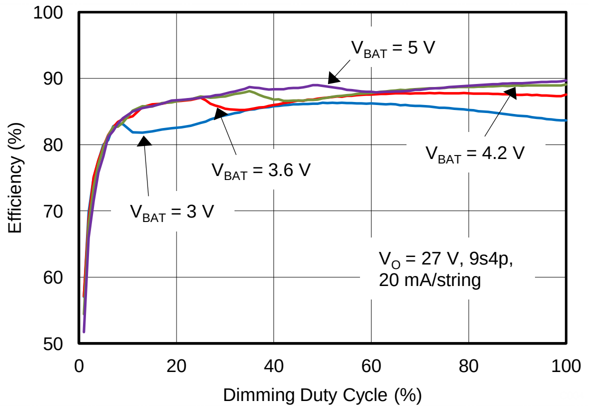


Figure 4. Efficiency vs Dimming Duty Cycle

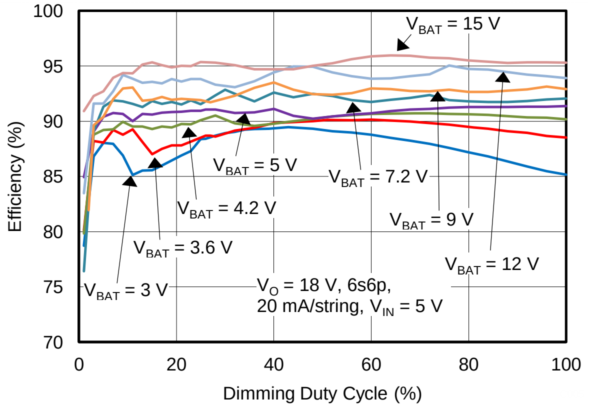


Figure 5. Efficiency vs Dimming Duty Cycle

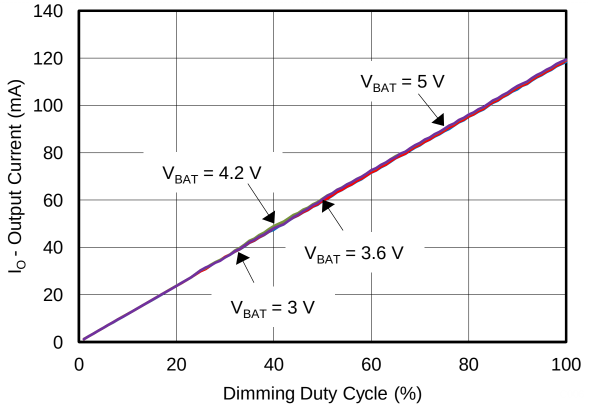


Figure 6. Dimming Linearity

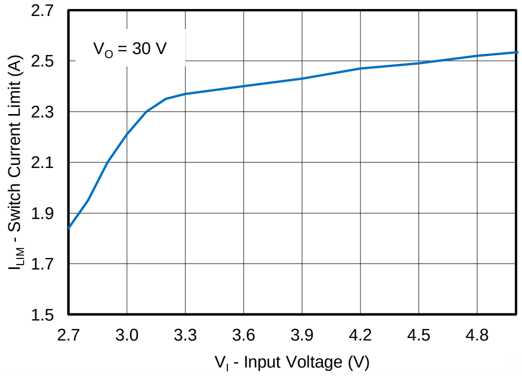


Figure 7. Switch Current Limit vs Input Voltage

7 Detailed Description

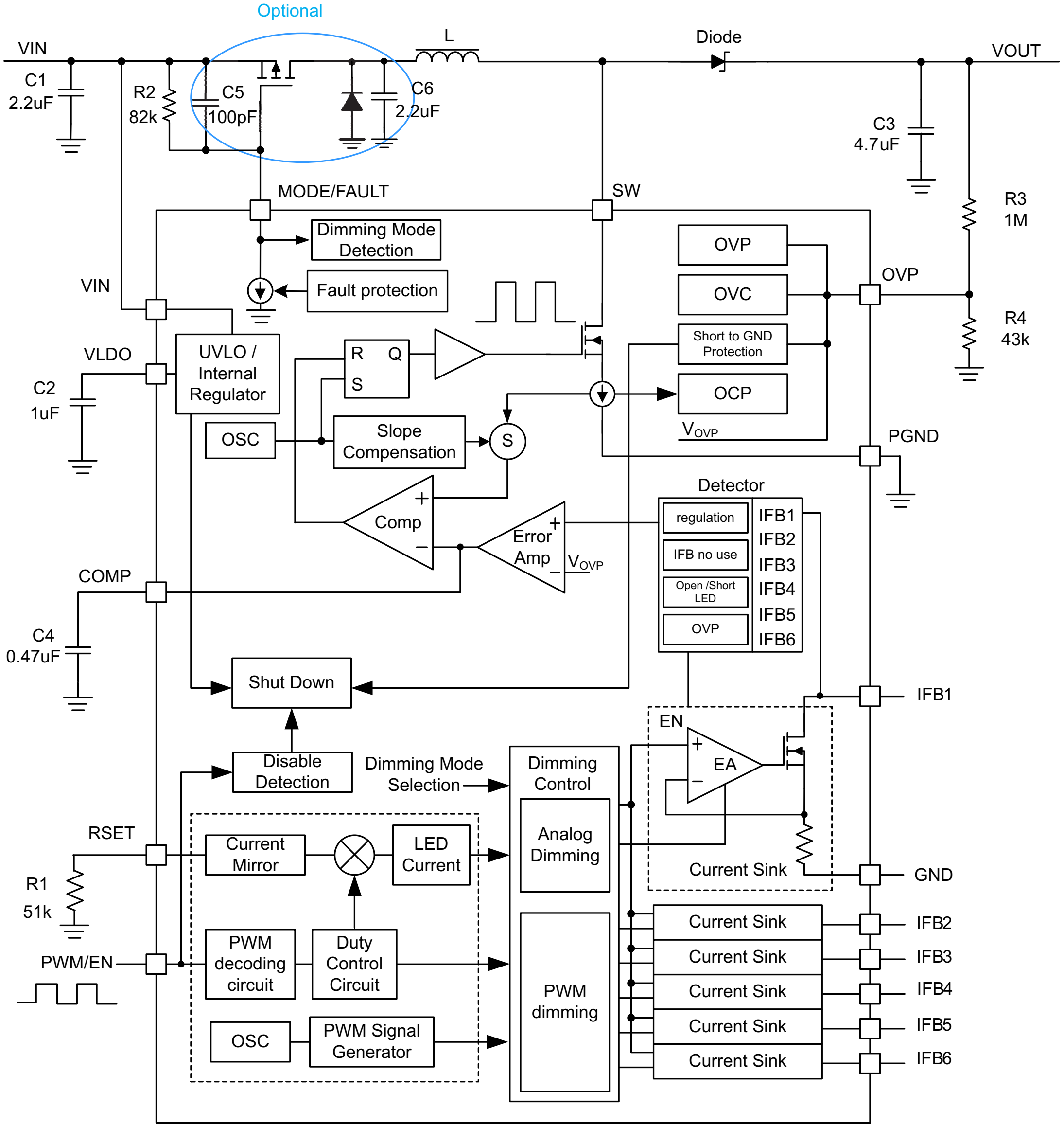
7.1 Overview

The TPS61176 is a high-efficiency, multi-channel WLED driver for tablet and notebook backlighting applications. Because a greater number of WLED diodes are required to provide high brightness backlighting for high resolution panels, the WLED diodes must be arranged in parallel strings. Having more WLED diodes in a string reduces the number of parallel strings and thus improves overall current matching; however, the efficiency of the boost regulator drops due to the high output voltage. Therefore, six current sink regulators of high current matching capability are integrated in the TPS61176 to provide the WLED connection flexibility and to improve the overall power efficiency. The six channels can also be combined as 2 or 3 channels to drive high brightness WLED diodes.

The TPS61176 has integrated all of the key function blocks to power and control up to 60 WLED diodes. The device consists of a boost converter with 2-A, 40-V power MOSFET, six 35-mA current sink regulators and protection circuit for overcurrent, overvoltage, open LED, short LED and output short circuit failures.

The device accepts PWM dimming signal and implements mixed dimming mode. When the dimming duty cycle is high, analog dimming mode works, under which the device controls the DC current of the WLED diodes to realize brightness dimming; when the dimming duty cycle is low, the device switches to PWM dimming mode automatically, so the current of WLED diodes is turned on and off in a high frequency to realize dimming. The automatic switch between analog and PWM dimming modes can leverage the advantages of the two modes: increasing the electrical-to-optical efficiency by analog dimming and avoiding potential color shift issue. The switch point can be programmed to either 25% or 12.5% by the external resistor connected at MODE/FAULT pin.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Supply Voltage

The TPS61176 can support single-cell Li-ion battery input directly. It has a built-in linear regulator to generate supply for internal analog and logic circuits. The VLDO pin, output of the regulator, should be connected to a 1-µF bypass capacitor for the regulator to be controlled in a stable loop. VLDO pin does not have current sourcing capability for external use.

If the device is used in a multi-cell battery system, the battery cannot be connected to VIN pin directly. In this case, connect a 3.3-V or 5-V power rail to bias the VIN pin and connect the battery voltage to the inductor. The VIN pin only consumes less than 3 mA for normal operation. Refer to *Application and Implementation* for more details.

Feature Description (continued)

7.3.2 Boost Converter

The boost converter of the TPS61176 has a fixed switching frequency of 1 MHz and uses current-mode control. A 2-A, 40-V power MOSFET is integrated so the device has a strong output driving capability. A 0.47-µF to 1-µF capacitor should be connected at COMP pin to ensure stable output over the full input and output voltage ranges assuming the recommended inductance and output capacitance values shown in *Recommended Operating Conditions* are used. The COMP pin is very sensitive, so careful layout is required to make sure no noise is coupled to it.

The output voltage of the boost is automatically set by the device to minimize the voltage drop across the IFBx (IFB1 ~ IFB6) pins. Normally the voltage across each WLED string is not same, so the voltages at IFBx pins are different. The device regulates the lowest IFBx voltage to 450 mV, and consistently adjusts the boost output voltage to account for any change of WLED forward voltage drop. If the input voltage is higher than the strings' forward voltage drop (for example, at low duty cycles), the boost converter can’t regulate the output due to its minimum duty-cycle limitation. In this case, increasing the number of WLED diodes in series is helpful to provide enough headroom for the converter to boost the voltage.

7.3.3 Current Sinks

The six current sink regulators embedded in TPS61176 can output up to 35 mA current each. By regulating the current sinks, the TPS61176 controls the current of the WLED strings to realize brightness dimming. The full-scale current per channel is programmed by the resistor at ISET pin according to Equation 1.

$$I_{FBx\_full} = \frac{V_{ISET\_full}}{R_{ISET}} \times K_{ISET}$$

where

- I_{FBx_full}, full-scale current per channel
- K_{ISET} = 1024 (Current multiple)
- V_{ISET_full} = 1.04 V (ISET pin voltage under 100% dimming duty cycle)
- R_{ISET} = ISET pin resistor (1)

7.3.4 IFBx Pin Unused

If fewer than six channels are used, a user can easily disable the unused channel(s) by shorting the corresponding IFBx pin(s) to ground. The TPS61176 detects IFBx pins short status during the start-up process and disables the unused channel(s) before the boost converter starts switching.

7.3.5 Enable and Start-up

The TPS61176 receives a PWM signal at PWM/EN pin to implement the dimming as well as to enable and disable the device. When a PWM signal (high logic or PWM pulse) is input, the device is enabled automatically; when the PWM signal is pulled low for more than 20 ms, the device is disabled and enters into shutdown mode. In shutdown mode, the boost converter stops switching, and the MODE/FAULT pin is internally pulled to VIN to turn off external isolation MOSFET for true shutdown. The input supply current at VIN pin is 4 µA (maximum) in shutdown mode. In order to avoid fault-triggered shutdown during dimming, the PWM dimming signal should have a higher frequency than 100Hz.

Once enabled by PWM input, the TPS61176 enters the start-up process. The internal regulator is enabled first to supply current to internal circuits. Then the device detects the R_{MODE} at MODE/FAULT pin to set the dimming mode. The TPS61176 can detect if the mode resistor is connected between VIN pin and MODE/FAULT pin or connected between MODE/FAULT pin and GND pin. If the mode resistor is detected to be between VIN pin and MODE/FAULT pin, which indicates an external isolation P-channel MOSFET is connected, the MODE/FAULT pin will be pulled down by an internal current sink to turn on the isolation MOSFET after the detection process. The device also checks the status of all IFBx pins (short-to-ground or not) to disable any unused channels. There is no special time sequence requirement of VIN and PWM signals for start-up. If PWM signal is input first, the device starts up when VIN powers up.

Feature Description (continued)

The dimming mode and IFBx status detection process lasts about 4 ms, during which the MODE/FAULT pin outputs a high voltage (V_{IN} – 0.6 V, typical) to keep the isolation MOSFET off. When the 4-ms detection window ends, an internal current sink pulls the MODE/FAULT pin low to turn on the isolation MOSFET. Another 4-ms time window then starts and, at the end of the window, the device detects the OVP pin voltage. If the OVP voltage V_{OVP} is still lower than V_{OVP_SC} ramp-up threshold (90 mV typical), which normally indicates output short-to-ground issue happens, the boost remains off, and the MODE/FAULT pin is pulled up to VIN immediately by an internal resistor to turn off the isolation MOSFET. In this case, the device restarts only after a power-on reset (POR) toggling or PWM toggling. POR toggling means the VIN pin voltage is pulled below UVLO falling threshold first and then pulled above UVLO rising threshold to restart the device; PWM toggling means pulling PWM/EN low for more than 20 ms to disable the device and then apply PWM signal (high logic or PWM pulse) to restart the device. If OVP voltage V_{OVP} is higher than V_{OVP_SC} ramp up threshold, indicating no short to ground issue is detected, boost starts switching to raise the output voltage. Soft start is implemented by gradually ramping up the reference voltage of the error amplifier to prevent voltage overshoot and in-rush current. The capacitor at COMP pin can adjust the soft-start speed. Larger capacitance leads to slower start-up. A 0.47-µF to 1-µF COMP capacitor is recommended.

7.3.6 Brightness Dimming Control

The TPS61176 receives the PWM dimming signal at PWM/EN pin. An internal PWM decoding circuit detects the on time and the period of the PWM signal and calculates the duty cycle information. The device controls the current-sink-regulator output current according to the duty cycle to realize the brightness dimming.

The device supports mixed dimming mode, which leverages the advantages of both analog dimming and PWM dimming modes. When the dimming duty cycle is high, analog-dimming mode is auto-implemented, increasing the electrical-to-optical efficiency and reducing the power budget for the backlight; when the dimming duty cycle is low, PWM dimming mode is auto-implemented, eliminating potential color shift effect which normally happens when the DC current of WLED diode goes low. The switch point between the analog dimming mode and PWM dimming mode can be programmed by the mode resistor connected at MODE/FAULT pin.

The TPS61176 provides four dimming mode options as shown in Table 2. Besides two different switch point options: 25% or 12.5%, the device also offers two different PWM dimming mode options: direct PWM dimming or 22-kHz fixed-frequency PWM dimming. Refer to *Dimming Modes* for the details of different dimming modes.

Different mode resistor values set the different dimming modes. 5% or higher precision resistor should be used for the mode resistor. When an isolation P-channel MOSFET is connected, the mode resistor must be connected between VIN pin and MODE/FAULT pin; when the isolation MOSFET is not connected, the mode resistor should be connected between MODE/FAULT pin and ground. If there is no resistor connected at MODE/FAULT pin, which is only allowed when the isolation MOSFET is not connected, default mode (Mode 1) will be selected. Refer to *Application and Implementation* section for more details.

Table 2. Dimming Mode Setting

MODE	MODE RESISTOR	DIMMING MODE	SWITCH POINT BETWEEN ANALOG AND PWM DIMMING
Mode 1 (Default mode)	1.3 MΩ (5%)	Analog dimming + 22-kHz fixed-frequency PWM dimming	25%
Mode 2	620 kΩ (5%)	Analog dimming + direct PWM dimming	25%
Mode 3	220 kΩ (5%)	Analog dimming + 22-kHz fixed-frequency PWM dimming	12.5%
Mode 4	82 kΩ (5%)	Analog dimming + direct PWM dimming	12.5%

7.4 Device Functional Modes

7.4.1 Dimming Modes

7.4.1.1 Analog Dimming Mode

In analog dimming mode, the brightness dimming is realized by controlling the DC current of WLED diodes. Because the forward voltage of a WLED diode drops when its DC current reduces, the required output voltage can become lower when dimming duty cycle goes low, reducing the power budget for the backlight and allowing more system power saving.

In analog dimming mode, the current of IFBx is regulated according to Equation 2:

$$I_{FBx} = \frac{V_{ISET}}{R_{ISET}} \times K_{ISET} = \frac{V_{ISET\_full}}{R_{ISET}} \times K_{ISET} \times \text{Duty}$$

where

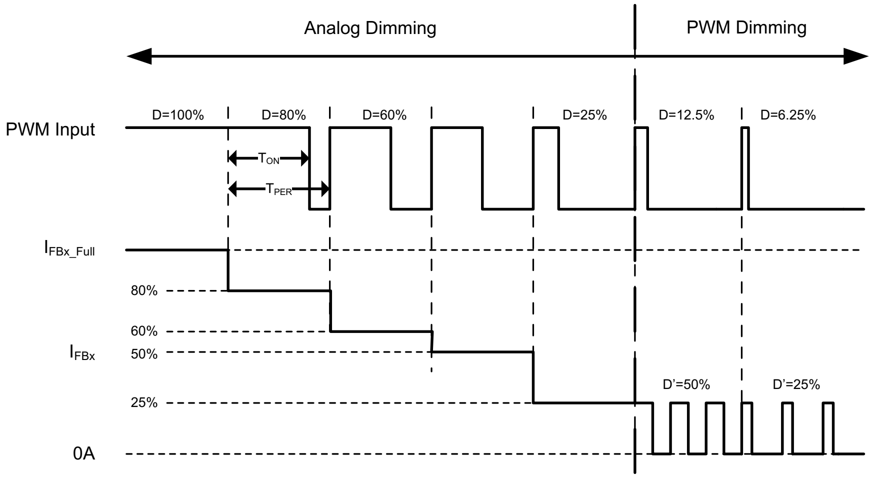
- I_{FBx}, current per string
- V_{ISET}, (ISET pin voltage during analog dimming)
- K_{ISET} = 1024 (Current multiple)
- V_{ISET_full} = 1.04 V (ISET pin voltage with 100% dimming duty cycle)
- R_{ISET} = ISET pin resistor
- Duty = duty cycle of the PWM signal (2)

7.4.1.2 PWM Dimming

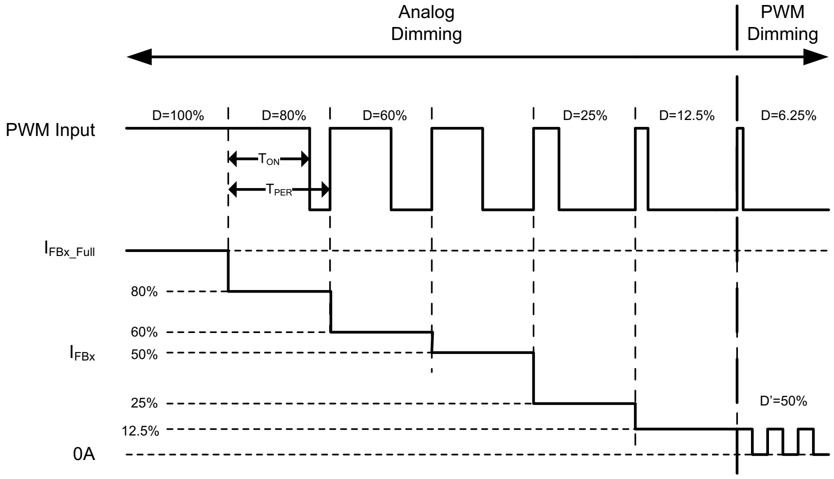
When the dimming duty cycle is below the switch point, PWM dimming mode is automatically implemented. In this mode, the current sink regulators are turned on and off according to the PWM duty cycle information, so the illumination of WLEDs is intermittent. At frequencies higher than a human eye critical flicker frequency, the brightness is the same as the average brightness of the fluctuating light, thus controlling the duty cycle can realize the brightness dimming.

While a current sink regulator is turned on during PWM dimming, its output current is equal to the DC current at the switch point. For example, if the switch point is set to 25%, the regulator's output current during the ON phase is equal to I_{FBx_full} × 25%, and the ON phase's duty cycle Duty' is equal to Duty / 25%, where Duty is the input PWM signal's duty cycle information. Then the average current during PWM dimming can be still equal to I_{FBx_full} × Duty. This design is in order to keep the brightness consistency between analog dimming and PWM dimming and avoid any abrupt brightness change around the switch point. If the switch point is set to 12.5%, the regulator's output current during the ON phase is equal to I_{FBx_full} × 12.5%, and the ON phase duty cycle Duty is equal to Duty / 12.5% (see Figure 8).

Device Functional Modes (continued)



(a). Mixed Dimming Mode with switch point = 25%



(b). Mixed Dimming Mode with switch point = 12.5%

Figure 8. Mixed Dimming Mode

Generally, the average current of an LED string in PWM dimming mode is equal to

$$I_{FBx\_PWM} = \frac{V_{ISET\_full}}{R_{ISET}} \times K_{ISET} \times Duty$$

where

- I_{FBx_PWM}, average current per string in PWM dimming mode
- V_{ISET_full} = 1.04V (ISET pin voltage with 100% dimming duty cycle)
- K_{ISET} = 1024 (Current multiple)
- R_{ISET} = ISET pin resistor
- Duty = duty cycle of the PWM signal

(3)

Device Functional Modes (continued)

The frequency of the current sink regulators ON and OFF control depends on which PWM dimming mode is set. The TPS61176 provides two different PWM dimming modes: direct PWM dimming mode and 22-kHz fixed frequency PWM dimming mode.

In direct PWM dimming mode, the current sinks are turned ON and OFF with the same frequency detected from the input PWM signal. The advantage of this mode is the dimming frequency can be adjusted freely. In addition, it is easy to achieve high dimming resolution in direct PWM dimming mode: with lower input PWM frequency, the higher dimming resolution can be detected and output. For example, when the input PWM frequency is 100 Hz, 14-bit resolution can be achieved; when the input PWM frequency is 20 kHz, 9-bit resolution is achieved. So if high resolution is required, 100-Hz or 200-Hz dimming frequency is recommended. The TPS61176 is designed to minimize the AC ripple on the output capacitor during PWM dimming. Careful passive component selection is also crucial to minimize AC ripple on the output capacitor. In order to further avoid the potential audible noise, input PWM frequency out of audible frequency range is recommended. See *Application and Implementation* for more information.

In 22-kHz fixed frequency PWM dimming mode, current sinks are turned on and off according to the duty cycle information detected from the input PWM signal but with an internally fixed frequency. This mode facilitates the application where the input PWM signal frequency cannot be adjusted outside the audio frequency range. Thus in this mode the audible noise is eliminated completely.

The human eye is much more sensitive to the brightness change at low brightness compared to at high brightness, so in order to improve the visual experience and avoid any potential flickering perception, high-resolution dimming is implemented in PWM dimming mode. The TPS61176 can achieve up to 14-bit dimming resolution during the PWM dimming. Generally, higher resolution can be achieved with lower input PWM frequency. Refer to Table 3 for detailed dimming resolution information.

Table 3. Dimming Resolution Information in PWM Dimming Mode

DIMMING MODE	INPUT PWM FREQUENCY	DIMMING RESOLUTION IN PWM DIMMING MODE
Mode 1	100 Hz ~ 4.5 kHz	12-bit
	4.5 kHz ~ 9 Hz	11-bit
	9 kHz ~ 18 kHz	10-bit
	18 kHz ~ 20 kHz	9-bit
Mode 2	100 Hz ~ 1 kHz	14-bit
	1 kHz ~2 kHz	13-bit
	2 kHz ~ 4 kHz	12- bit
	4 kHz ~ 8 kHz	11-bit
	8 kHz ~ 16 kHz	10-bit
	16 kHz ~ 20 kHz	9 -bit
Mode 3	100 Hz ~ 5 kHz	12-bit
	5 kHz ~ 10 kHz	11-bit
	10 kHz ~ 20 kHz	10-bit
Mode 4	100 Hz ~ 1.2 kHz	14-bit
	1.2 kHz ~2.4 kHz	13-bit
	2.4 kHz ~ 4.8 kHz	12- bit
	4.8 kHz ~ 9.6 kHz	11-bit
	9.6k Hz ~ 20 kHz	10-bit

7.4.2 Overvoltage Protection

The output voltage of the boost converter is detected by the OVP pin. The overvoltage-protection threshold can be programmed by an external resistor divider (R3 and R4 in the *Typical Application*), allowing the usage of low voltage-rating Schottky diode in a low output-voltage application. The correct divider ratio is important for optimum operation of the device. Use the following guidelines to choose the divider value. It can be noise sensitive if R_{upper} and R_{down} have high impedance. Careful layout is required. Also, choose lower resistance values for R_{upper} and R_{down} when power dissipation allows.

Step 1. Determine the maximum output voltage, V_{OUT}, for the system according to the number of series WLEDs.

Step 2. Select R_{upper} resistor value (1 MΩ for a typical application; a lower value such as 100 kΩ for a noisy environment).

Step 3. Calculate R_{down} by using Equation 4.

$$V_{OUT} = \left(\frac{R_{upper}}{R_{down}} + 1 \right) \times V_{OVP\_clamp}$$

where

- $V_{OVP\_clamp} = 1.5\ V$ (4)

When the overvoltage threshold V_{OVP_clamp} is reached, the TPS61176 detects if there are any LED strings open, first by sensing whether there is current on IFBx pin. If any string is open, the corresponding current sink is disabled and removed from regulation. Subsequently, the output voltage drops down and is regulated to a voltage for the connected WLED strings. The IFBx current of the connected WLED strings keeps in regulation during the whole transition. If an open string is reconnected again, a POR toggling or PWM toggling is required to reactivate a previously deactivated string. The TPS61176 shuts down and keeps off when it detects that all of the WLED strings are open. In this case, a POR toggling or PWM toggling is required to restart the device. If there isn't any string open, the TPS61176 regulates the boost output at the over-voltage threshold.

If the output voltage cannot be regulated at the value set by Equation 4 and keeps rising, once the OVP pin voltage exceeds V_{OVP_sd} rising threshold (1.6 V typical), the boost stops switching. When the OVP voltage falls below V_{OVP_sd} falling threshold (1.55 V typical), the boost recovers to switch. During the process, the IFBx current of the connected WLED strings keeps in regulation.

7.4.3 Current Sink Open Protection

If any IFBx pin voltage exceeds the 1st level IFB overvoltage threshold (8.5 V typical) when its current sink is turned on, the TPS61176 turns off this current sink and removes it from output regulation loop. The current regulation of the remaining IFBx pins is not affected. This situation often occurs when there are several shorted WLED diodes in one string. WLED mismatch typically does not create such large voltage difference among WLED strings. The TPS61176 shuts down when it detects that all of the IFBx pin voltages exceed the threshold. In this case, a POR toggling or PWM toggling is required to restart the device.

If any IFBx pin voltage exceeds the 2nd level IFB overvoltage threshold (18 V typical), no matter whether the current sink is turned on or off, the TPS61176 shuts down immediately to avoid potential over stress damage at IFBx pin. A POR toggling or PWM toggling is required to restart the device.

7.4.4 Overcurrent and Short Circuit Protection

The TPS61176 has a pulse-by-pulse overcurrent limit of 2 A (minimum). The boost power MOSFET is turned off when the inductor current reaches this current limit threshold, and it remains off until the beginning of the next switching cycle. This protects the device and external component under overload conditions.

Under severe overload or short-circuit conditions, if the OVP pin voltage is detected below V_{OVP_SC} ramp-down threshold (70 mV typical), The TPS61176 shuts down, and the MODE/FAULT pin is pulled to VIN by an internal switch immediately. As a result, the external isolation MOSFET can be turned off at once, cutting off the power path from input to output. The device restarts after a POR toggling or PWM toggling.

7.4.5 Thermal Protection

An internal thermal shutdown turns off the device when the typical junction temperature of 160°C is exceeded. The device is released from shutdown automatically when the junction temperature decreases by 15°C.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS61176 provides a high-performance LED lighting solution for tablets, notebooks and other low power LCD backlit displays. The device can drive 6 strings of 10 series LEDs in a compact and high efficient solution. The boost voltage can be set with a resistor divider on the OVP pin. The LED current is controlled via a logic level PWM input and the LED current level is set using an I_{SET} resistor. Boost compensation can be adjusted using a capacitor on the COMP pin.

8.2 Typical Application

8.2.1 Single-Cell Battery Input Application

TPS61176's VIN pin voltage range is from 2.7 V to 6.5 V, so it can support single-cell battery input directly. If isolation MOSFET is connected, the mode resistor must be connected between VIN pin and MODE/FAULT pin as shown in Figure 9; if isolation MOSFET is not connected, the mode resistor can be connected between VIN pin and GND as shown in Figure 10. If there is no resistor connected at MODE/FAULT pin, which is only allowed when the isolation MOSFET is not connected, default mode (Mode 1) will be selected.

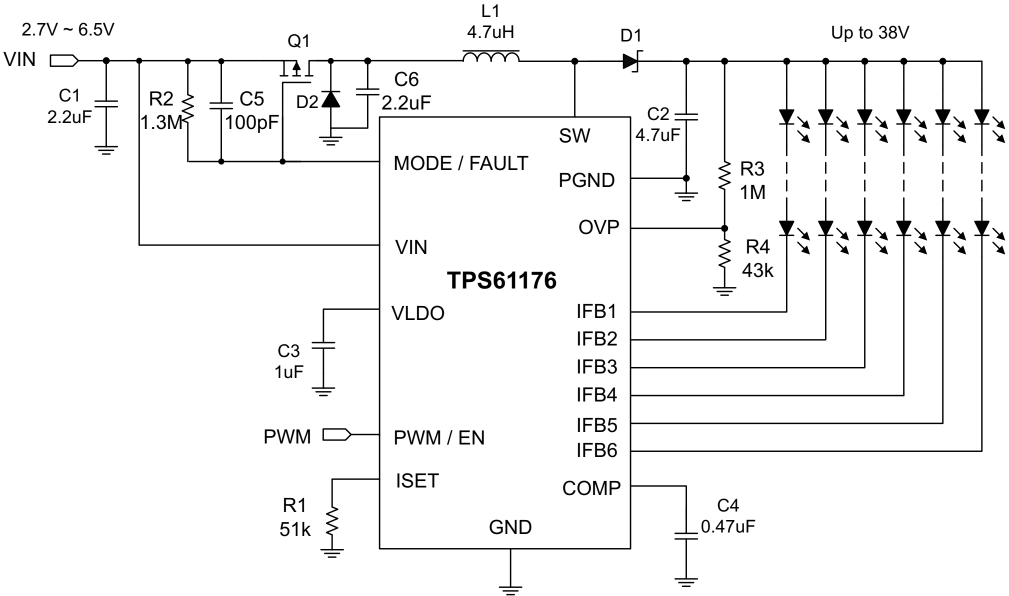


Figure 9. Typical Applications (Single-Cell Battery Input Application)

Typical Application (continued)

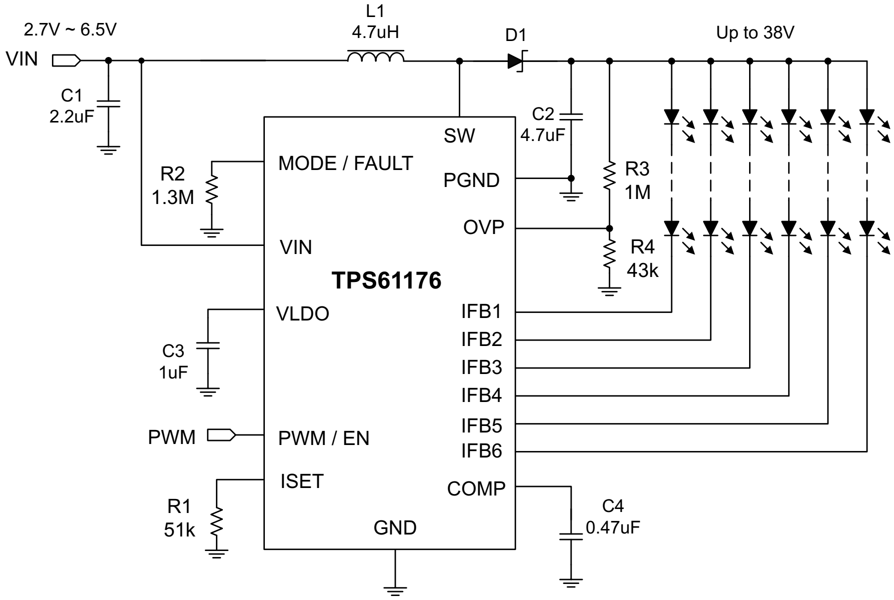


Figure 10. Typical Application (Single-Cell Battery Input Without Isolation MOSFET Application)

8.2.1.1 *Design Requirements*

For TPS61176 typical applications, use the parameters listed in Table 4 as input parameters.

Table 4. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Minimum input voltage	2.7 V
Output voltage	Up to 38 V
Number of series LED	up to 8
Switching frequency	1 MHz, typical
LED current	Up to 35 mA

8.2.1.2 *Detailed Design Procedure*

8.2.1.2.1 Inductor Selection

Because the selection of the inductor affects the power supply steady-state operation, transient behavior, loop stability, and the boost converter efficiency, the inductor is the most important component in switching power regulator design. There are three specifications most important to the performance of the inductor: inductance value, DC resistance and saturation current. TPS61176 is designed to work with inductor values between 4.7 µH and 10 µH. A 4.7-µH inductor is typically available in a smaller or lower profile package, while a 10-µH inductor produces lower inductor ripple. If the boost output current is limited by the overcurrent protection of the device, using a 10-µH inductor can maximize the controller output current capability.

In a boost regulator, the inductor DC current can be calculated as Equation 5.

$$I_{DC} = \frac{Vout \times Iout}{Vin \times \eta}$$

where

- Vout = boost output voltage
- Iout = boost output current
- Vin = boost input voltage

- η = power conversion efficiency, use 85% for TPS61176 normal applications (5)

The inductor current peak-to-peak ripple can be calculated as Equation 6.

$$I_{PP} = \frac{1}{L \times \left(\frac{1}{Vout - Vin} + \frac{1}{Vin} \right) \times F_S}$$

where

- I_{PP} = inductor peak-to-peak ripple
- L = inductor value
- F_S = Switching frequency
- Vout = boost output voltage
- Vin = boost input voltage (6)

Therefore, the peak current seen by the inductor is calculated with Equation 7.

$$I_P = I_{DC} + \frac{I_{PP}}{2} \quad (7)$$

Select the inductor with saturation current over the calculated peak current. To calculate the worse case inductor peak current, use minimum input voltage, maximum output voltage and maximum load current.

Converter efficiency is dependent on the resistance of its high current path and switching losses associated with the internal switch and external power diode. Although the TPS61176 has optimized the internal switch resistance, the overall efficiency is affected by the inductor's DC resistance (DCR). Lower DCR improves efficiency. However, there is a trade-off between DCR and inductor footprint. Furthermore, shielded inductors typically have higher DCR than unshielded ones.

Note that inductor values can have ±20% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the 0-A value depending on how the inductor vendor defines saturation. Table 5 lists the recommended inductors.

Table 5. Recommended Inductors for the TPS61176

PART NUMBER	L (µH)	DCR (mΩ)	I_{SAT} (A)	SIZE (L x W x H mm)	VENDOR
PCMB051H-4R7MS	4.7	78	4.0	5.4 x 5.2 x 1.8	Cyntec
PCMB051H-6R8MS	6.8	107	3.4	5.4 x 5.2 x 1.8	Cyntec
PCMB051H-100MS	10	140	3	5.4 x 5.2 x 1.8	Cyntec
LPS4018-472ML	4.7	125	1.9	4.0 x 4.0 x 1.8	Coilcraft
LPS4018-103ML	10	200	1.3	4.0 x 4.0 x 1.8	Coilcraft
A915AY – 4R7M	4.7	38	1.87	5.2 x 5.2 x 3	TOKO
A915AY – 100M	10	75	1.24	5.2 x 5.2 x 3	TOKO

8.2.1.2.2 Output Capacitor Selection

The output capacitor is mainly selected to meet the requirement for the loop stability and the output ripple. The loop is designed to be stable with an output capacitor within 2.2-µF to 10-µF range. This output ripple is related to the capacitor's capacitance and its equivalent series resistance (ESR). Due to its low ESR, the ripple caused by ESR could be neglected for ceramic capacitors. Assuming a capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated with Equation 8.

$$Cout = \frac{(Vout - Vin) \times Iout}{Vout \times F_S \times Vripple}$$

where

- Vripple = peak-to-peak output ripple. (8)

Note that capacitor degradation increases the ripple much. Select the capacitor which has less degradation at the output voltage. If the output ripple is too large, change a bigger capacitor could be helpful. Normally, X5R ±10% or better capacitors are recommended.

8.2.1.2.3 Schottky Diode Selection

The TPS61176 demands a low forward voltage, high-speed rectification and low capacitance schottky diode for optimum efficiency. Ensure that the diode average and peak current rating exceeds the average output current and peak inductor current. In addition, the diode's reverse breakdown voltage must exceed the open LED protection voltage. Vishay SS2P5, MSS1P4, and NXP PMEG4010EPK are recommended for the TPS61176.

8.2.1.2.4 Isolation FET Selection

The TPS61176 provides a gate driver at MODE/FAULT pin to drive an external P-channel MOSFET which can act as an isolation MOSFET. When the device is disabled or output short to ground issue happens, MODE/FAULT pin can turn off the isolation MOSFET to cut off the power path from the battery to the output. The source of the MOSFET should be connected to the battery input, and an external resistor must be connected between the source and gate of the MOSFET to keep the FET off when the device is disabled. This gate resistor also acts as a mode resistor to select the dimming mode. To turn on the isolation MOSFET, an internal current sink pulls MODE/FAULT pin low. When output short to ground fault happens, an internal switch pulls up the MODE/FAULT pin to VIN, turning off the isolation MOSFET immediately.

When the isolation FET is turned on during start-up, an inrush current will flow through the MOSFET from battery to charge the output capacitor. If the peak current is too large, a capacitor can be connected between the source and the gate of the isolation MOSFET to control the turning on speed (C5 in Figure 9), thus controlling the inrush current. Normally, a 100-pF to 1-nF capacitor is recommended.

During output short to ground protection process, the catch diode (D2 in Figure 9) may be forward biased to provide the continuous current of the inductor when the isolation FET is turned off. In this case, the drain of the isolation FET swings below ground. The voltage across the isolation FET can be momentarily greater than the input voltage. Therefore, select at least 10-V maximum input MOSFET. Adding a capacitor parallel with D2 (refer to Figure 9) could also help reduce the voltage across MOSFET when this failure happens. The ON resistance of the MOSFET has large impact on power conversion efficiency because the MOSFET carries the input current. Select a MOSFET with $R_{ds(on)}$ less than 100 mΩ to limit the power losses. In order to detect larger than 1 M R_{Mode} correctly, the gate leakage of isolation MOSFET should be less than 0.1 µA.

In multi-cell battery input applications, if the isolation MOSFET is connected, the voltage at MODE/FAULT pin may exceed its maximum rating voltage 7 V when the device is disabled or output short to ground issue happens. In order to prevent this over stress damange, isolation MOSFET can't be connected.

8.2.1.2.5 Audible Noise Reduction

Output voltage of the controller also ripples due to the load transient that occurs during PWM dimming. If the PWM dimming frequency is in the audible frequency range, the ripple can produce audible noises on the output ceramic capacitor. There are two ways of reducing or eliminating the audible noise. The first way is to reduce the amount of the output ripple, and therefore minimize the audible noise. The TPS61176 adopts a patented technology to limit this type of output ripple even with the minimum recommended output capacitance. The second way is to select PWM dimming frequency outside the audible frequency range to eliminate the audible noise completely. However, in some applications, the input PWM signal frequency range couldn't be adjusted outside the audible frequency range. To solve this problem, the device provides the 22-kHz fixed frequency PWM dimming mode. In this dimming mode, no matter what the input PWM frequency is, the PWM dimming is implemented at 22 kHz, which is outside the audible frequency range, saving the effort to adjust the input PWM frequency.

8.2.1.3 Application Curves

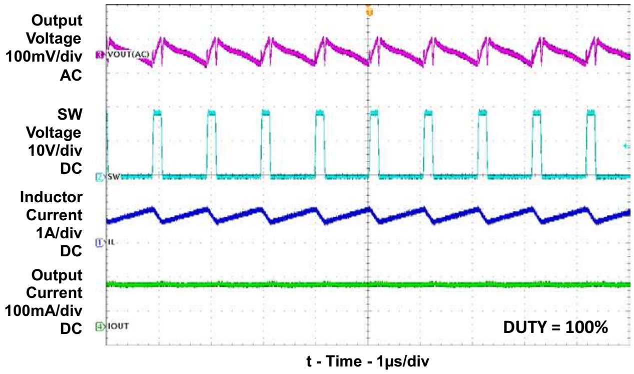


Figure 11. Switching Waveform

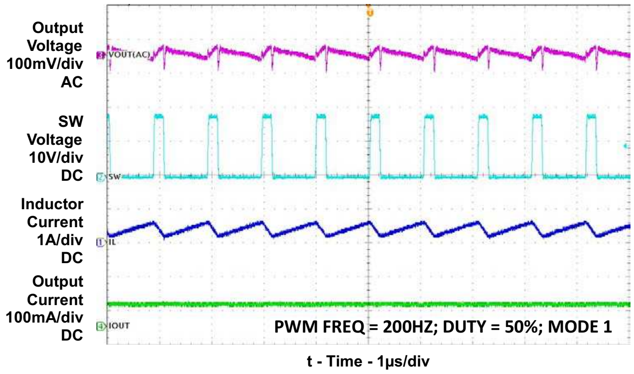


Figure 12. Switching Waveform

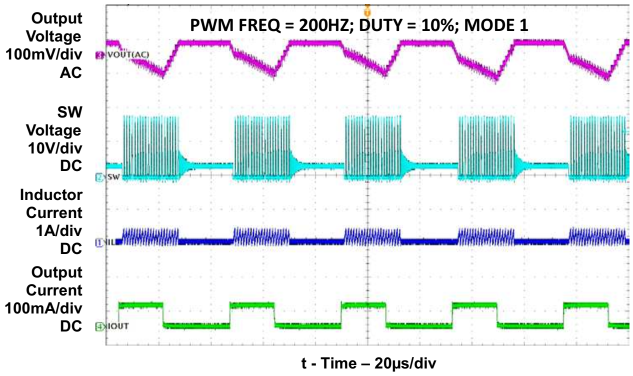


Figure 13. Switching Waveform

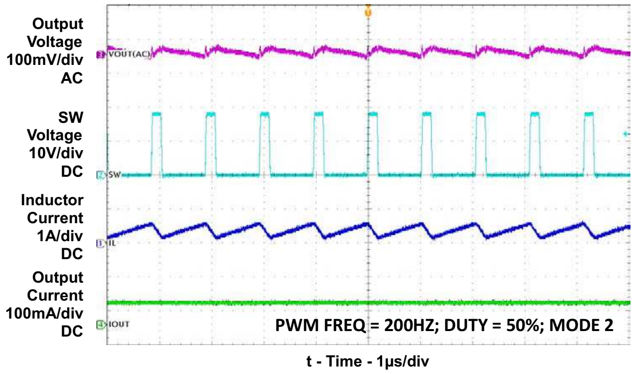


Figure 14. Switching Waveform

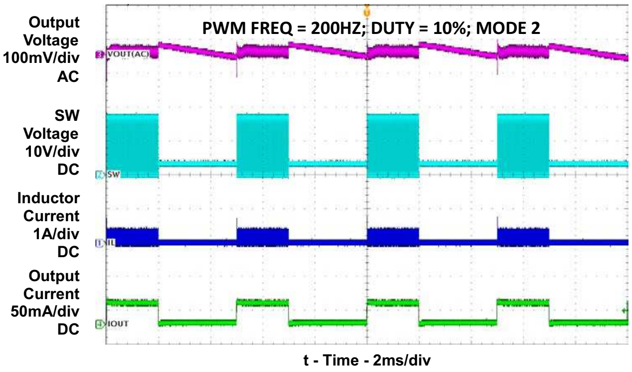


Figure 15. Switching Waveform

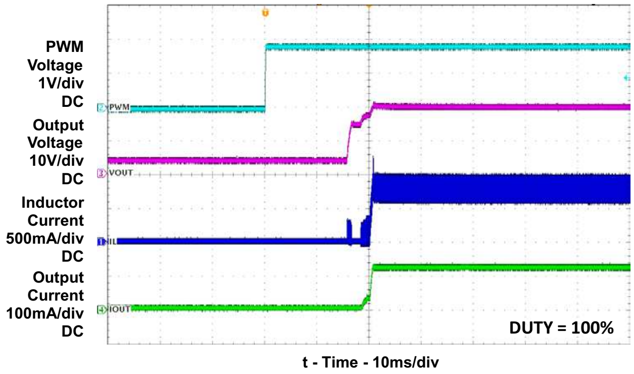


Figure 16. Start-up Waveform

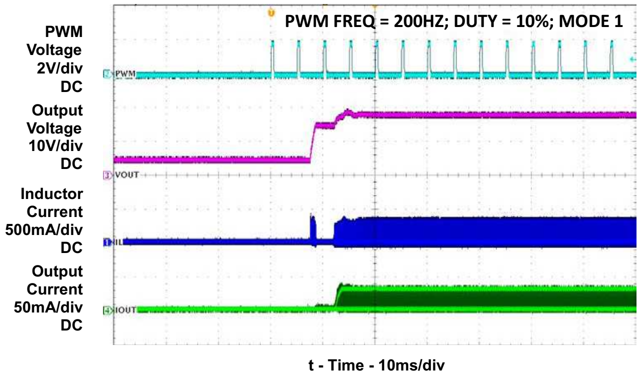


Figure 17. Start-up Waveform

8.2.2 Multi-Cell Battery Input Application

In multi-cell battery input applications, because the normal input voltage is higher than the VIN pin and MODE/FAULT pin’s maximum rating voltage of 7 V, the battery input cannot be connected to VIN pin directly, nor can the isolation MOSFET. A 3.3-V or 5-V bias is required to power the VIN pin of the device with up to 3-mA current consumption, and the mode resistor should be connected between MODE/FAULT pin and ground. Refer to Figure 18.

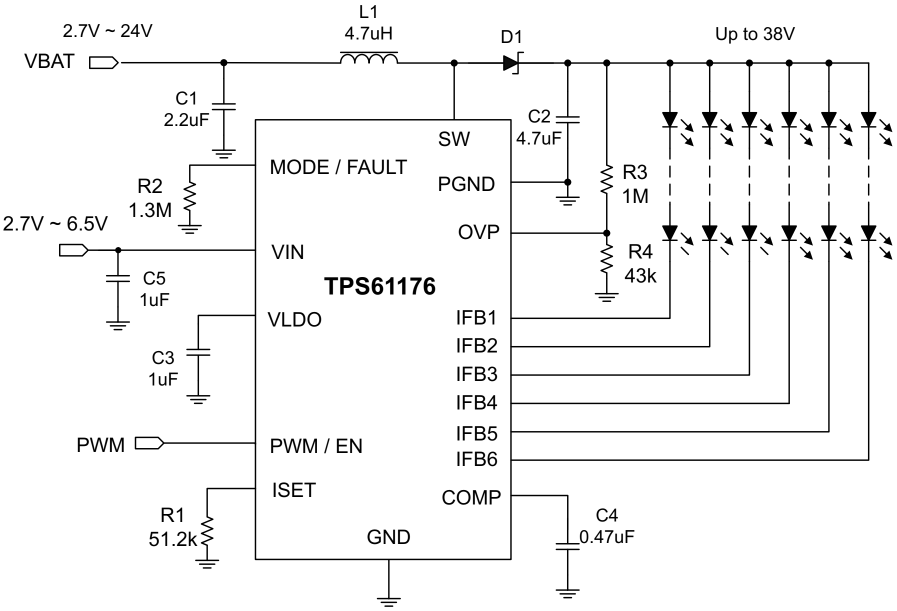


Figure 18. Typical Applications (Multi-Cell Battery Input Application)

8.2.3 Combined String Application

The TPS61176 provides six current sinks with up to 35-mA current capability each. If high brightness WLED diodes are used, the current sinks can be combined as two or three channels to support higher current capability requirement. Refer to Figure 19.

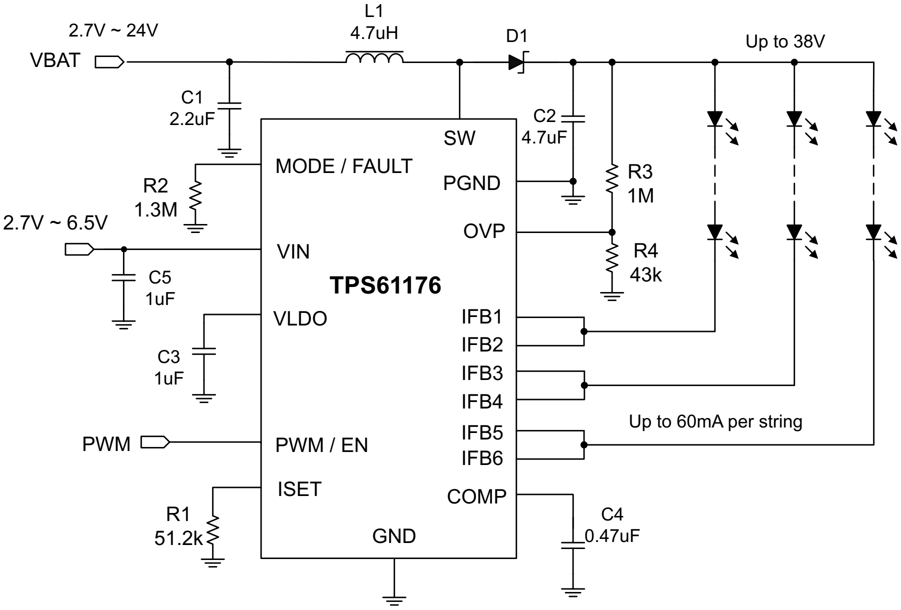


Figure 19. Typical Applications (Combined String to Support High Brightness WLED Diodes)

8.2.4 Separate PWM and EN Signals Application

The TPS61176 can be enabled or disabled automatically according to the PWM signal's status. However, if the user wants to use separate EN and PWM signals to control the driver, the application circuit in Figure 20 or Figure 21 are recommended.

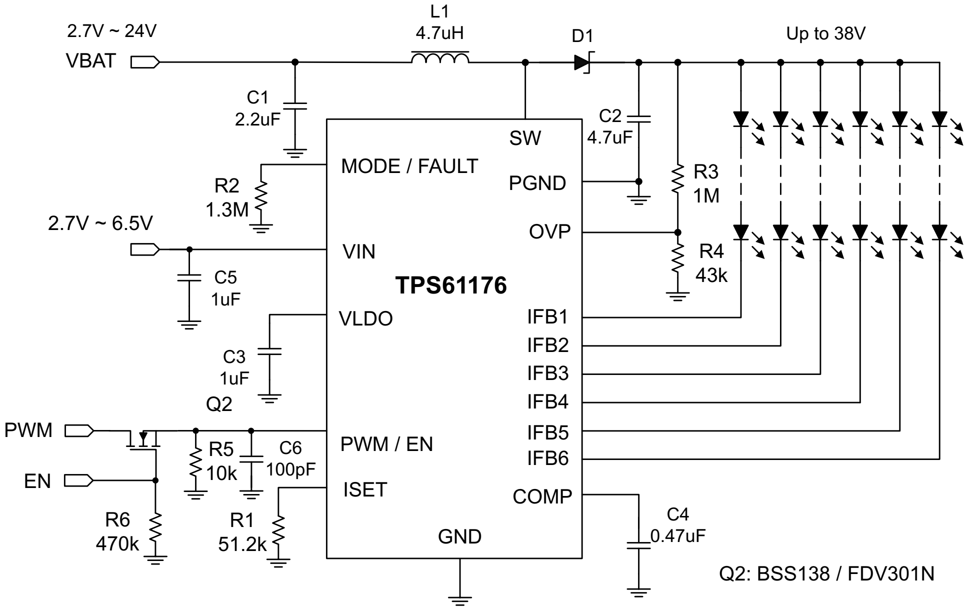


Figure 20. Typical Applications (to Support Separate 3.3-V Logic PWM and EN Signals)

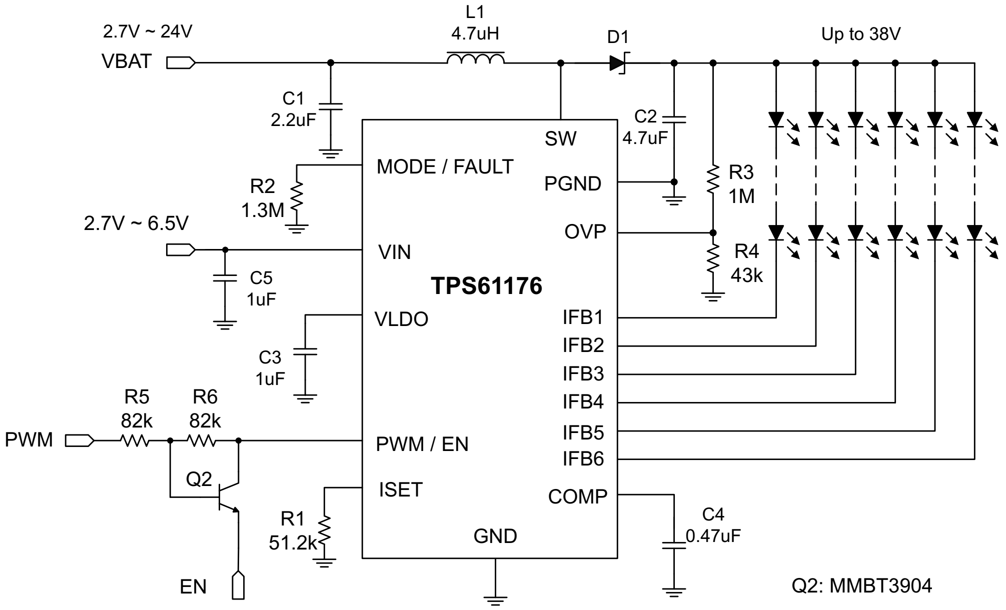


Figure 21. Typical Applications (to Support Separate 1.8-V Logic PWM and EN Signals)

9 Power Supply Recommendations

The TPS61176 device requires a VIN pin supply from 2.7 V to 6.5 V. The boost converter requires a 2.7-V to 24-V supply. The boost input and V_{IN} can be powered from a single supply if it meets the 2.7-V to 6.5-V V_{IN} supply requirement.

10 Layout

10.1 Layout Guidelines

As for all switching power supplies, especially those providing high current and using high switching frequencies, layout is an important design step. If layout is not carefully done, the regulator could show instability as well as EMI problems. Therefore, use wide and short traces for high current paths. The input capacitor, C1 in Figure 9, needs not only to be close to the VIN pin, but also to the GND pin in order to reduce the input ripple seen by the device. It should also be placed close to the inductor. C3 is the filter and noise decoupling capacitor for the internal linear regulator powering the internal digital circuits. It should be placed as close as possible between the VLDO and GND pins to prevent any noise insertion to the digital circuits. The SW pin carries high current with fast rising and falling edges. Therefore, the connection between the SW pin to the inductor and Schottky diode should be kept as short and wide as possible. The trace between the Schottky diode and the output capacitor C2 should also be as short and wide as possible. It is also beneficial to have the ground of the output capacitor C2 close to the PGND pin because there is a large ground return current flowing between them. When laying out signal grounds, it is recommended to use short traces separated from power ground traces, and connect them together at a single point — for example, on the thermal pad. The thermal pad needs to be soldered onto the PCB and connected to the GND pin of the device. An additional thermal via can significantly improve power dissipation of the device.

10.2 Layout Example

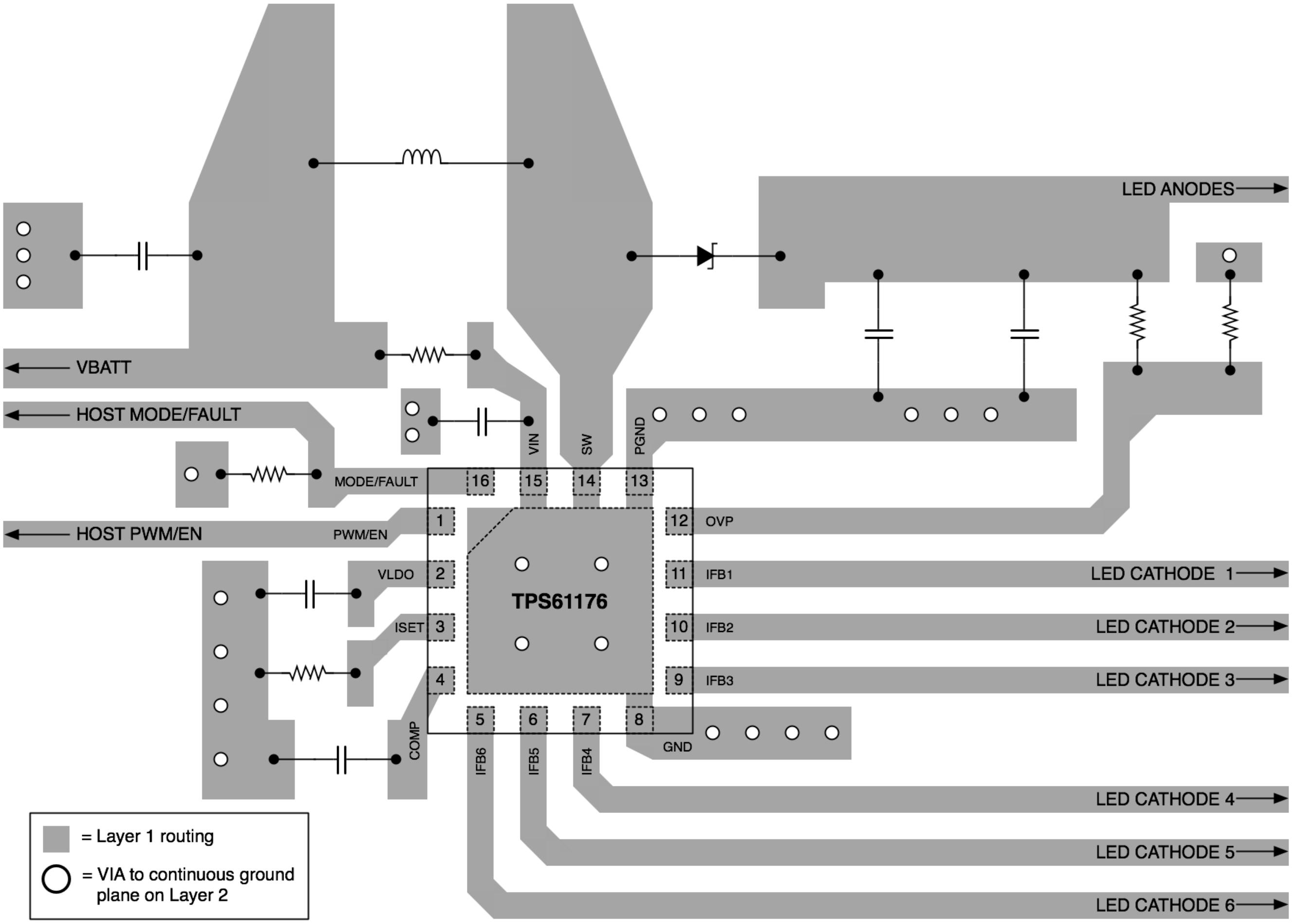


Figure 22. TPS61176 Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61176RTER	ACTIVE	WQFN	RTE	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PZJI	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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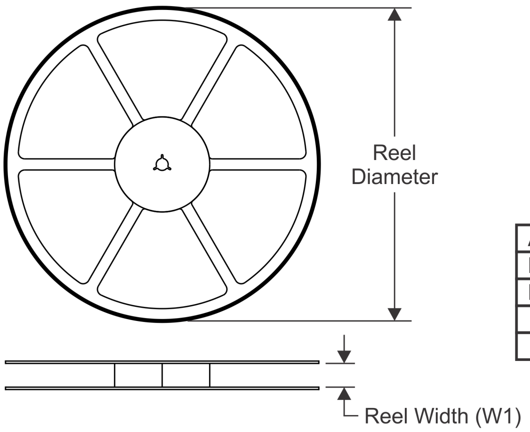
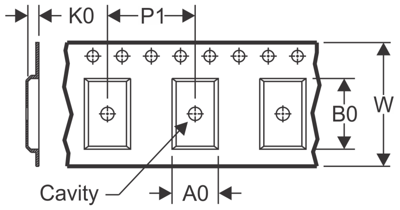
TAPE AND REEL INFORMATION

REEL DIMENSIONS

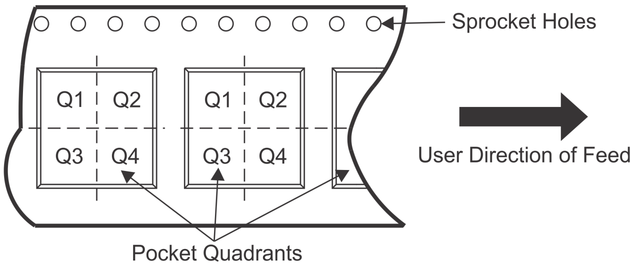


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

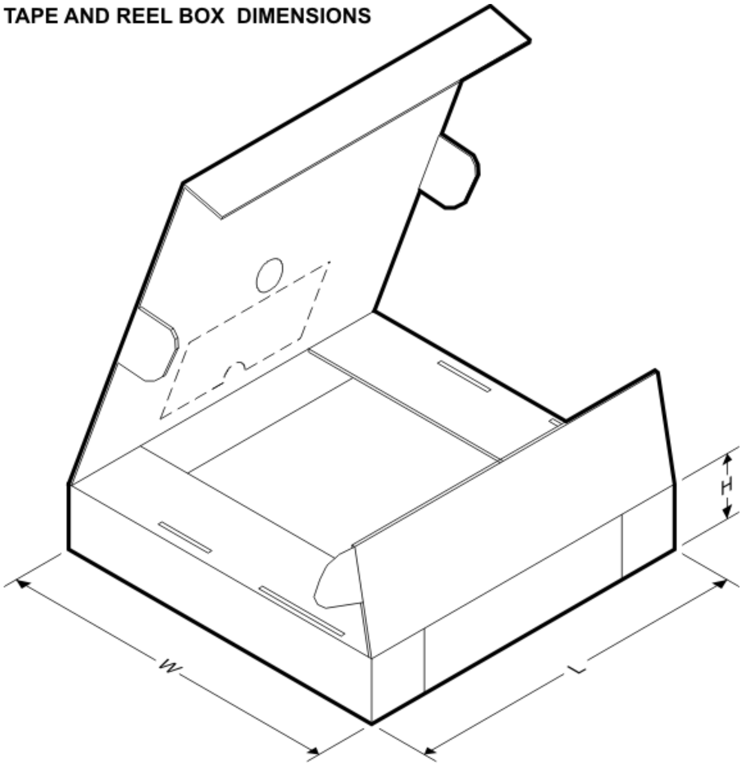
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61176RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

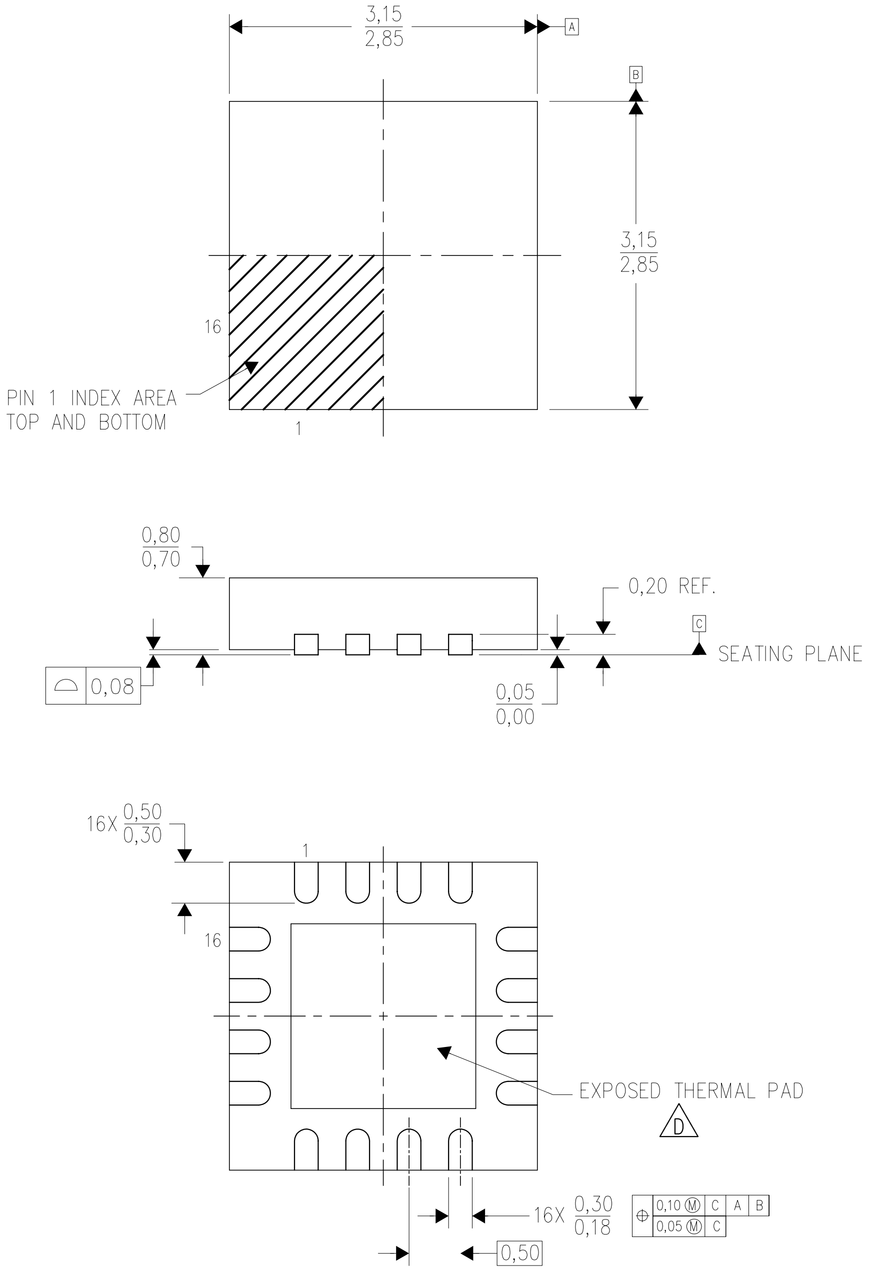
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61176RTER	WQFN	RTE	16	3000	367.0	367.0	35.0

RTE (S-PWQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD



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NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Quad Flatpack, No–leads (QFN) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
- E. Falls within JEDEC MO–220.

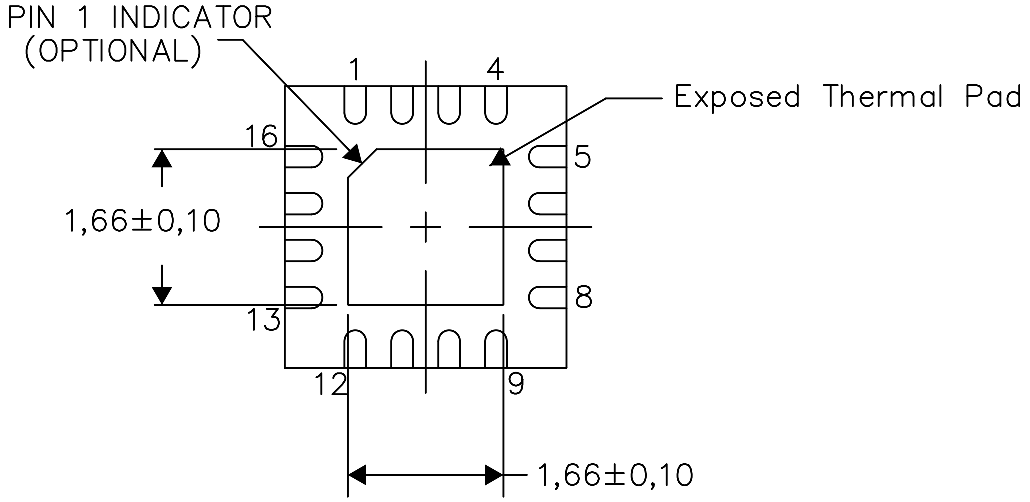
RTE (S-PWQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

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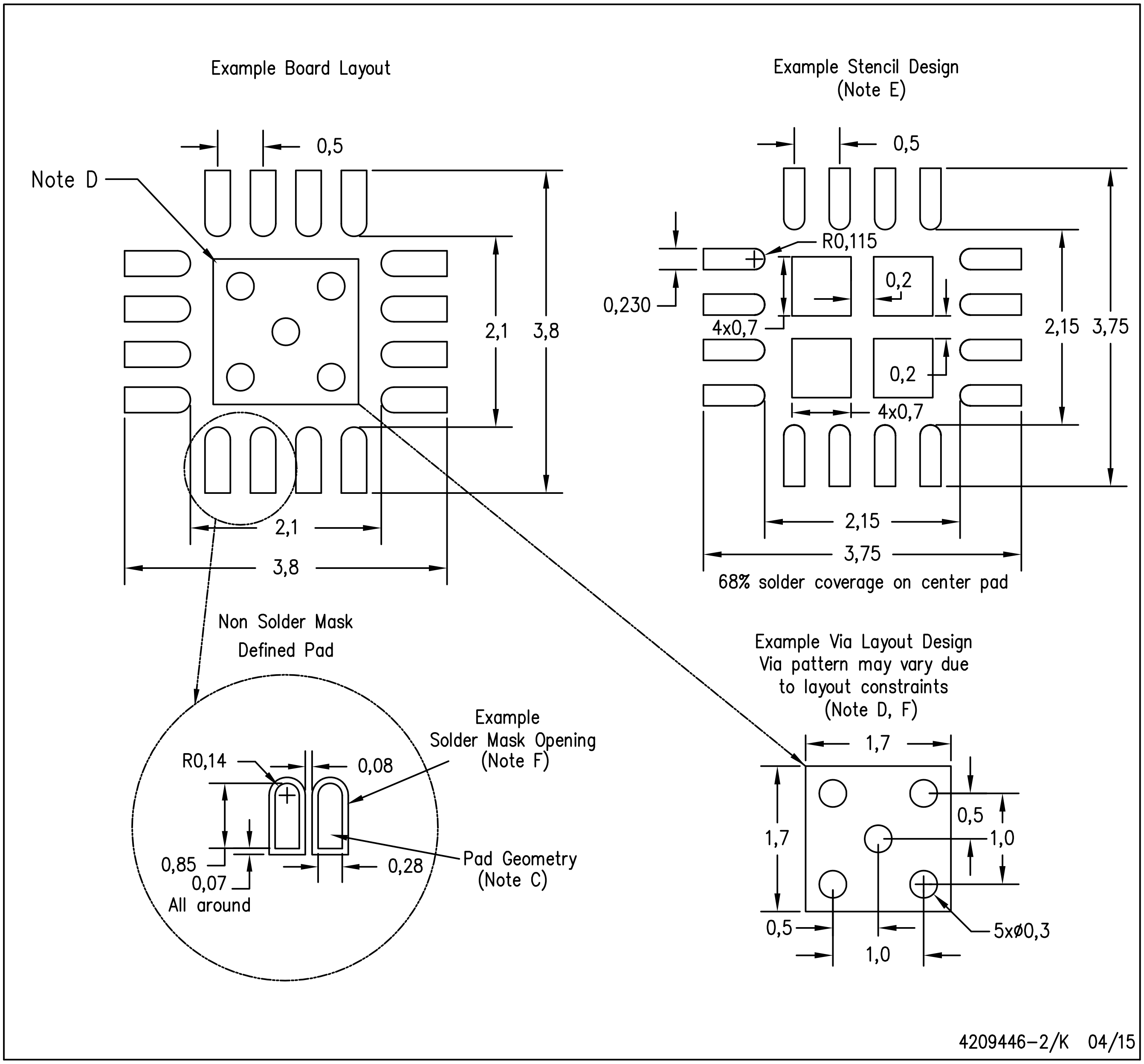
NOTE: A. All linear dimensions are in millimeters

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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