GENERAL DESCRIPTION

OB2362D is a highly integrated current mode PWM control IC optimized for high performance, low standby power and cost effective offline flyback converter applications.

At full loading, the IC operates in fixed frequency (65KHz) mode. When the loading goes low, it operates in Green mode with valley switching for high power conversion efficiency. When the load is very small, the IC operates in 'Extended Burst Mode' to minimize the standby power loss. As a result, high conversion efficiency can be achieved in the whole loading range.

VCC low startup current and low operating current contribute to a reliable power on startup and low standby design with OB2362D.

OB2362D offers comprehensive protection coverage with auto-recovery including Cycle-by-Cycle current limiting (OCP), over load protection (OLP), VCC under voltage lockout (UVLO), over temperature protection (OTP), and over voltage protection (OVP). Excellent EMI performance is achieved with On-Bright proprietary frequency shuffling technique.

The tone energy at below 23KHz is minimized in the design and audio noise is eliminated during operation.

OB2362D is offered in SOT23-6 package.

APPLICATIONS

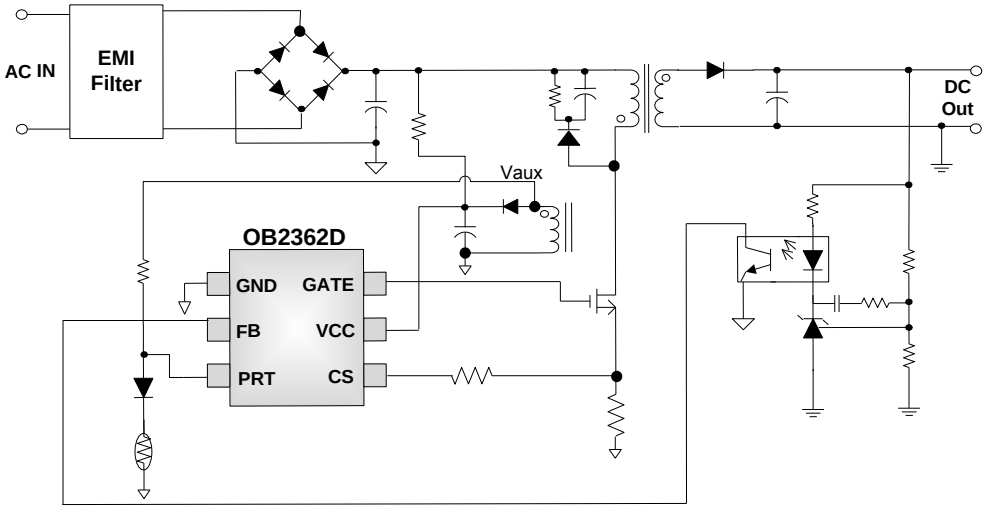
Offline AC/DC flyback converter for

- General power supply
- Power Adapter

FEATURES

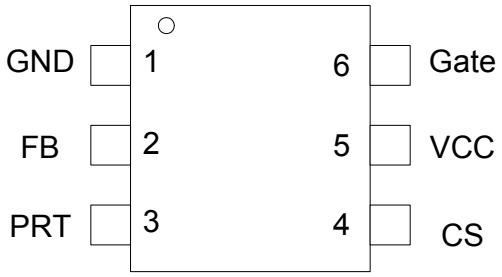
- Power on soft start reducing MOSFET Vds stress
- Multi-Mode Operation:
  130KHz maximum frequency PWM at peak load;
  65KHz fixed frequency PWM at full load;
  Valley switching operation at light to middle load range;
  Burst mode at light load and no load
- Frequency shuffling for EMI
- Extended burst mode control for improved efficiency and low standby power design
- Audio noise free operation
- Comprehensive protection coverage
  - o VCC Under Voltage Lockout with hysteresis (UVLO)
  - o VCC Over Voltage Protection (VCC OVP) with latch shut down.
  - o Internal integrated two level OCP protection
  - o Internal integrated SCP protection
  - o Over Load Protection (OLP)
  - o External (if NTC resistor is connected at RT pin) or internal (if RT pin floating) Over Temperature Protection (OTP) with auto recovery protection.
  - o Output diode short protection with auto recovery protection
  - o Cycle-by-cycle over current threshold setting for constant output power limiting over universal input voltage range
  - o Output Over Voltage Protection(Output OVP) with latched shut down, and the OVP triggered voltage can be adjusted by the resistor connected between auxiliary winding and PRT pin

TYPICAL APPLICATION



GENERAL INFORMATION

Pin Configuration



Ordering Information

Part Number	Description
OB2362DMP	SOT23-6, Pb-free in T&R,

Package Dissipation Rating

Package	RθJA(℃/W)
SOT23-6	200

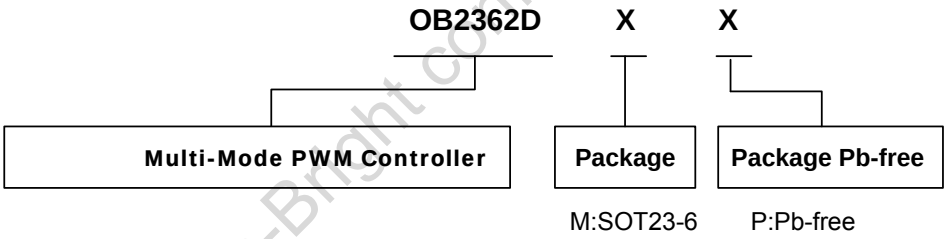
Recommended operating condition

Symbol	Parameter	Range
VCC	VCC Supply Voltage	12 to 26V

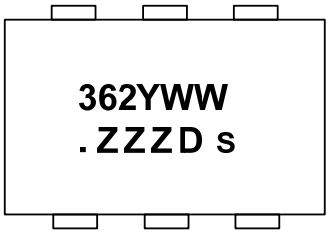
Absolute Maximum Ratings

Parameter	Value
VCC DC Supply Voltage	V_{OVP}-1V
FB Input Voltage	-0.3 to 7V
CS Input Voltage	-0.3 to 7V
PRT Input Voltage	-0.3 to 7V
Min/Max Operating Junction Temperature TJ	-40 to 150 ℃
Operating Ambient Temperature T_A	-40 to 85 ℃
Min/Max Storage Temperature Tstg	-55 to 150 ℃
Lead Temperature (Soldering, 10secs)	260 ℃

Note: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.



Marking Information

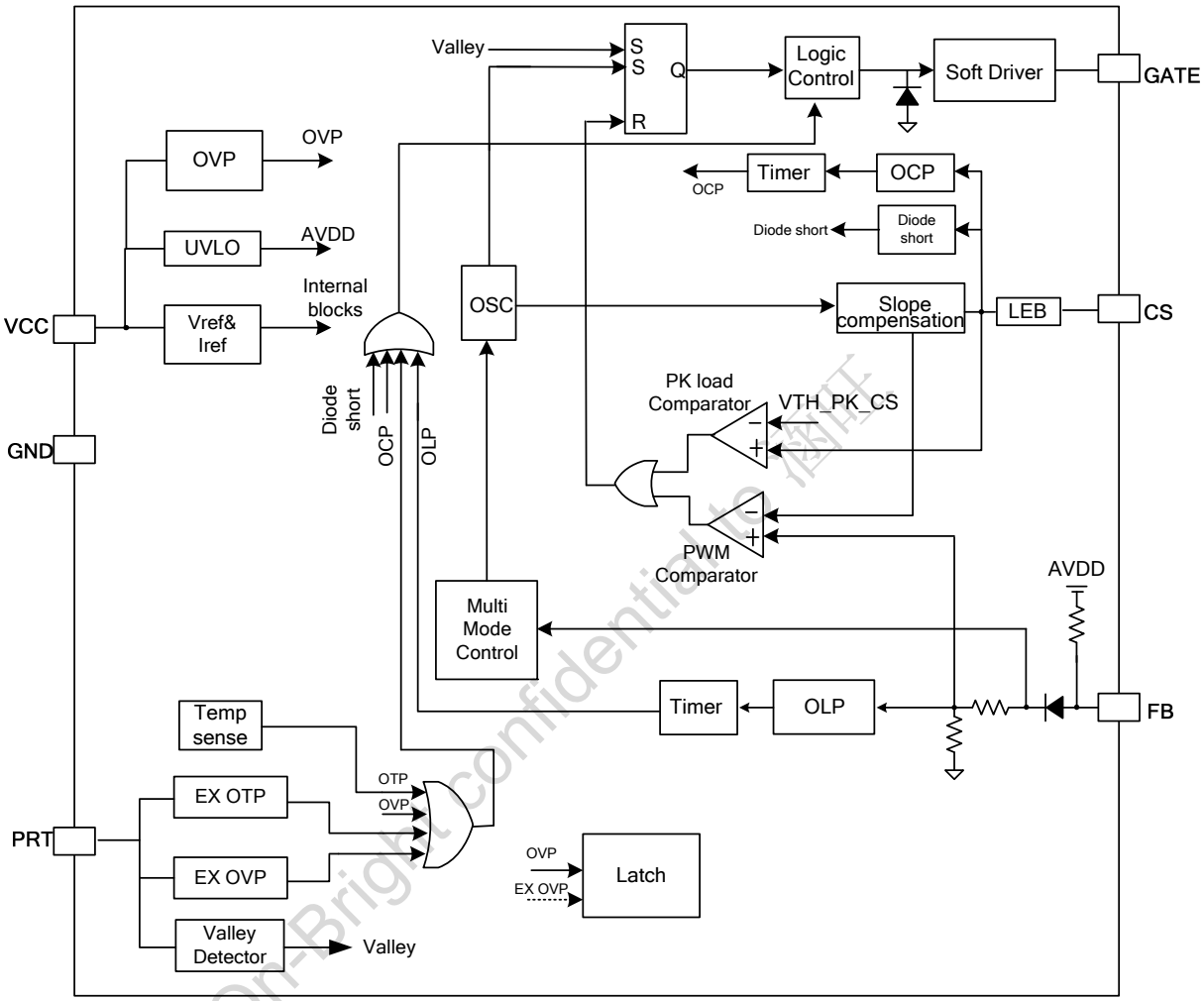


Y:Year Code
WW:Week Code(01-52)
ZZZ:Lot code
D:Character Code
S: Internal code

TERMINAL ASSIGNMENTS

Pin Name	I/O	Description
GND	P	Ground
FB	I	Feedback input pin. The PWM duty cycle is determined by voltage level into this pin and the current-sense signal at Pin CS.
PRT	I	Multiple functions pin. Connecting a NTC resistor to ground for OTP detection. Connecting a resistor from Vaux can adjust OVP trigger voltage and detect transformer core demagnetization. If both OTP and OVP are needed, a diode should be connected between PRT pin and the NTC resistor.
CS	I	Current sense input
VCC	P	Power Supply
GATE	O	Totem-pole gate driver output for power MOSFET

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

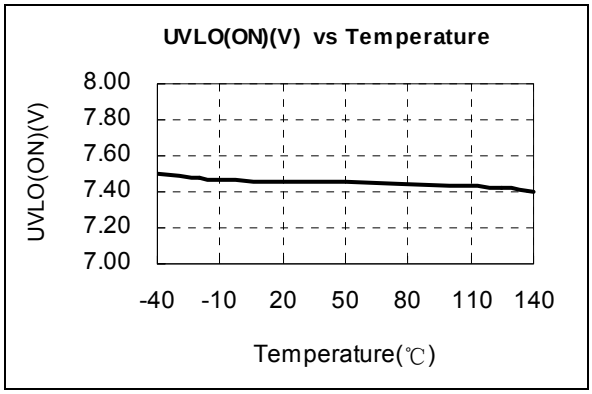
(T_A = 25℃, VCC=18V, unless otherwise noted)

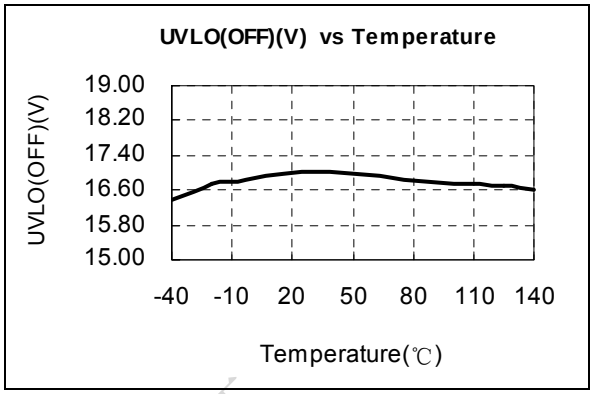
Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
Supply Voltage (VDD)						
Istartup	VCC Start up Current	VCC=UVLO(OFF)-1V, measure leakage current into VCC		2	5	uA
I_VCC_Operation	Operation Current	VDD=18V,CS=4V, FB=3.5V,measure I(VCC)		2.5	3	mA
I_VCC_Burst	Burst Current	CS=0V,FB=0.5V, measure I(VCC)		0.6	0.7	mA
UVLO(ON)	VCC Under Voltage Lockout Enter		7	7.5	8	V
UVLO(OFF)	VCC Under Voltage Lockout Exit (Recovery)		16	17	18	V
Vpull-up	Pull-up PMOS active			10		V
OVP	VCC Over Voltage Protection threshold voltage	FB=3V,CS=0V. Slowly ramp VCC, until no gate switching.	26.5	28	29.5	V
Feedback Input Section(FB Pin)						
V_{FB} Open	V_{FB} Open Loop Voltage			5.1		V
Avcs	PWM input gain ΔVFB/ΔVCS			3.5		V/V
Maximum duty cycle	Max duty cycle @ VCC=18V,VFB=3V,VCS=0V		77	80	83	%
Vref_green	The threshold enter green mode			2.1		V
Vref_burst_H	The threshold exits burst mode			1.33		V
Vref_burst_L	The threshold enters burst mode			1.23		V
I_{FB}_Short	FB pin short circuit current	Short FB pin to GND and measure current		0.21		mA
V_{TH}_PK	Peak load, FB Threshold Voltage			4.4		V
Td_PK	Peak load, Debounce Time		13.5	15	18.5	ms
Z_{FB}_IN	Input Impedance			30		KΩ
Current Sense Input(CS Pin)						
SST_CS	Soft start time for CS peak			2		ms
T_blanking	Leading edge blanking time			300		ns
Td_OC	Over Current Detection and Control Delay	From Over Current Occurs till the Gate driver output start to turn off		90		ns
V_{TH}_OC	Internal Current Limiting Threshold Voltage with zero duty cycle		0.43	0.45	0.47	V
V_{TH}_OC_Clamp	OCP CS voltage clamper			0.6		V
Td_OLP	Over load, debounce Time		11.5	13	15.5	s
V_{TH}_PK_CS	Internal Current Limiting Threshold Voltage with zero duty cycle for PK load			0.55		V

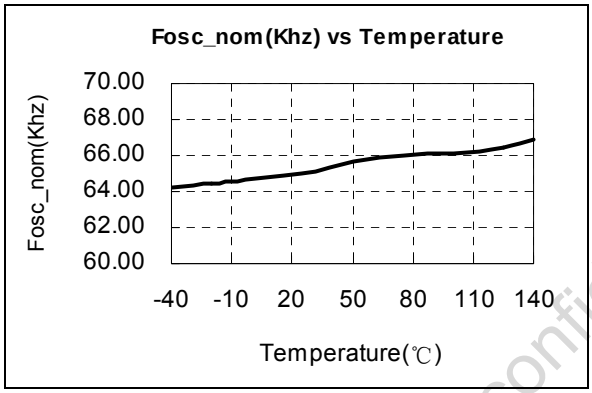
V_{TH}_PK_ CS_Clamp	PK load CS voltage clamper			0.87		V
PRT pin						
IRT	Output current for external OTP detection		94	100	106	uA
VOTP	Threshold voltage for external OTP		0.95	1	1.05	V
Ioutput_ovp	Current threshold for adjustable output OVP		170	180	190	uA
Td_output_ovp	Output OVP debounce time			5		Cycles
In-chip OTP						
OTP enter				150		℃
OTP exit				120		℃
Oscillator						
F_{OSC}	Normal Oscillation Frequency	VDD=18V,FB=3V, CS=0V	60	65	70	KHz
Fosc_PK	Peak load frequency (Duty>47%)	VDD=18V,FB=4.5V, CS=0V		130		KHz
∆f_OSC	Frequency jittering	VDD=18V,FB=3V, CS=0V		+/-6		%
F_shuffling	Shuffling frequency			32		Hz
∆f_Temp	Frequency Temperature Stability			1		%
∆f_VCC	Frequency Voltage Stability			1		%
F_Burst	Burst Mode Switch Frequency			23		KHz
Gate driver						
VOL	Output low level @ VDD=18V, Io=5mA				1	V
VOH	Output high level @ VCC=18V, Io=20mA		6			V
V_clamping	Output clamp voltage			11		V
T_r	Output rising time 1.2V ~ 10.8V @ CL=1000pF			100		ns
T_f	Output falling time 10.8V ~ 1.2V @ CL=1000pF			30		ns

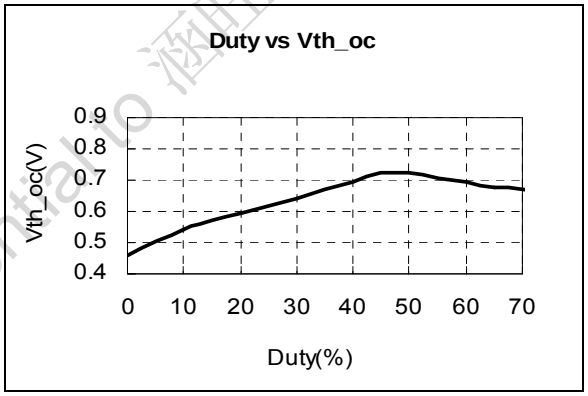
CHARACTERIZATION PLOTS

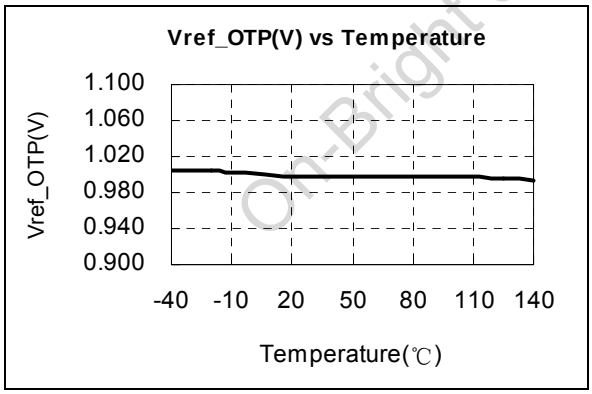
VDD = 18V, TA = 25℃ condition applies if not otherwise noted.

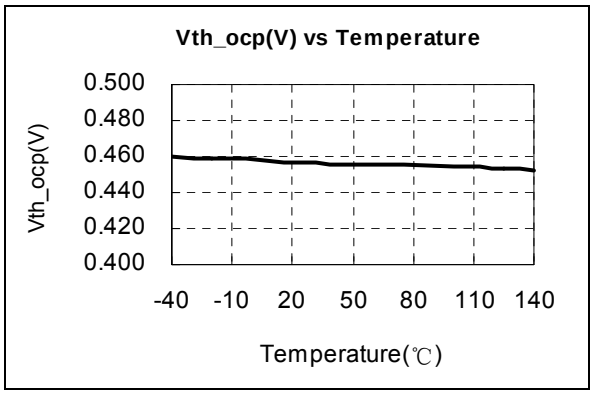


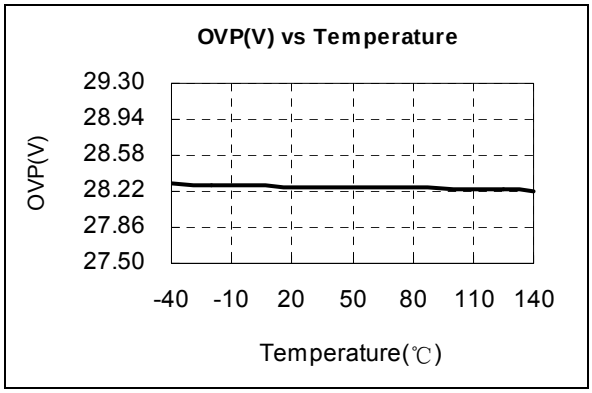


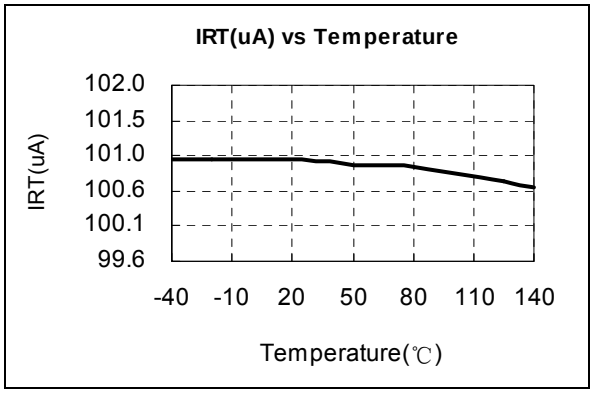












OPERATION DESCRIPTION

OB2362D is a highly integrated current mode PWM control IC optimized for high performance, low standby power and cost effective offline flyback converter applications. The 'extended burst mode' control greatly reduces the standby power consumption and helps the design easier to meet the international power conservation requirements.

Startup Current and Start up Control

Startup current of OB236D is designed to be very low so that VCC could be charged up above UVLO threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet achieve a reliable startup in application.

Operating Current

The Operating current of OB2362D is low at 2.5mA (typical). Good efficiency is achieved with OB2362D low operation current together with the 'extended burst mode' control features.

Soft Start

OB2362D features an internal 2ms (typical) soft start to soften the electrical stress occurring in the power supply during startup. It is activated during the power on sequence. As soon as VCC reaches UVLO(OFF), the CS peak voltage is gradually increased from 0.05V to the maximum level. Every restart up is followed by a soft start.

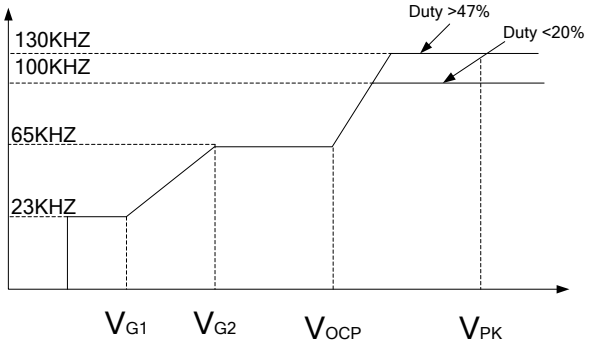
Frequency shuffling for EMI improvement

The frequency shuffling (switching frequency modulation) is implemented in OB2362D. The oscillation frequency is modulated so that the tone energy is spread out. The spread spectrum minimizes the conduction band EMI and therefore eases the system design.

Multi Mode Operation for High Efficiency

OB2362D is a multi mode controller. The controller changes the mode of operation according to the FB pin voltage.

During the full load power operation, OB2362D operates at a 65KHz (typical) fixed frequency. The efficiency and system cost is controlled at an optimal level. A peak mode is implemented based on On-Bright proprietary technology to supply a peak current output requirement. In peak power mode, frequency is increased from 65KHz (typical) to 130KHz (typical). The maximum frequency is limited to 100KHz when the PWM duty is lower than 20%.



As the output load current is decreased , the IC enter into green mode smoothly from the PWM mode. In this mode , the switching frequency will start to linearly decrease from 65KHz to 23KHz, meanwhile the valley turn on can be realized by monitoring the voltage activity on auxiliary windings through the PRT pin. So the switching loss is minimized and the high conversion efficiency can be achieved.

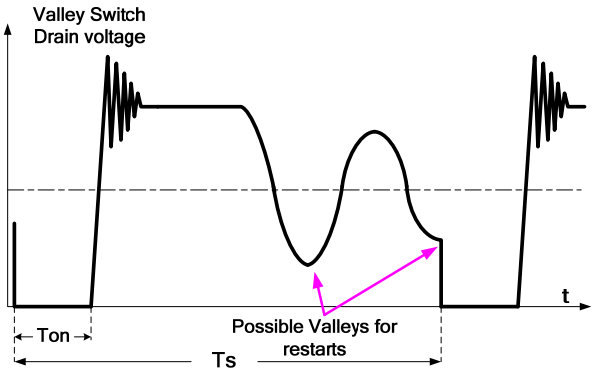
At light load or no load condition, most of the power dissipation in a switching mode power supply is from switching loss of the MOSFET, the core loss of the transformer and the loss of the snubber circuit. The magnitude of power loss is in proportion to the switching frequency. Lower switching frequency leads to the reduction on the power loss and thus conserves the energy.

The switching frequency is internally adjusted at no load or light load condition. The switch frequency reduces at light/no load condition to improve the conversion efficiency. At light load or no load condition, the FB input drops below Vref_burst_L (the threshold enter burst mode) and device enters Burst Mode control. The Gate drive output switches when FB input rises back to Vref_burst_H (the threshold exit burst mode). Otherwise the gate drive remains at off state to minimize the switching loss and reduces the standby power consumption to the greatest extend.

Demagnetization Detection

The transformer core demagnetization is detected by monitoring the voltage activity on the auxiliary windings through PRT pin. This voltage features a flyback polarity. After the on time (determined by the CS voltage and FB voltage), the switch is off and the flyback stroke starts. After the flyback stroke, the drain voltage shows an oscillation with a frequency of approximately $1/2\pi\sqrt{L_p C_d}$, where L_p is the primary self inductance of primary winding of the transformer and C_d is the capacitance on the drain node.

The typical detection level is fixed at -50mV at the PRT pin. Demagnetization is recognized by detection of a possible "valley" when the voltage at PRT is below -50mV in falling edge.



Current Sensing and Leading Edge Blanking

Cycle-by-Cycle current limiting is offered in OB2362D current mode PWM control. The switch current is detected by a sense resistor into the CS pin. An internal leading edge blanking circuit chops off the sensed voltage spike at initial internal power MOSFET on state due to snubber diode reverse recovery and surge gate current of power MOSFET. The current limiting comparator is disabled and cannot turn off the internal power MOSFET during the blanking period. The PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

Internal Synchronized Slope Compensation

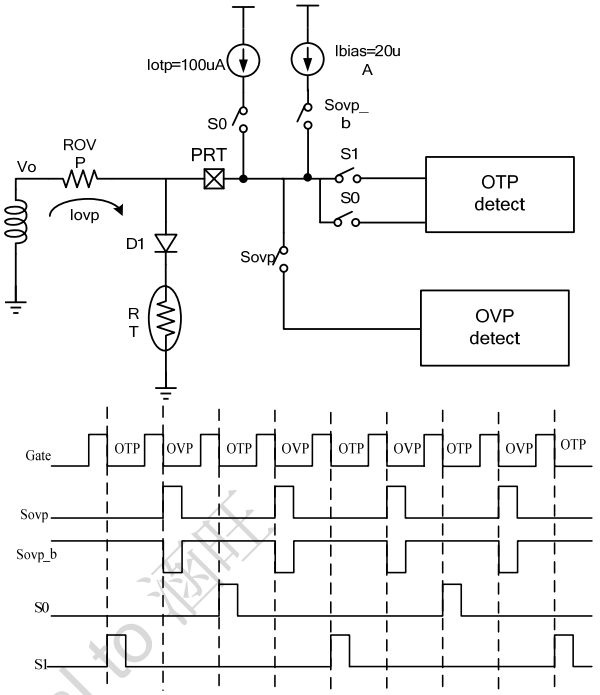
Built-in slope compensation circuit adds voltage ramp into the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

Driver

The power MOSFET is driven by a dedicated gate driver for power switch control. Too weak the gate driver strength results in higher conduction and switch loss of MOSFET while too strong gate driver strength results the compromise of EMI.

A good tradeoff is achieved through the built-in totem pole gate design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme.

Dual Function of External OTP and Output OVP



On-Bright proprietary dual function of external OTP and output OVP provides feasible and accurate detection of external OTP through NTC resistor and output OVP. The dual function is realized through time-division technology as shown in the figure. To meet Dell's OTP application requirement, the specification for the OTP threshold voltage, VOTP, is 1.0V (typical), the specification of the outflowing current for external OTP detection, IRT, is 100uA (typical).

There is a 20uA(typical) bias current outflowing except during Sovp=1. For external OTP detection, when switch control signal S1= "1", the 20uA (typical) current flows out from PRT pin. When switch control signal S0= "1", another 100uA (typical) current flows out from PRT pin in addition to 20uA.

So the PRT pin voltage V1(s0) at phase S1="1" is:

$$V1(s1) = \frac{ROVP \cdot VD + RT \cdot Vaux + RT \cdot ROVP \cdot 20uA}{ROVP + RT}$$

The PRT pin voltage V1(s1) at phase S0="1" is

$$V1(s0) = \frac{ROVP \cdot VD + RT \cdot Vaux + RT \cdot ROVP(20uA + 100uA)}{ROVP + RT}$$

Vaux is the auxiliary winding demagnetization voltage.

VD is D1 forward voltage.

ROVP and RT are shown in fig3.

Voltage difference of ΔVotp at phase S0 and S1 phase is

$$\Delta V_{otp} = V1(s0) - V1(s1) = \frac{RT \cdot ROVP}{ROVP + RT} \cdot 100uA$$

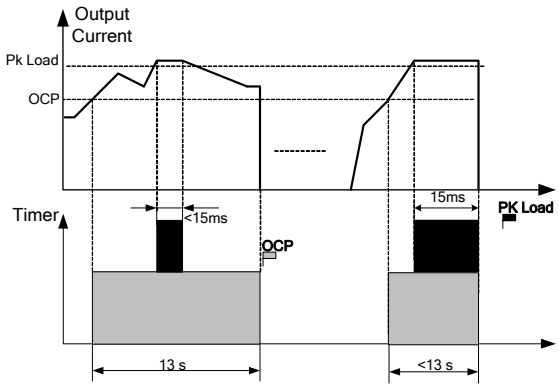
This voltage difference cancels the effect of D1 diode forward voltage.
When △Votp<VOTP (1.0V typical) , external OTP latch protection is triggered after 60 (typical) PWM cycles debounce.

For output OVP detection, when Sovp= “1”, Iovp is equal to Vo/ROVP. To meet output OVP application requirements, the Current threshold for adjustable output OVP, Ioutput_ovp，is specified as 180uA (typical). If Iovp is larger than Ioutput_ovp, output OVP is triggered. The output OVP is calculated as

$$V_{outovp} = \frac{180uA \cdot N_{sec} . ROVP}{N_{aux}} - V_{diode}$$

Nsec is transformer secondary winding turns, Naux is transformer auxiliary winding turns, Vdiode is the secondary output diode forward voltage .
OVP latch protection is triggered after 5 Gate cycles debounce. By selecting proper Rovp resistance, output OVP level can be programmed.

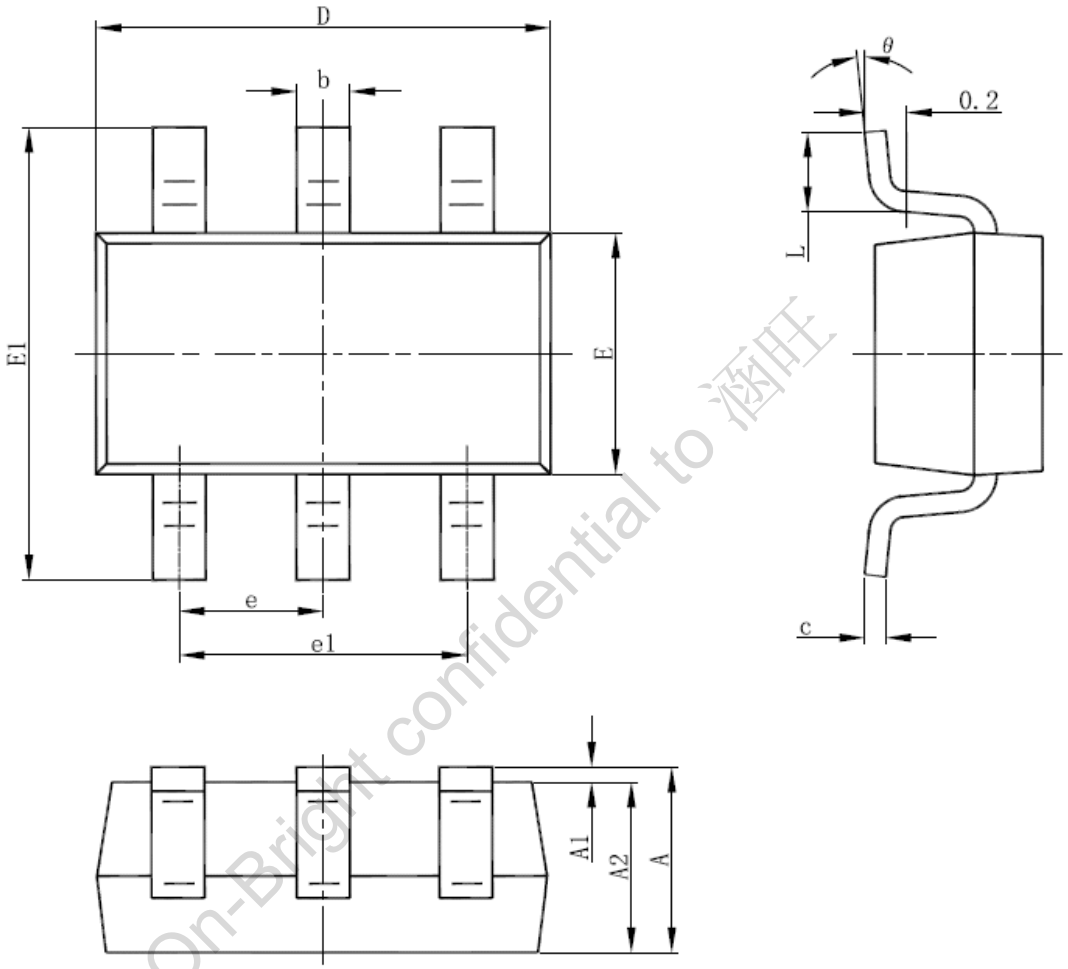
OCP and Peak output Current Controls
In order to meet peak current output requirement, OB2362D sets up two levels OCP protection thresholds. The two thresholds correspond to the normal OCP protection and peak power protection respectively, and these two threshold values are internally compensated. When primary side inductor current exceeds the OCP threshold, OCP timer will begin counting. After 13s (typical), OCP protection occurs.
When primary side inductor current exceeds the peak power threshold, over peak power timer will begin counting. After 15ms (typical), peak load protection occurs.
OCP and peak power protection are mutually independent and do not affect each.
When



Protection Controls
Good power supply system reliability is achieved with auto-recovery protection features including Cycle-by-Cycle current limiting (OCP), Under Voltage Lockout on VDD (UVLO), Over Temperature Protection (OTP), VCC and output Over Voltage Protection (OVP).
With On-Bright proprietary technology, the OCP is line voltage compensated to achieve constant output power limit over the universal input voltage range.
At overload condition when FB input voltage exceeds power limit threshold value for more than Td_PK, control circuit reacts to shut down the converter. It restarts when VDD voltage drops below UVLO limit.
At output diode short condition, CS can ramp higher than 1.1V (typical). After counting 8 cycles for CS higher than 1.1V (typical), auto- recover protection is triggered.
At start up, normally gate driver turn-on time grow longer, if 15ms later, the turn-on time is less than 1.1us (typical) in consecutive 9 cycles, SCP protection occurs, OB2362D auto recovery.

PACKAGE MECHANICAL DATA

SOT-23-6L PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.000	1.450	0.039	0.057
A1	0.000	0.150	0.000	0.006
A2	0.900	1.300	0.035	0.051
b	0.300	0.500	0.012	0.020
c	0.080	0.220	0.003	0.009
D	2.800	3.020	0.110	0.119
E	1.500	1.726	0.059	0.068
E1	2.600	3.000	0.102	0.118
e	0.950 (BSC)		0.037 (BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

IMPORTANT NOTICE

RIGHT TO MAKE CHANGES
On-Bright Electronics Corp. reserves the right to make corrections, modifications, enhancements, improvements and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

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On-Bright Electronics Corp. assumes no liability for application assistance or customer product design. Customers are responsible for their products and applications using On-Bright's components, data sheet and application notes. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

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