PIXELPLUS CO., LTD.

Data sheet

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1/4 inch VGA class Analog/Digital Output NTSC/PAL CMOS Image Sensor

PC1030N

Rev 1.0

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1/4 inch VGA class Analog/Digital Output NTSC/PAL CMOS Image Sensor

▶ Revision History

Version	Date [D/M/Y]	Notes	Writer
0.0	20/05/2008	*(Preliminary)*	Jong Beom Choi
0.1	04/06/2008	Customer datasheet is released	SungJe Cheon
0.2	20/06/2008	DVDD voltage is modified	SungJe Cheon
0.3	04/07/2008	Add DC Characteristics Add AC Characteristics Add Optical Performance Add Power Sequence	Junhee Cho
0.4	09/07/2008	Modify effective pixel area. Fig.10	SungJe Cheon
0.5	22/07/2008	Modify LED Control	Bongju Lee
0.6	28/07/2008	Add VGA digital output only mode	SungJe Cheon
0.7	23/09/2008	Removed “Preliminary” letters	Jincheol Jeong
0.8	06/02/2009	Released Power Sequence	Yoon Shik Kim
0.9	27/03/2009	Change (Total pixel array → Effective pixel array)	Heungseok Park
1.0	21/05/2009	Add Application note	Jongwu Ryu
1.1	22/09/2009	Change(SCLK → SSCLK, SDAT → SSDAT, RCLK → RSCLK, RDAT → RSDAT) Page 7,20,29,30 Modify Fig number. Page 13,14,15,18,19	JiKyung Moon

Caution : This datasheet can be changed without prior notice !! If you want to get up-to-date version, please send a mail to support@pixelplus.co.kr.

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▶ Features

▷ 648 x 488 Effective pixel array with RGB bayer color filters and micro-lens and optical black pixel.

▷ Power supply :
AVDD : 2.8V, CVDD : 2.8V, DVDD : 1.8V, HVDD : 2.8 ~ 3.3V

▷ Output formats :
CVBS (NTSC/PAL),
ITU-R. BT601/656(60 fields/sec. interlaced @ 27MHz) with CVBS,
320x240(288) YCbCr422 (30(25)fps. @ 27MHz) with CVBS,
640x480(VGA) YCbCr422 digital output only (30fps. @ 27MHz).

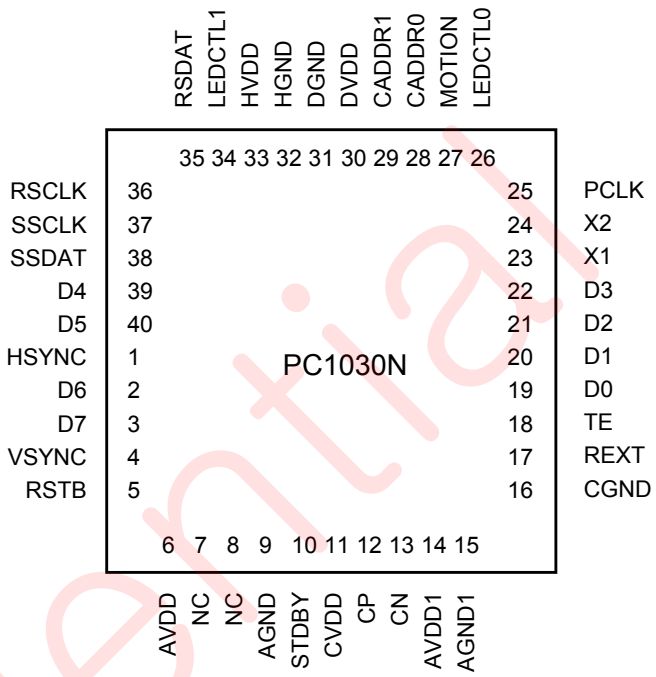
▷ Image processing on chip :
lens shading, gamma correction, defect correction, low pass filter, color interpolation, edge enhancement, color correction, brightness, contrast, saturation, auto black level compensation, auto white balance, auto exposure control and back light compensation.

▷ Frame size, window size and position can be programmed through a 2-wire serial interface bus.

▷ VGA / QVGA / QQVGA / CIF / QCIF Scaling.

▷ 50Hz, 60Hz flicker automatic cancellation.

▷ High Image Quality and High low light performance.



[Fig. 1] PIN Description (CLCC)

Optical Format	¼ inch
Pixel Size	5.55 um x 5.55 um
Effective Pixel Array	648 x 488
Effective Image Area	3596.4um x 2708.4um
Clock Frequency	27 MHz
Frame Rate	60(50) fields/sec @ 27MHz
Dark Signal	47.9 [mV/sec] @60'C
Sensitivity	3.16 [V/Lux.sec]
Power Consumption	213 [mW] @ Dynamic
	19.2 [uW] @ Standby
Operating Temp. (Fully Functional Temp.)	-40'C ~ 105'C
Dynamic Range	63.5 [dB] @60'C
SNR	45.6 [dB] @60'C

[Table 1] Typical Parameters

▶ PIN Descriptions

[Table 2] Pin Descriptions

PIN No.	Name	I/O Type	Functions / Descriptions
1	HSYNC	O	Horizontal synchronization pulse. HSYNC is high (or low) for the horizontal window of interest. It can be programmed to appear or not outside the vertical window of interest.
2	D6	O	Bit 6 of parallel data output.
3	D7	O	Bit 7 of parallel data output.
4	VSYNC	O	Vertical sync : Indicates the start of a new frame.
5	RSTB	I	System reset must remain low for at least 8 master clocks after power is stabilized. When the sensor is reset, all registers are set to their default values.
6	AVDD	P	Analog Power supply : 2.8V DC with 0.1uF capacitor to AGND.
7	N.C		
8	N.C		
9	AGND	P	Analog Power ground
10	STDBY	I	Power standby mode. When STDBY='1' there's no current flow in any analog circuit branch, neither any beat of digital clock. D<9:0> and PCLK, HSYNC, VSYNC pins can be programmed to tri-state or all '1' or all '0'. But it is possible to control internal registers through I2C bus interface in STDBY mode. All registers retain their current values.
11	CVDD	P	DAC Power supply : 2.8V DC with 0.1uF capacitor to AGND.
12	CP	O	Composite signal. (Connect to 75ohm to AGND)
13	CN	O	Connect 37.5ohm to AGND
14	AVDD1	P	Analog Power supply : 2.8V DC with 0.1uF capacitor to AGND.
15	AGND1	P	Analog Power ground
16	CGND	P	DAC Power ground.
17	REXT	I	External Resistor. The resistor value can be changed by user tuning. (Connect to 30Kohm to AGND)
18	TE	I	Chip Test Mode enable. (Connect to HGND)
19	D0	O	Bit 0 of parallel data output.
20	D1	O	Bit 1 of parallel data output.
21	D2	O	Bit 2 of parallel data output.
22	D3	O	Bit 3 of parallel data output.
23	X1	I	Master clock input pad or Crystal input pad
24	X2	O	Crystal output pad
25	PCLK	O	Pixel clock. Data can be latched by external devices at the rising or falling edge of PCLK. The polarity and drivability can be controlled.
26	LEDCTRL0	O	LED Control bit 0. LEDCTRL[1:0] provide 2bit combination of enable signal which can turn-on LED device when low light condition.

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PIN No.	Name	I/O Type	Functions / Descriptions
27	MOTION	O	Motion detection. It lets user or processor know whether there are motion of something on video. When the motion exists on the video, the output goes LOW to HIGH
28	CADDR0	I	Chip address bit 0. Chip address can be changed If this CADDR[1:0] pins are tied to HVDD or HGND.
29	CADDR1	I	Chip address bit 1. Chip address can be changed If this CADDR[1:0] pins are tied to HVDD or HGND.
30	DVDD	P	Digital Power supply : 1.8V DC with 0.1uF to DGND
31	DGND	P	Digital Power ground.
32	HGND	P	I/O Power ground.
33	HVDD	P	I/O Power supply: 2.8~3.3V DC with 0.1uF capacitor to HGND.
34	LEDCTRL1	O	LED Control bit 1. LEDCTRL[1:0] provide 2bit combination of enable signal which can turn-on LED device when low light condition.
35	RSDAT	I/O	2-wire serial interface for external EEPROM.
36	RSCLK	O	2-wire serial interface for external EEPROM
37	SSCLK	I	2-wire serial interface slave clock input.
38	SSDAT	I/O	2-wire serial interface slave databus.
39	D4	O	Bit 4 of parallel data output.
40	D5	O	Bit 5 of parallel data output.

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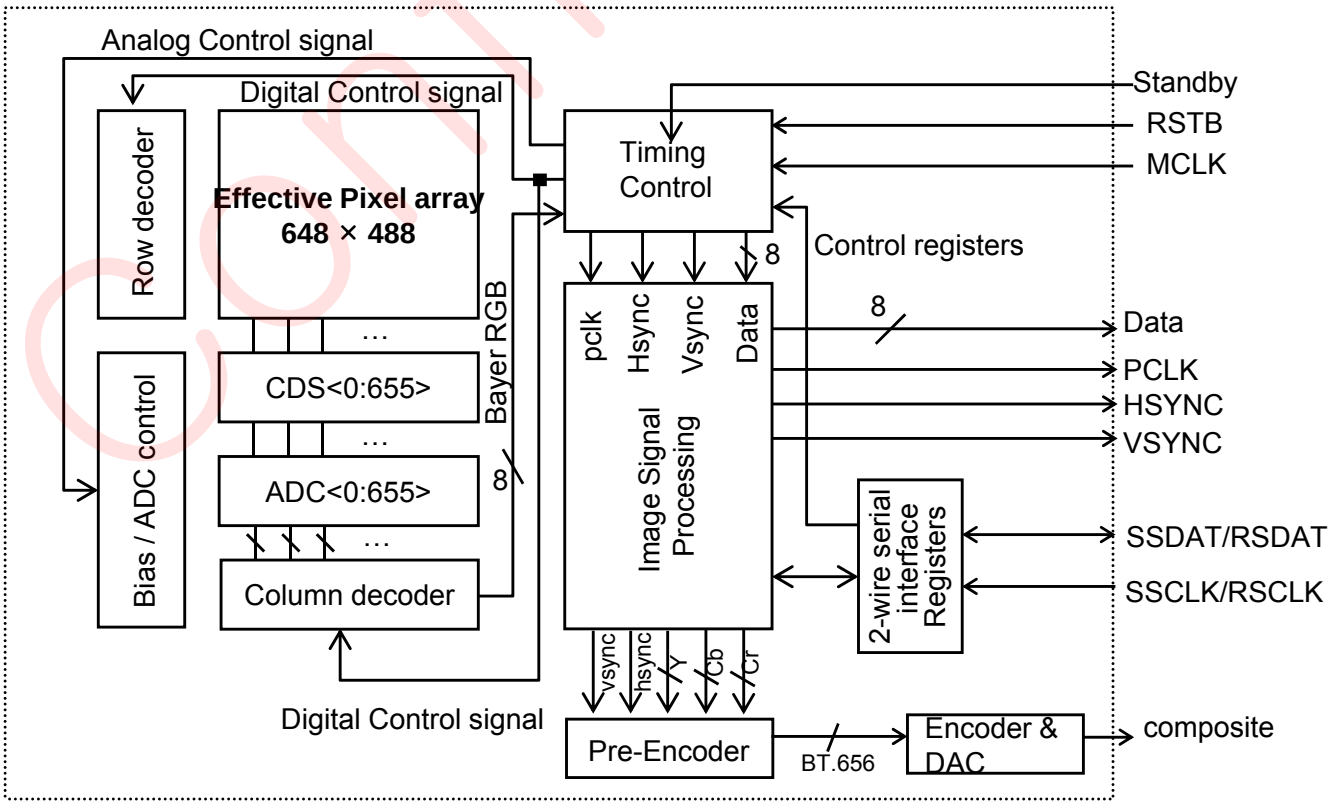
▶ Signal Environment

PC1030N has 3.3V tolerant Input pads. Input signals must be higher than or equal to HVDD but cannot be higher than 3.3V. PC1030N input pad has built in reverse current protection circuit, which makes it possible to apply input voltage even if the HVDD is disconnected or floating. Voltage range for all output signals is 0V ~ HVDD.

▶ Chip Architecture

PC1030N has 648 x 488 effective pixel array and column/row driver circuits to read out the pixel data progressively. CDS circuit reduces noise signals generated from various sources mainly resulting from process variations. Pixel output is compared with the reset level of its own and only the difference signal is sampled, thus reducing fixed error signal level. Each of R, G, B pixel output can be multiplied by different gain factors to balance the color of images in various light conditions. The analog signals are converted to digital forms one line at a time and 1 line data are streamed out column by column. The Bayer RGB data are passed through a sequence of image signal processing block and pre-encoder and encoder blocks to produce YCbCr 4:2:2 output data or composite output. Image signal processing includes such operations as gamma correction, defect correction, low pass filter, color interpolation, edge enhancement, color correction, contrast stretch, color saturation, white balance, exposure control and back light compensation. Internal functions and output signal timing can be programmed simply by modifying the register files through 2-wire serial interface.



[Fig. 2] Block Diagram

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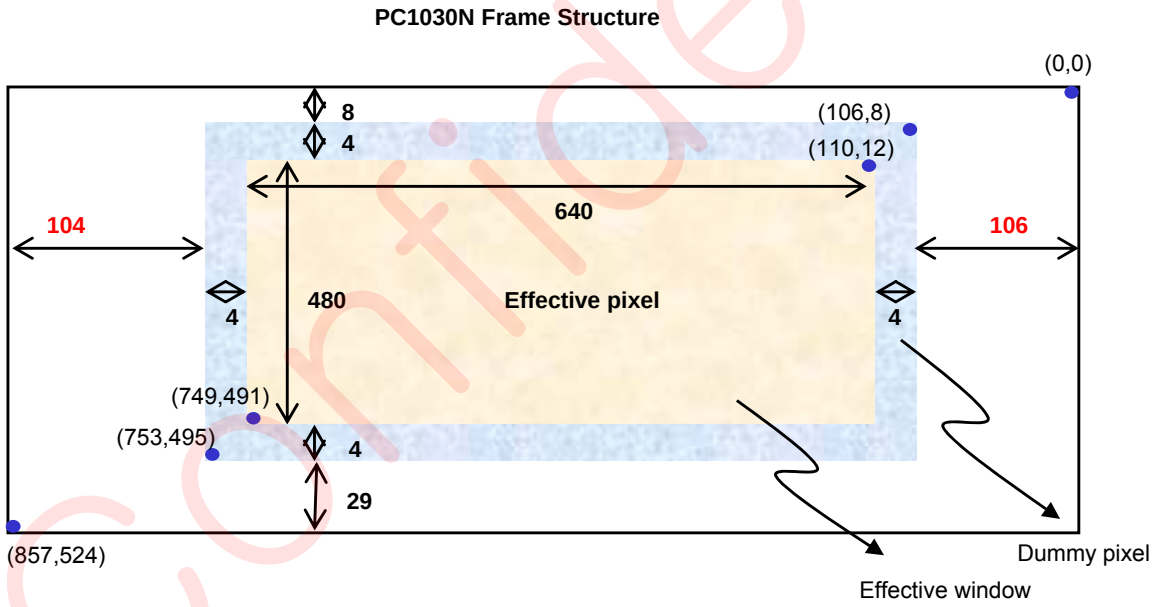
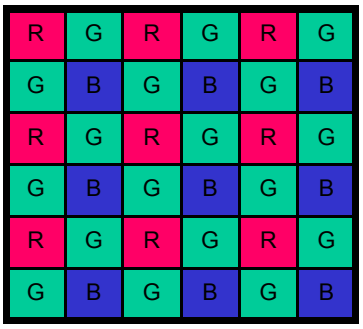
▶ Frame Structure and Windowing

Origin *(0, 0)* of the frame is at the upper right corner. Size of the frame is determined by two registers : *framewidth(Reg.A-06h, A-07h)* and *frameheight(Reg.A-08h, A-09h).* One frame consists of *framewidth + 1* columns and *frameheight + 1* rows. *framewidth* and *frameheight* can be programmed to be larger than total array size. Default window array of 640 x 480 pixels is positioned at *(110, 12).* It is possible to define a specific region of the frame as a window. Pixel scanning begins from *(0, 0)* and proceeds row by row downward, and for each line scan direction is from right to the left. Hsync signal indicates if the output is from a pixel that belongs to the window or not. There are two counters to indicate the present coordinate of frame scanning : Frame row counter and frame column counter. Counter values repeat the cycle of 0 to *frameheight* , and 0 to *framewidth* respectively. The counter values increase at the pace of pixel clock (PCLK), which does not change as the frame size is altered. The pixel data rate is fixed and is independent of frame size(frame rate).



[Fig. 3] Default data structure of frame and window. (Top view)

▶ Digital Data Formats



[Fig. 4] Bayer Color filter pattern

Pixel array is covered by Bayer color filters as can be seen in the [Fig. 4]. Since each pixel can have only one type of filter on it, only one color component can be produced by a pixel. PC1030N sensor provides this Bayer pattern RGB data through an 9-bit channel. It takes one PCLK to pass one pixel RGB data to output bus. Generally one pixel of an image consists of R,G,B color components. Since one pixel of bayer RGB is composed of one of the 3 components, the other two components of a pixel must be derived from neighbor pixels. For example, G component for a B pixel is calculated as an average of its four nearest G neighbors, and its R component as an average of its four nearest R neighbors.

This operation of inferring missing data from existing ones is called the color interpolation. Color interpolation produces an undesirable artifact in image. Sampling nature of color filter can leave an interference pattern around an area with repetitive fine lines. PC1030K adopts a low pass filter to prevent the interference patterns (called Moire pattern) from degrading the image quality too much. After color interpolation, every pixel has all three color components. And then the pixel data pass image processing block to improve the image quality.

It is possible to extract monochrome luminance data from RGB color components and the conversion equation is : Y = 0.299R + 0.587G + 0.114B where R,G and B are gamma corrected color components. And the color information is separated from luminance information according to following equations.

$$Cb = -0.148R - 0.291G + 0.439, \quad Cr = 0.439R - 0.368G - 0.071B$$

Since human eyes are less sensitive to color variation than to luminance, color components can be sub-sampled to reduce the amount of data to be transmitted, but preserving almost the same image quality.

Cb1	Y1	Cr1	Y2	Cb3	Y3	Cr3	Y4	…

[Fig. 5] 4:2:2 YCbCr data sequence.

PC1030K supports 4:2:2 YCbCr data format where Cb and Cr components are horizontally sub-sampled such that U and V for every other pixel are omitted. PC1030K also support 4:2:2 YUV data format.

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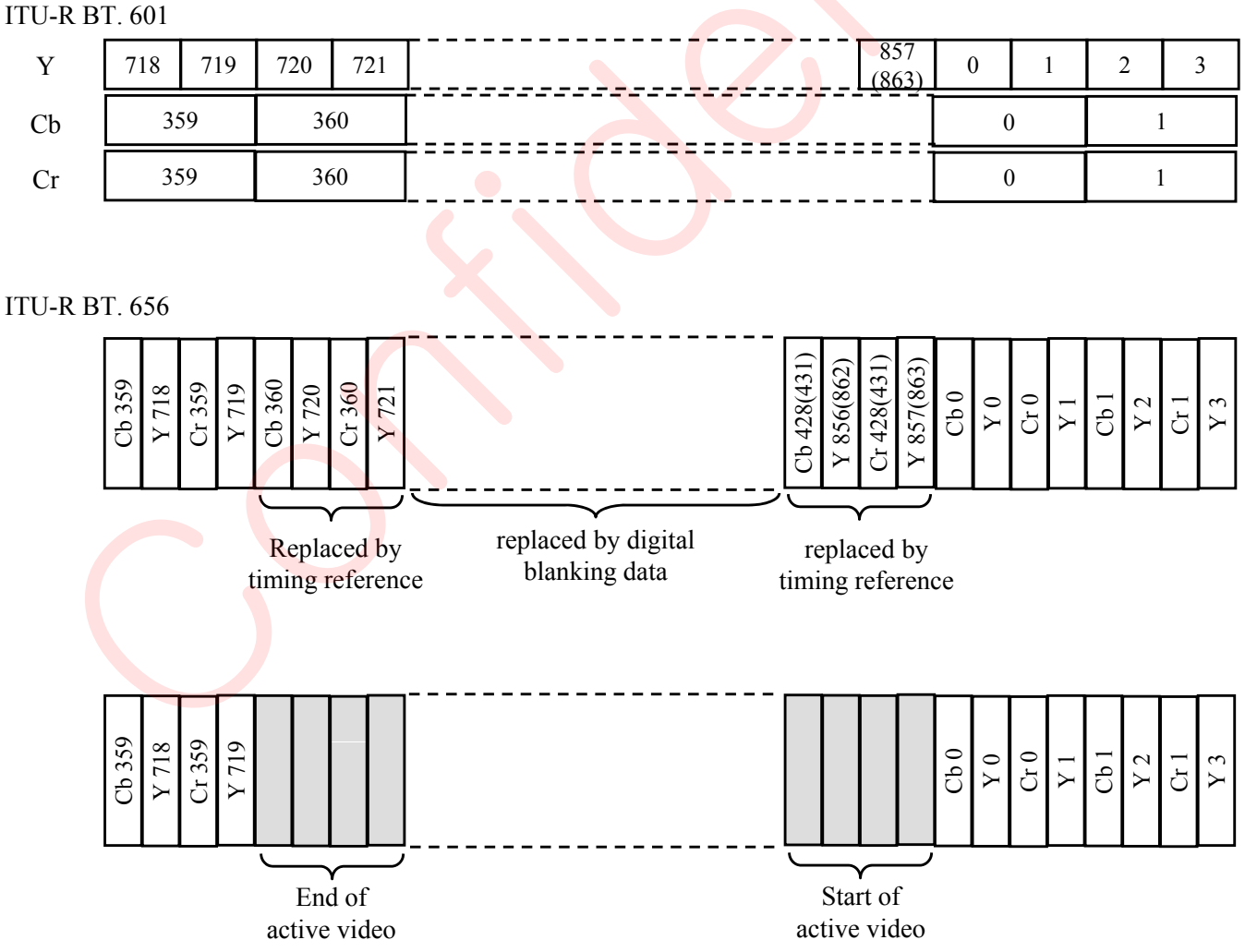
▶ Data and Synchronization Timing

(1) ITU-R BT656 (CCIR656)

[Fig. 6] shows ITU-R BT601 and ITU-R BT656 timing diagram. Sampling clocks of ITU-R BT601 and ITU-R BT656 are 13.5MHz and 27MHz respectively. ITU-R BT656 format is generated from ITU-R BT601 format data by serialization and timing reference. Timing reference indicates Start or End of video. It includes field, vsync and hsync information.

PC1030N provides two kinds of active video sizes with BT656 format such as 720x480i and 720x576i ('i' stands for interlaced scan). The horizontal size is stretched from 640 to 720 pixels. 720x480i size BT656 supports for 525-line video, and 720x576i size BT656 for 625-line video. Horizontal timing of 720x480i and 720x576i size BT656 is shown in [Fig. 6] and vertical Timing diagram is shown in [Fig. 7]



[Fig. 6] Timing diagram of ITU-R BT601 and ITU-R BT656

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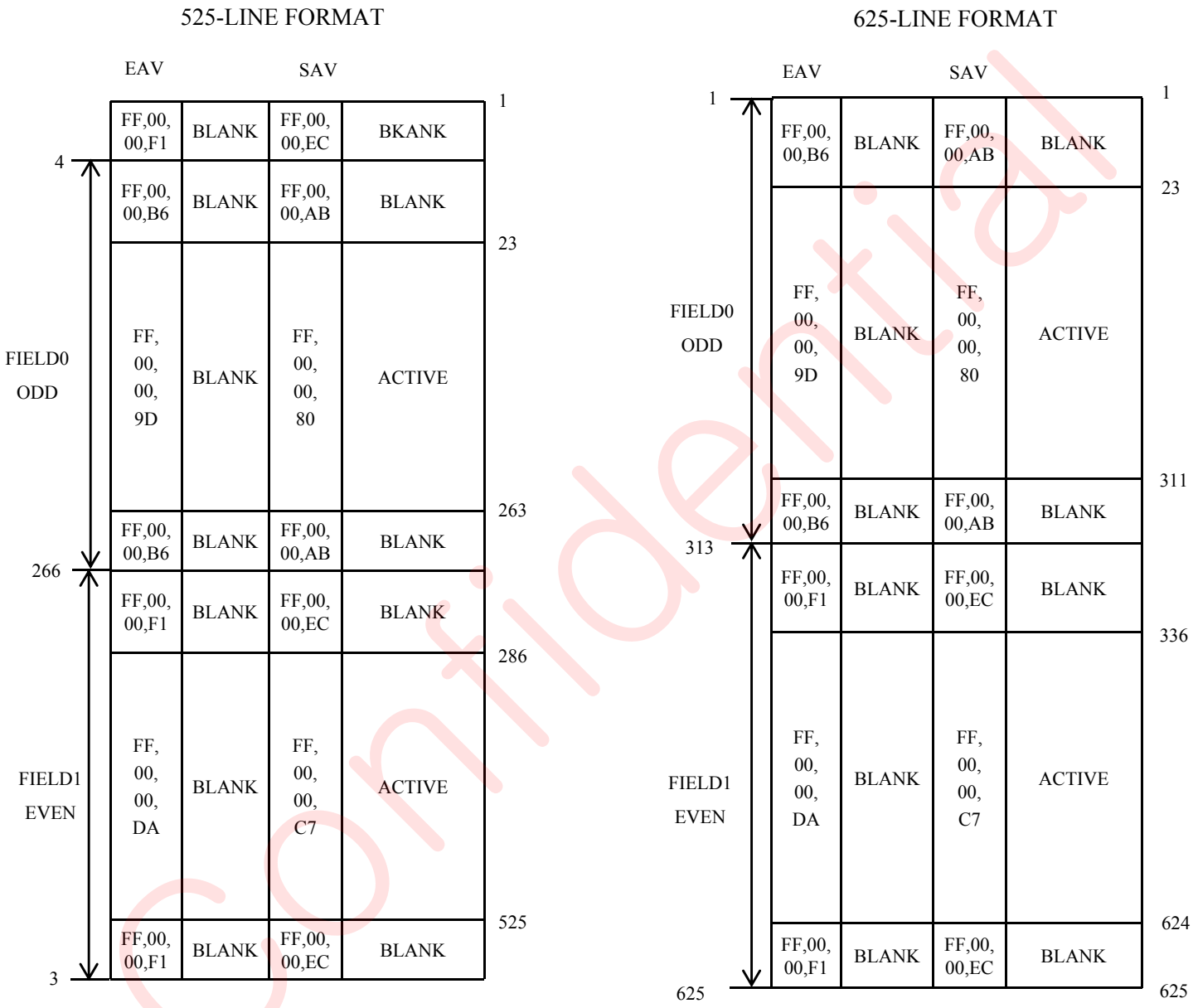


[Fig. 7] Vertical Timing diagram of ITU-R BT656

- The numbers on the image indicate Line number.
- For 525-line format, active lines are 240 per a field. For 625-line format, active lines are 288 per a field.
- Vertical Timing is slightly different to Typical BT.656 for 525-line format. In active data regions above [Fig. 7], they have only active pixel data not any fixed data (eg. black data).
- (design reference: Video Demystified 3rd edition, chapter 4)

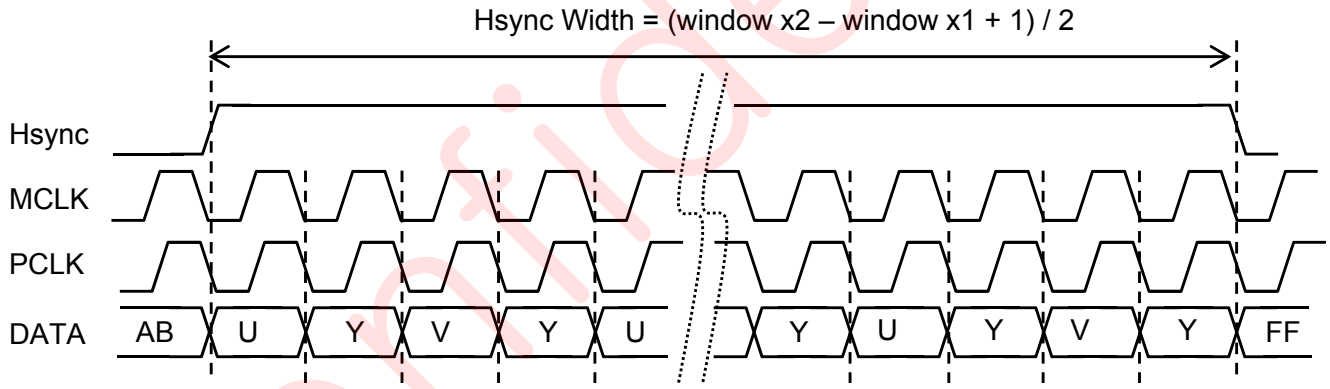
(2) 320x240 (320x288) Digital Output Timing

[Fig. 8] shows the Horizontal sub-sampled YUV422 data sequence of PC1030N. In this mode, the frequencies of MCLK, PCLK and internal processing clock are equal. And Horizontal data are reduced by one half of full size(640). The width of Hsync can be programmed by *windowx1 / x2(Reg.A-0Ah, 0Bh, 0Eh, 0Fh)* and given by

Hsync Width = *(windowx2 - windowx1 + 1) / 2*

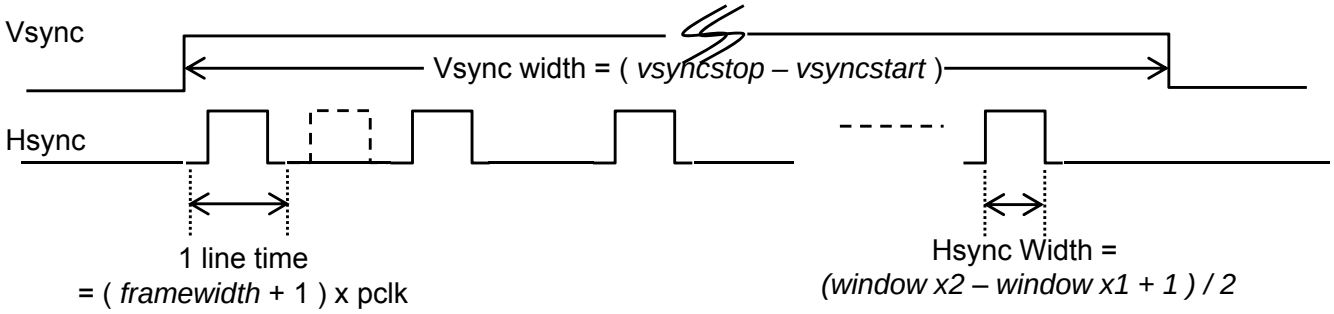
It is not the same to horizontal scaling. This mode can provide digital data output concurrent to analog TV output. In NTSC mode, it provides 320x240 size images with 30fps. And in PAL mode, it does 320x288 size images with 25 fps.

In this mode Hsync / PCLK polarity can also have any combinations possible. Data can be latched at the rising or falling edge of PCLK. Hsync can be set to be active high or active low
Data value can be selected in Invalid or blanking region . (Reg.B-13h ~ 16h, Reg. B-1B ~ 1Eh)



[Fig. 8] Timing diagram for Hsync, MCLK, PCLK and Data

[Fig. 9] shows timing diagram of Vsync and Hsync in NTSC mode. Valid Hsync number is controlled by scale_y, windowY1 and windowY2 registers. Vsync is controlled by Vsyncstart and vsyncstop registers.



[Fig. 9] Timing diagram for Vsync and Hsync

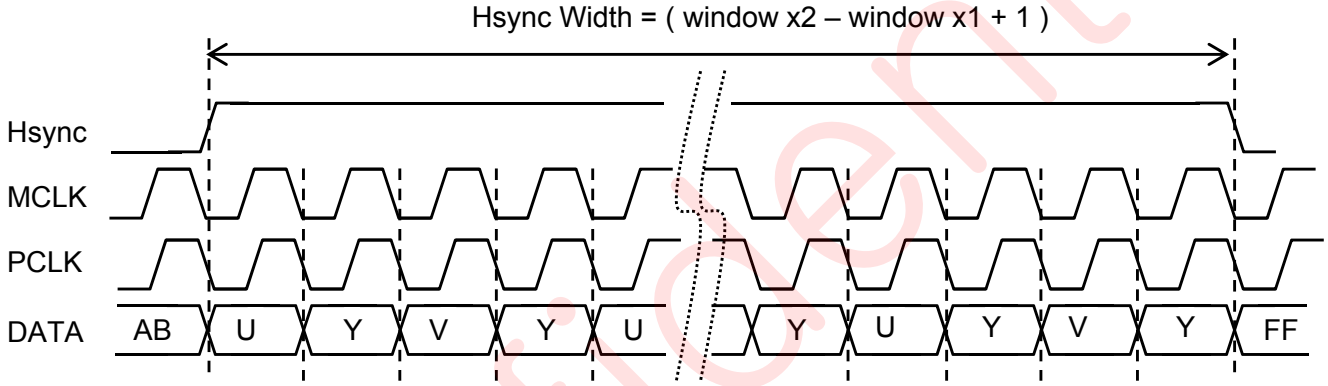
(3) 640x480 VGA Digital Output Only Timing

[Fig. 10] shows the VGA data sequence of PC1030N. In [Fig. 10] Hsync / PCLK polarity can have any combinations possible. Data can be latched at the rising or falling edge of PCLK. Hsync can be set to be active high or active low. The sequence default YUV data is [U,Y, V, Y, …] for common even / odd rows.

The width of Hsync can be programmed by *windowx1 / x2(Reg.A-0Ah, 0Bh, 0Eh, 0Fh)* and given by

Hsync Width = *(windowx2 - windowx1 + 1)*

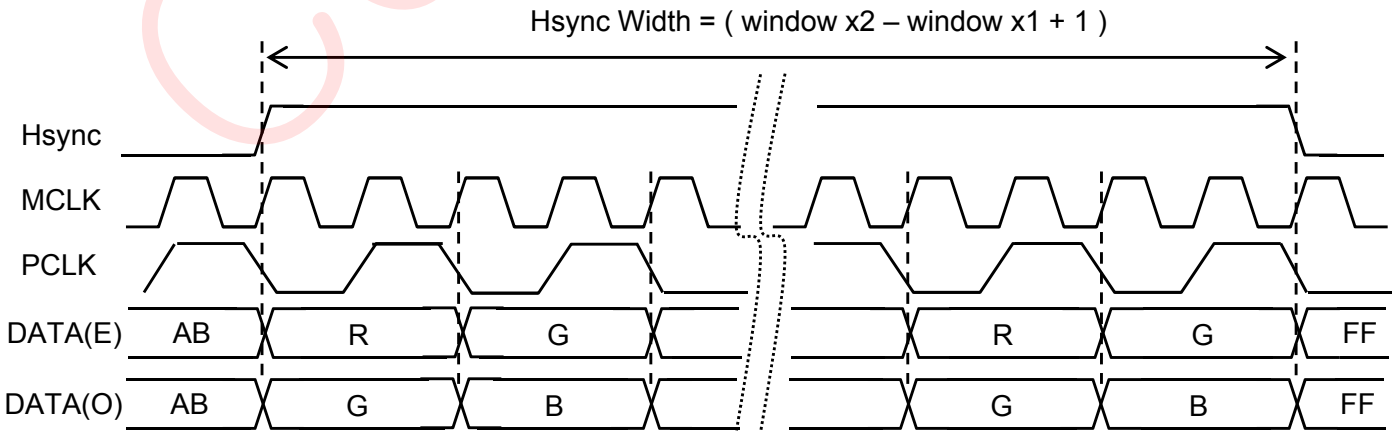
Data value can be selected in Invalid or blanking region . (Reg.B-13h ~ 1Eh)



[Fig. 10] Timing diagram for Hsync, MCLK, PCLK and Data (default)

The default sequence Bayer data is [RGRG…] for even rows and [GBGB…] for odd rows. The data order can be changed by register (*Reg.B-09h).*

[Fig. 11] shows the bayer data sequence of PC1030N. PCLK frequency is (MCLK)/2 when output data is bayer data.



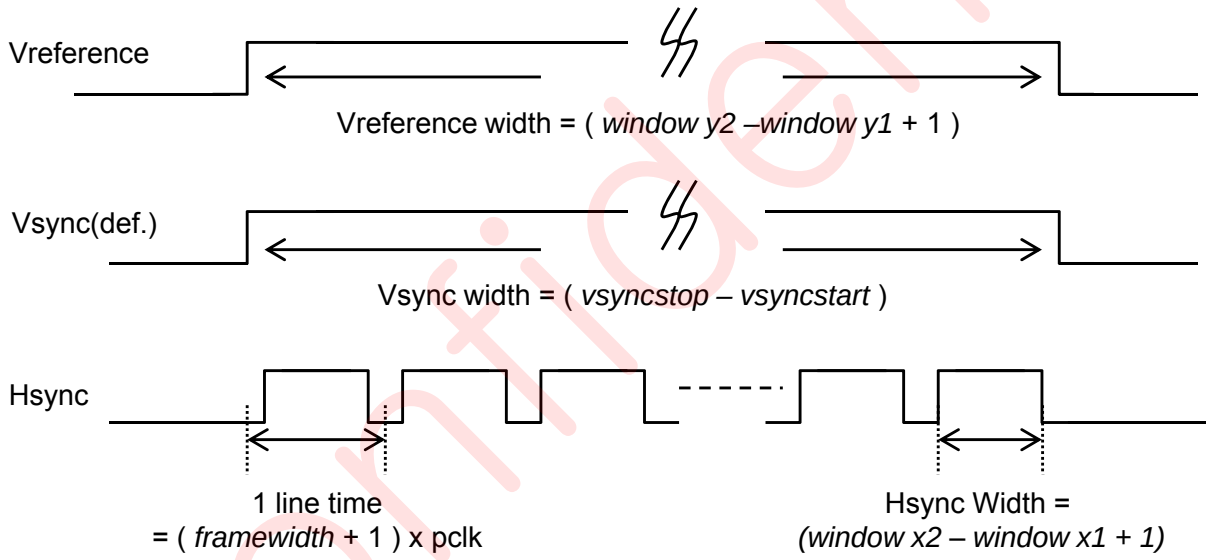
[Fig. 11] Timing diagram for Hsync, MCLK', PCLK and Data (Bayer)

In [Fig. 12], Vsync polarity also can have any combinations possible and can be set to be active high or active low. The width of Vsync can be programmed by *vsyncstart / vsyncstop(Reg.A-12h ~ 15h)* and given by

Vsync Width = (*vsyncstop – vsyncstart*).

The width of Vreference can be programmed by register *windowy1 / y2(Reg.A-0Ch, 0Dh, 10h, 11h)* and given by

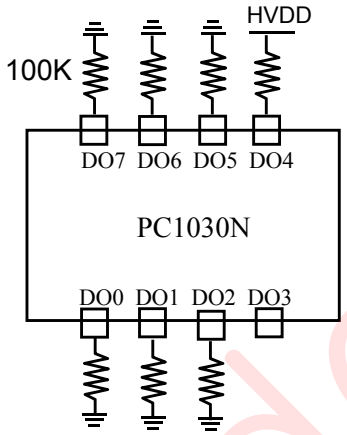
Vreference width = (*windowy2* - *windowy1* + 1).



[Fig. 12] Timing diagram for Vsync and Hsync

▶ NTSC/PAL Wire-strapping

Wire_strapping is a function of chip mode selection at Reset(HW reset or soft reset). Chip mode is automatically selected according to DO7~DO0 pads wired with pull-up or pull-down at RESET. [Fig.10] shows one example of Wire-strapping configuration and [Table 3] shows chip mode selection by wire-strapping.



[Fig.13] Example of wire-strapping ((M)NTSC, Manual-A Flicker Mode, No Mirror)

		DO7	DO6	DO5	DO4	DO2	DO1	DO0
TV_MODE	(M)NTSC	-	-	-	-	L	L	L
	NTSC-J	-	-	-	-	L	L	H
	(M)PAL	-	-	-	-	L	H	L
	(Nc)PAL	-	-	-	-	L	H	H
	(N)PAL	-	-	-	-	H	L	L
	(B,D,G,H,I)PAL	-	-	-	-	H	L	H
FLICKER	No Flicker cancel	-	-	L	L	-	-	-
	Manual-A	-	-	L	H	-	-	-
	Manual-B	-	-	H	L	-	-	-
	Auto Flicker cancel	-	-	H	H	-	-	-
MIRROR	No Mirror	L	L					
	Mirror-V	H	L	-	-	-	-	-
	Mirror-H	L	H	-	-	-	-	-
	Mirror-VH	H	H	-	-	-	-	-

[Table 3] wire-strapping

[Table 4] shows TV_mode wire-strapping registers. The registers are changed by DO2~DO0 under RESET='0'.

		"000b"	"001b"	"010b"	"011b"	"100b"	"101b"
Register name	Reg.Addr	(M)NTSC	NTSC-J	(M)PAL	(Nc)PAL	(N)PAL	(OTHER)PALs
chip_mode	A-04h	00	00	00	01	01	01
framewidth	A-06/07h	0359	0359	0359	040D	040D	040D
frameheight	A-08/09h	020C	020C	020C	0207	0207	0207
windowy2	A-10/11h	00F0	00F0	00F0	0120	0120	0120
scale_y	B-21h	40	40	40	35	35	35
fd_a_step	B-89/8Ah	03E8	03E8	03E8	03F0	03F0	03F0
fd_b_step	B-8B/8Ch	0341	0341	0341	04B9	04B9	04B9
fd_period_a	B-91/92/93h	010600	010600	010600	010380	010380	010380
fd_period_b	B-94/95/96h	013AAF	013AAF	013AAF	00D8C3	00D8C3	00D8C3
fd_period_c	B-97/98h	0625	0625	0625	0514	0514	0514
fd_fheight_a	B-99/9Ah	020C	020C	020C	0207	0207	0207
fd_fheight_b	B-9B/9Ch	020C	020C	020C	0207	0207	0207
enc_scfreq	B-A5h	00	00	03	02	01	01
enc_blank	B-A8h	F0	F0	F0	FC	F0	FC
enc_pedestal	B-A9h	2A	00	2A	00	2A	00
enc_burst	B-Aah	70	70	75	75	75	75
enc_Ygain	B-Abh	82	8D	82	89	82	89
enc_Ugain	B-Ach	6F	78	6F	75	6F	75
enc_Vgain	B-Adh	9C	A9	9C	A6	9C	A6
enc_Crange_L	B-B1h	48	62	48	5B	48	5B
enc_chroma_max_L	B-B3h	CD	DF	CD	D7	CD	D7
enc_chroma_min_L	B-B5h	6D	35	6D	45	6D	45
expfrmH	C-11h	020C	020C	020C	0207	0207	0207
ae_winy_L	C-51h	07	07	07	08	08	08
ae_height	C-54/55h	00E2	00E2	00E2	0110	0110	0110
ae_cwiny_L	C-59h	4C	4C	4C	5B	5B	5B
ae_cheight_L	C-5Dh	4B	4B	4B	5A	5A	5A

[Table 4] TV_mode registers

[Table 5] and [Table 6] show Flicker mode and Mirror mode related registers and setting values at RESET respectively.

	"00b"	"01b"	"10b"	"11b"
Register name	Normal(off)	manual A	manual B	auto fd
flicker_control_2	80	88	84	C0

[Table 5] Flicker mode register

	"00b"	"01b"	"10b"	"11b"
Register name	No mirror	H mirror	V mirror	HV mirror
mirror	00	01	02	03

[Table 6] Mirror mode register

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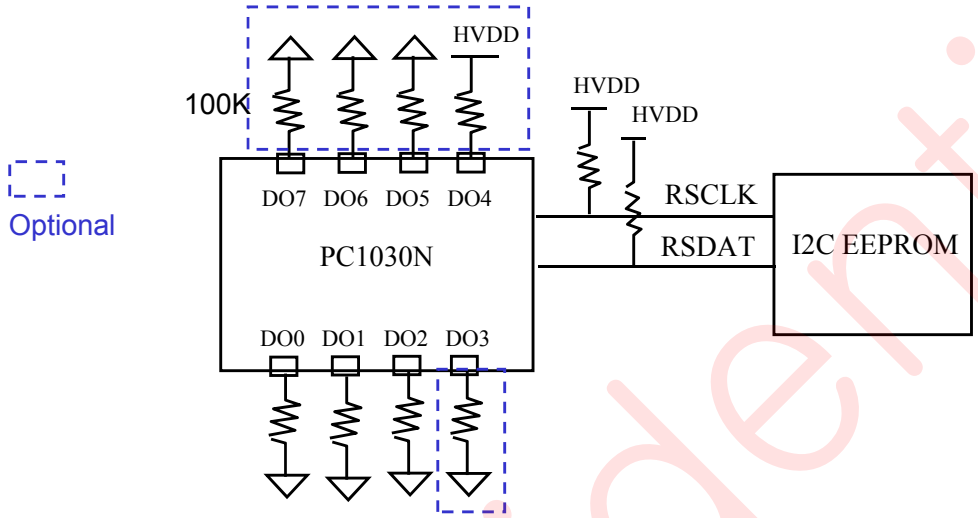
▶ Register Initializing by I2C-EEPROM

PC1030N supports that user tuning registers can be set by I2C EEPROM initially. After reset time it tries to access I2C EEPROM whether it has connected. If the connection has accomplished, it reads data from I2C EEPROM and sets its registers. [Fig. 14] shows how to connect PC1030N and I2C EEPROM.



[Fig. 14] Example of connection with EEPROM

User can make use of two methods below. Please refer to [Fig. 15] on next page about EEPROM configuration.

1. Using strap & EEPROM – NTSC / PAL selectable by strap
   (1) Write proper values to NTSC_START, NTSC_LENGTH, PAL_STARTP, PAL_LENGTH, COM_STARTP and COM_LENGTH on EEPROM
   (2) Write register addresses and data that user want to set on EEPROM
   (3) Adjust strap as user want.
   * (M)NTSC, NTSC-J, (M)PAL : Setting is loaded by NTSC_START and NTSC_LENGTH.
   (Nc)PAL, (N)PAL, (B,D,G,H,I)PAL : Setting is loaded by PAL_STARTP and PAL_LENGTH
   * Caution : In case PAL-M, NTSC setting method should be used

2. Using EEPROM without strap – NTSC or PAL only
   (1) Write 0(zero) to NTSC_STARTP, NTSC_LENGTH, PAL_STARTP, PAL_LENGTH on EEPROM
   (2) Write proper values to COM_STARTP and COM_LENGTH on EEPROM
   (3) Write register addresses and data that user wants to set.

** Caution : It covers up to 2K bytes ROM (24xx16)

ADDRESS	CONTENT	EXAMPLE(DEC)
0	NTSC_STARTP_H	0
1	NTSC_STARTP_L	12
2	NTSC_LENGTH_H	0
3	NTSC_LENGTH_L	10
4	PAL_STARTP_H	0
5	PAL_STARTP_L	22
6	PAL_LENGTH_H	00
7	PAL_LENGTH_L	20
8	COM_STARTP_H	0
9	COM_STARTP_L	50
10	COM_LENGTH_H	0
11	COM_LENGTH_L	30
12	REG_ADDRESS	(NTSC_START)
13	REG_DATA	
14	REG_ADDRESS	
15	REG_DATA	
…	…	
20	REG_ADDRESS	…
21	REG_DATA	(NTSC_END)
22	REG_ADDRESS	(PAL_START)
23	REG_DATA	
..	…	…
41	REG_DATA	(PAL_END)
…	…	…
50	REG_ADDRESS	(COMMON START)
51	REG_DATA	
…	…	…
78	REG_ADDRESS	
79	REG_DATA	(COMMON END)
…	…	…

ROM Address from 0 to 11 are reserved. These memory spaces have information how the EEPROM are configured.

1. NTSC_STARTP_H/L : indicates start address for NTSC setting
2. NTSC_LENGTH: Total length for NTSC setting (Reg.Addrs & Data)
3. PAL_STARTP_H/L : indicates start address for PAL setting
4. PAL_LENGTH : Total length for PAL setting
5. COM_STARTP_H/L : indicates start address for common register setting to NTSC and PAL
6. COM_LENGTH: Total length for common setting

User must configure the pair of register address and setting data

[Fig. 15] Configuration of EEPROM & Example

▶ 2-wire Serial Interface Description

The registers of PC1030N are written and read through the 2-wire Serial Interface. The PC1030N has 2-wire Serial Interface slave. The PC1030N is controlled by the Register Access Clock (SSCLK), which is driven by the 2-wire Serial Interface master. Data is transferred into and out of the PC1030N through the Register Access Data (SSDAT) line. The SSCLK and SSDAT lines are pulled up to VDD by a 2kΩ off-chip resistor. Either the slave or master device can pull the lines down. The 2-wire Serial Interface protocol determines which device is allowed to pull the two lines down at any given time.

Start bit

The start bit is defined as a HIGH to LOW transition of the data line while the clock line is HIGH.

Stop bit

The stop bit is defined as a LOW to HIGH transition of the data line while the clock line is HIGH.

Slave Address

The 8-bit address of a 2-wire Serial Interface device consists of 7-bit of address and 1-bit of direction. A '0' in the LSB of the address indicates write mode, and a '1' indicates read-mode.

Data bit transfer

One data bit is transferred during each clock pulse. The SSCLK pulse is provided by the master. The data must be sGroup During the HIGH period of the SSCLK : it can only change when the SSCLK is LOW. Data is transferred 8 bits at a time, followed by an acknowledge bit.

Acknowledge bit

The receiver generates the acknowledge clock pulse. The transmitter (which is the master when writing, or the slave when reading) releases the data line, and receiver indicates an acknowledge bit by pulling the data line low during the acknowledge clock pulse.

No-acknowledge bit

The no-acknowledge bit is generated when the data line is not pulled down by the receiver during the acknowledge clock pulse. A no-acknowledge bit is used to terminate a read sequence.

Sequence

A typical read or write sequence begins by the master sending a start bit. After start bit, the master sends the slave device's 8-bit address. The last bit of the address determines if the request will be a read or a write, where a '0' indicates a write and a '1' indicates a read. The slave device acknowledges its address by sending an acknowledge bit back to the master. If the request was a write, the master then transfers the 8-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data 8 bits at a time, with the slave sending an acknowledge bit after each 8 bits. The PC1030N uses 8 bit data for its internal registers, thus requiring one 8-bit transfer to write to one register. After 8 bits are transferred, the register address is automatically incremented, so that the next 8 bits are written to the next register address. The master stops writing by sending a start or stop bit. A typical read sequence is executed as follows. First the master sends the write-mode slave address and 8-bit register address just as in the write request. The master then sends a start bit and the read-mode slave address. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The register address is auto-incremented after each 8 bit is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

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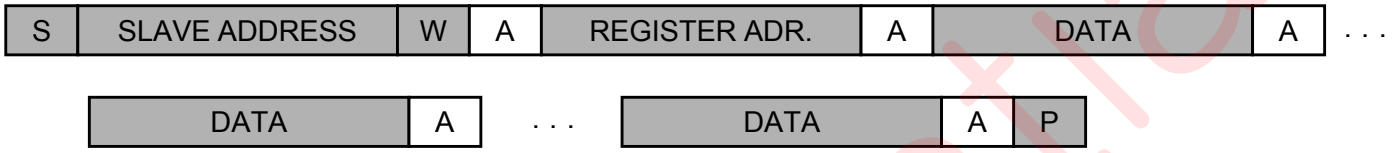
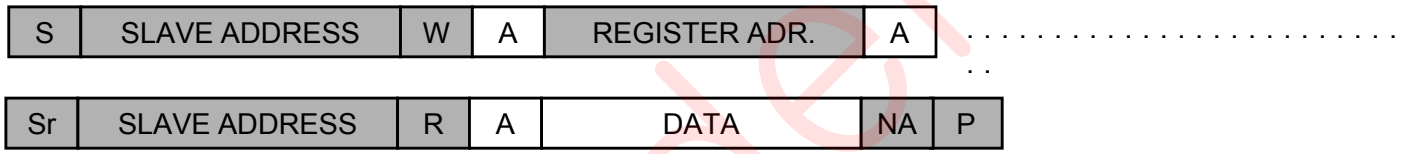
▶ 2-wire Serial Interface Functional Description

Single Write Mode operation

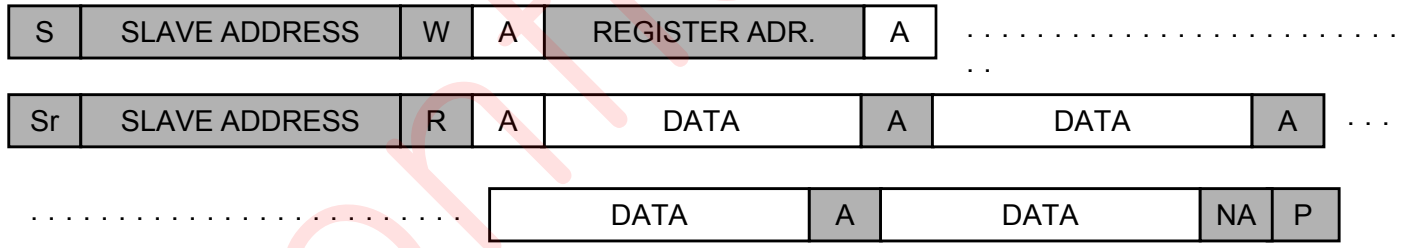
Multiple Write Mode (Register address is increased automatically)[1] operation



Single Read Mode operation



Multiple Read Mode (Register address is increased automatically)[1] operation



From master to slave From slave to master

S: Start condition. Sr : Repeated Start (Start without preceding stop.)

SLAVE ADDRESS: It can be extended 60h to 67h via CADDR0 and CADDR1 pads

CADDR[1..0]	"00"	"01"	"10"	"11"
write address	60h	62h	64h	66h(default)
read address	61h	63h	65h	67h(default)

R/W: Read/Write selection. High = read / LOW = write.
A: Acknowledge bit. NA : No Acknowledge.
DATA: 8-bit data
P: Stop condition

Note 1: Continuous writing or reading without any interrupt increases the register address automatically. If the address is increased above valid register address range, further writing does not affect the chip operation in write mode. Data from invalid registers are undefined in read mode.

▶ Register Tables (Group A)

GROUP A								
#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
0	00	DeviceID_H	16	10	00010000	RO	0	device ID
1	01	DeviceID_L	48	30	00110000	RO	0	
2	02	RevNumber	1	01	00000001	RO	0	revision number
3	03	bank	0	00	xxxxxx00	RW	5	register group selector
4	04	chip_mode	0	00	xxxxxx00	RW	7	chip mode selection : ntsc(525-line system), pal(625-line system)
5	05	mirror	0	00	xxxxxx00	RW	7	
6	06	framewidth_h	3	03	xxxx0011	RW	5	framewidth
7	07	framewidth_l	89	59	01011001	RW	5	
8	08	frameheight_h	2	02	xxxx0010	RW	5	frameheight
9	09	frameheight_l	12	0C	00001100	RW	5	
10	0A	windowx1_h	0	00	xxxxx000	RW	6	window X1 position
11	0B	windowx1_l	3	03	00000011	RW	6	
12	0C	windowy1_h	0	00	xxxxx000	RW	6	window Y1 position
13	0D	windowy1_l	1	01	00000001	RW	6	
14	0E	windowx2_h	2	02	xxxxx010	RW	6	window X2 position
15	0F	windowx2_l	130	82	10000010	RW	6	
16	10	windowy2_h	1	01	xxxxx001	RW	7	window Y2 position
17	11	windowy2_l	224	E0	11100000	RW	7	
18	12	vsyncstartrow_h	0	00	xxxxx000	RW	5	vsync start point of rcount
19	13	vsyncstartrow_l	14	0E	00001110	RW	5	
20	14	vsyncstoprow_h	1	01	xxxxx001	RW	5	vsync stop point of rcount
21	15	vsyncstoprow_l	238	EE	11101110	RW	5	
22	16	vsynccolumn_h	0	00	xxxxx000	RW	5	vsync start/stop point of ccount
23	17	vsynccolumn_l	31	1F	00011111	RW	5	
25	19	digitalgain	64	40	01000000	RW	6	digital gain
26	1A	globalgain	0	00	00000000	RW	6	globalgain
33	21	Inttime_H	0	00	00000000	RW	6	integration time
34	22	Inttime_M	128	80	10000000	RW	6	
35	23	Inttime_L	0	00	00000000	RW	6	
39	27	wb_rgain	64	40	01000000	RW	6	white balance Red gain
40	28	wb_ggain	64	40	01000000	RW	6	white balance Green gain
41	29	wb_bgain	64	40	01000000	RW	6	white balance Blue gain
49	31	analog_control_06	89	59	01011001	RW	5	analog control 06
50	32	analog_control_07	0	00	00000000	RW	5	analog control 07
51	33	analog_control_08	5	05	00000101	RW	5	analog control 08
52	34	analog_control_09	0	00	00000000	RW	5	analog control 09
53	35	pixelbias	1	01	xxxx0001	RW	5	pixel bias
54	36	compbias	15	0F	xx001111	RW	6	comparator bias
55	37	softreset	0	00	xxxxxxx0	RW	5	softreset
56	38	bayer_control_01	61	3D	00111101	RW	6	bayer control 01
62	3E	bayer_control_07	0	00	00000000	RW	5	bayer control 07
235	EB	pg_x0_h	0	00	00000000	RW	5	pg_x0_h
236	EC	pg_x0_l	0	00	00000000	RW	5	pg_x0_l
237	ED	pg_x1_h	0	00	00000000	RW	5	pg_x1_h
238	EE	pg_x1_l	0	00	00000000	RW	5	pg_x1_l
239	EF	pg_y1_h	0	00	00000000	RW	5	pg_y1_h
240	F0	pg_y1_l	0	00	00000000	RW	5	pg_y1_l
241	F1	pg_y2_h	0	00	00000000	RW	5	pg_y2_h
242	F2	pg_y2_l	0	00	00000000	RW	5	pg_y2_l
243	F3	pg_y3_h	0	00	00000000	RW	5	pg_y3_h
244	F4	pg_y3_l	0	00	00000000	RW	5	pg_y3_l
245	F5	pg_y4_h	0	00	00000000	RW	5	pg_y4_h
246	F6	pg_y4_l	0	00	00000000	RW	5	pg_y4_l
247	F7	pg_dx1	0	00	00000000	RW	5	pg_dx1
248	F8	pg_dx2	0	00	00000000	RW	5	pg_dx2
249	F9	pg_dx3	0	00	00000000	RW	5	pg_dx3
250	FA	pg_dx4	0	00	00000000	RW	5	pg_dx4
251	FB	pg_bottom_h	0	00	00000000	RW	5	
252	FC	pg_bottom_l	0	00	00000000	RW	5	
253	FD	pg_T	0	00	00000000	RW	5	line thick
254	FE	pg_bg_clamp	200	C8	11001000	RW	5	pg_background color_clamping

(Group A : continue)

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▶ Register Tables (Group B)

GROUP B								
#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
256	00	DeviceID_H	16	10	00010000	RO	0	device ID
257	01	DeviceID_L	48	30	00110000	RO	0	
258	02	RevNumber	1	1	00000001	RO	0	revision number
259	03	bank	0	00	xxxxxx00	RW	5	register group selector
260	04	isp_func_0	255	FF	11111111	RW	6	ISP control register 00
262	06	isp_func_2	96	60	01100000	RW	6	ISP control register 02
263	07	isp_func_3	203	CB	11001011	RW	6	ISP control register 03
264	08	i2c_control_1	80	50	01010000	RW	5	I2C control register 01
265	09	format	0	00	00000000	RW	6	output format control register
266	0A	format2	128	80	10000000	RW	6	output format control2 register
267	0B	sync_control_0	0	00	00000000	RW	6	Sync control 00
268	0C	sync_control_1	2	02	00000010	RW	6	Sync control 01
275	13	sync_blankEAV_f0	182	B6	10110110	RW	5	blank EAV for field0 of CCIR656 data
276	14	sync_blankSAV_f0	171	AB	10101011	RW	5	blank SAV for field0 of CCIR656 data
277	15	sync_activeEAV_f0	157	9D	10011101	RW	5	active EAV for field0 of CCIR656 data
278	16	sync_activeSAV_f0	128	80	10000000	RW	5	active SAV for field0 of CCIR656 data
279	17	sync_blankEAV_f1	241	F1	11110001	RW	5	blank EAV for field1 of CCIR656 data
280	18	sync_blankSAV_f1	236	EC	11101100	RW	5	blank SAV for field1 of CCIR656 data
281	19	sync_activeEAV_f1	218	DA	11011010	RW	5	active EAV for field1 of CCIR656 data
282	1A	sync_activeSAV_f1	199	C7	11000111	RW	5	active SAV for field1 of CCIR656 data
283	1B	sync_CCIR_FF	255	FF	11111111	RW	5	CCIR data format FFh
284	1C	sync_CCIR_00	0	00	00000000	RW	5	CCIR data format 00h
285	1D	sync_CCIR_80	128	80	10000000	RW	5	CCIR data format 80h
286	1E	sync_CCIR_10	16	10	00010000	RW	5	CCIR data format 10h
288	20	scale_x	32	20	00100000	RW	6	horizontal scale ratio (20h= x1)
289	21	scale_y	32	20	00100000	RW	7	vertical scale ratio (20h= x1)
290	22	scale_th	4	04	00000100	RW	6	scale threshold
292	24	ycontrast	64	40	01000000	RW	6	Y contrast
293	25	ybrightness	1	01	00000001	RW	6	brightness (signed value)
294	26	ymax	254	FE	11111110	RW	6	brightness max.
295	27	sephia_cb	192	C0	11000000	RW	6	Cb for sephia effect
296	28	sephia_cr	64	40	01000000	RW	6	Cr for sephia effect
302	2E	edge_gainp	36	24	00100100	RW	5	edge gain
303	2F	edge_thp	16	10	00010000	RW	5	edge threshold
314	3A	gm_y0	0	00	00000000	RW	5	gamma parameter 0
315	3B	gm_y1	12	0C	00001100	RW	5	gamma parameter 1
316	3C	gm_y2	25	19	00011001	RW	5	gamma parameter 2
317	3D	gm_y3	39	27	00100111	RW	5	gamma parameter 3
318	3E	gm_y4	52	34	00110100	RW	5	gamma parameter 4
319	3F	gm_y5	75	4B	01001011	RW	5	gamma parameter 5
320	40	gm_y6	92	5C	01011100	RW	5	gamma parameter 6
321	41	gm_y7	116	74	01110100	RW	5	gamma parameter 7
322	42	gm_y8	134	86	10000110	RW	5	gamma parameter 8
323	43	gm_y9	164	A4	10100100	RW	5	gamma parameter 9
324	44	gm_y10	186	BA	10111010	RW	5	gamma parameter 10
325	45	gm_y11	206	CE	11001110	RW	5	gamma parameter 11
326	46	gm_y12	224	E0	11100000	RW	5	gamma parameter 12
327	47	gm_y13	241	F1	11110001	RW	5	gamma parameter 13
328	48	gm_y14	255	FF	11111111	RW	5	gamma parameter 14
330	4A	lens_gainr	0	00	00000000	RW	5	Red lens gain results from Axis A,B,C
331	4B	lens_gaing1	0	00	00000000	RW	5	Gr lens gain results from Axis A,B,C
332	4C	lens_gaing2	0	00	00000000	RW	5	Gb lens gain results from Axis A,B,C
333	4D	lens_gainb	0	00	00000000	RW	5	Blue lens gain results from Axis A,B,C
334	4E	lens_coffset_h	6	06	00000110	RW	5	lens column offset (H)
335	4F	lens_coffset_l	66	42	01000010	RW	5	lens column offset (L)
336	50	lens_rx	0	00	00000000	RW	5	red lens x origin
337	51	lens_ry	0	00	00000000	RW	5	red lens y origin
338	52	lens_g1x	0	00	00000000	RW	5	green1 lens x origin
339	53	lens_g1y	0	00	00000000	RW	5	green1 lens y origin
340	54	lens_g2x	0	00	00000000	RW	5	green2lens x origin
341	55	lens_g2y	0	00	00000000	RW	5	green2 lens y origin
342	56	lens_bx	0	00	00000000	RW	5	blue lens x origin
343	57	lens_by	0	00	00000000	RW	5	blue lens y origin
344	58	lens_scale	81	51	01010001	RW	5	East/West/South/North lens scale factor
351	5F	af_cweight	7	07	xxxx0111	RW	6	auto focus center weight

(Group B : continue)

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▶ Register Tables (Group B)

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
352	00	af_cwinx1_h	1	01	xxxxxx01	RW	6	auto focus window X1
353	01	af_cwinx1_l	104	68	01101000	RW	6	
354	02	af_cwinx2_h	2	02	xxxxxx10	RW	6	auto focus window X2
355	03	af_cwinx2_l	48	30	00110000	RW	6	
356	04	af_cwiny1_h	0	00	xxxxxx00	RW	6	auto focus window Y1
357	05	af_cwiny1_l	179	B3	10110011	RW	6	
358	06	af_cwiny2_h	1	01	xxxxxx01	RW	6	auto focus window Y2
359	07	af_cwiny2_l	72	48	01001000	RW	6	
360	08	af_edge_th	0	00	00000000	RW	6	auto focus edge threshold
362	0A	tp_control_0	0	00	00000000	RW	5	test pattern control 0
363	0B	tp_control_1	255	FF	11111111	RW	5	test pattern control 1
364	0C	tp_control_2	255	FF	11111111	RW	5	test pattern control 2
365	0D	tp_control_3	255	FF	11111111	RW	5	test pattern control 3
366	0E	tp_control_4	255	FF	11111111	RW	5	test pattern control 4
374	76	flicker_control2	128	80	10000000	RW	5	flicker control 2
401	91	fdl_period_a_h	0	00	00000000	RW	5	flicker period for CASE A (H)
402	92	fdl_period_a_m	80	50	01010000	RW	5	flicker period for CASE A (M)
403	93	fdl_period_a_l	192	C0	11000000	RW	5	flicker period for CASE A (L)
404	94	fdl_period_b_h	0	00	00000000	RW	5	flicker period for CASE B (H)
405	95	fdl_period_b_m	67	43	01000011	RW	5	flicker period for CASE B (M)
406	96	fdl_period_b_l	74	4A	01001010	RW	5	flicker period for CASE B (L)
407	97	fdl_period_c_h	1	01	00000001	RW	5	flicker period for CASE C (H)
408	98	fdl_period_c_m	147	93	10010011	RW	5	flicker period for CASE C (M)
409	99	fdl_fheight_a_h	2	02	00000010	RW	5	flicker frameheight for CASE A (H)
410	9A	fdl_fheight_a_l	12	0C	00001100	RW	5	flicker frameheight for CASE A (L)
411	9B	fdl_fheight_b_h	2	02	00000010	RW	5	flicker frameheight for CASE B (H)
412	9C	fdl_fheight_b_l	12	0C	00001100	RW	5	flicker frameheight for CASE B (L)
420	A4	enc_control	0	00	00000000	RW	5	encoder control
421	A5	enc_scfreq	0	00	xxxxxx00	RW	5	subcarrier freqency selection for which TV mode
422	A6	enc_sync	16	10	00010000	RW	5	sync level
423	A7	enc_blankH	0	00	00000000	RW	5	blank level
424	A8	enc_blankL	240	F0	11110000	RW	5	
425	A9	enc_pedestal	42	2A	00101010	RW	5	pedestal
426	AA	enc_burst	112	70	01110000	RW	5	burst amplitude
427	AB	enc_Ygain	130	82	10000010	RW	5	Y convergence gain from YCbCr to YUV
428	AC	enc_Ugain	111	6F	01101111	RW	5	U convergence gain from YCbCr to YUV
429	AD	enc_Vgain	156	9C	10011100	RW	5	V convergence gain from YCbCr to YUV
430	AE	enc_Yrange_H	3	03	xxxxx011	RW	5	max. luminance
431	AF	enc_Yrange_L	32	20	00100000	RW	5	
432	B0	enc_Crange_H	1	01	xxxxx001	RW	5	max. amplitudes of chrominance
433	B1	enc_Crange_L	72	48	01001000	RW	5	
434	B2	enc_chroma_max_H	3	03	xxxxx011	RW	5	maximum chrominance of composite output
435	B3	enc_chroma_max_L	205	CD	11001101	RW	5	
436	B4	enc_chroma_min_H	0	00	xxxxx000	RW	5	minmum chrominance of composite output
437	B5	enc_chroma_min_L	109	6D	01101101	RW	5	
473	D9	burst_toffset	0	00	00000000	RW	5	burst time +/- offset
485	E5	md_yth	64	40	01000000	RW	5	Y threshold for motion detection
486	E6	md_diff	64	40	01000000	RW	5	difference for motion detection
487	E7	md_interval	8	08	00001000	RW	5	intervals of frames used for motion detection
489	E9	md_section7	255	FF	11111111	RW	5	image section 7 for motion detection
490	EA	md_section6	255	FF	11111111	RW	5	image section 6 for motion detection
491	EB	md_section5	255	FF	11111111	RW	5	image section 5 for motion detection
492	EC	md_section4	255	FF	11111111	RW	5	image section 4 for motion detection
493	ED	md_section3	255	FF	11111111	RW	5	image section 3 for motion detection
494	EE	md_section2	255	FF	11111111	RW	5	image section 2 for motion detection
495	EF	md_section1	255	FF	11111111	RW	5	image section 1 for motion detection
496	F0	md_section0	255	FF	11111111	RW	5	image section 0 for motion detection

(Group B : continue)

▶ Register Tables (Group C)

GROUP C								
#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
512	00	DeviceID_H	16	10	00010000	RO	0	device ID
513	01	DeviceID_L	48	30	00110000	RO	0	
514	02	RevNumber	1	01	00000001	RO	0	revision number
515	03	bank	0	00	xxxxxx00	RW	5	register group selector
516	04	auto_control_1	152	98	10011000	RW	0	auto control 01
518	06	auto_control_3	144	90	10010000	RW	0	auto control 03
519	07	ext_intime_h	0	00	00000000	RW	0	external intime
520	08	ext_intime_m	128	80	10000000	RW	0	
521	09	ext_intime_l	0	00	00000000	RW	0	
522	0A	ext_glbg_h	1	01	00000001	RW	0	external linear global gain
523	0B	ext_glbg_l	0	00	00000000	RW	0	
524	0C	exposure_t	0	00	00000000	RW	0	exposure
525	0D	exposure_h	0	00	00000000	RW	0	
526	0E	exposure_m	128	80	10000000	RW	0	
527	0F	exposure_l	0	00	00000000	RW	0	
528	10	expFrmH_H	2	02	00000010	RW	5	frame height for exposure
529	11	expFrmH_L	12	0C	00001100	RW	5	
530	12	midfrmheight_h	2	02	00000010	RW	5	mid frame height for exposure
531	13	midfrmheight_l	12	0C	00001100	RW	5	
532	14	maxfrmheight_h	2	02	00000010	RW	5	max frame height for exposure
533	15	maxfrmheight_l	12	0C	00001100	RW	5	
534	16	minexp_h	0	00	00000000	RW	5	minimum exposure
535	17	minexp_m	0	00	00000000	RW	5	
536	18	minexp_l	12	0C	00001100	RW	5	
537	19	midexp_t	0	00	00000000	RW	5	mid-exposure point
538	1A	midexp_h	65	41	01000001	RW	5	
539	1B	midexp_m	159	9F	10011111	RW	5	
540	1C	maxexp_t	0	00	00000000	RW	5	maximum exposure
541	1D	maxexp_h	65	41	01000001	RW	5	
542	1E	maxexp_m	159	9F	10011111	RW	5	
549	25	ae_c_weight	3	03	00000011	RW	0	AE center weight
550	26	ae_up_speed	8	08	00001000	RW	0	AE upside speed
551	27	ae_down_speed	12	0C	00001100	RW	0	AE downside speed
552	28	ae_lock	10	0A	00001010	RW	0	AE lock
564	34	user_wyt	128	80	10000000	RW	0	user weight Y target
590	4E	ae_winx_h	0	00	00000000	RW	5	AE window start X point
591	4F	ae_winx_l	26	1A	00011010	RW	5	
592	50	ae_winy_h	0	00	00000000	RW	5	AE window start Y point
593	51	ae_winy_l	14	0E	00001110	RW	5	
594	52	ae_width_h	2	02	00000010	RW	5	AE window width
595	53	ae_width_l	108	6C	01101100	RW	5	
596	54	ae_height_h	1	01	00000001	RW	5	AE window height
597	55	ae_height_l	196	C4	11000100	RW	5	
598	56	ae_cwinx_h	0	00	00000000	RW	5	AE center window start X point
599	57	ae_cwinx_l	210	D2	11010010	RW	5	
600	58	ae_cwiny_h	0	00	00000000	RW	5	AE center window start Y point
601	59	ae_cwiny_l	151	97	10010111	RW	5	
602	5A	ae_cwidth_h	0	00	00000000	RW	5	AE center window width
603	5B	ae_cwidth_l	200	C8	11001000	RW	5	
604	5C	ae_cheight_h	0	00	00000000	RW	5	AE center window height
605	5D	ae_cheight_l	150	96	10010110	RW	5	
606	5A	awb_winx1_h	0	00	00000000	RW	5	AWB window start X point
607	5B	awb_winx1_l	124	7C	01111100	RW	5	
608	5C	awb_winy1_h	0	00	00000000	RW	5	AWB window start Y point
609	5D	awb_winy1_l	46	2E	00101110	RW	5	
610	5E	awb_winx2_h	3	03	00000011	RW	5	AWB window end X point
611	5F	awb_winx2_l	0	00	00000000	RW	5	
612	A0	awb_winy2_h	1	01	00000001	RW	5	AWB window end Y point
613	A1	awb_winy2_l	202	CA	11001010	RW	5	
614	A2	awb_deltax	0	00	00000000	RW	5	AWB deltaX
615	A3	awb_deltay	0	00	00000000	RW	5	AWB deltaY
616	A4	awb_rgratio	128	80	10000000	RW	5	AWB R-G ratio
617	A5	awb_bgratio	128	80	10000000	RW	5	AWB B-G ratio
618	A6	awb_lock	2	02	00000010	RW	5	AWB lock
619	A7	awb_speed	8	08	00001000	RW	5	AWB speed

(Group C : continue)

1/4 inch VGA class Analog/Digital Output NTSC/PAL CMOS Image Sensor

▶ Register Tables (Group C)

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
697	B9	cc11	57	39	00111001	RW	5	Color correction matrix (1 , 1)
698	BA	cc12	145	91	10010001	RW	5	Color correction matrix (1 , 2)
699	BB	cc13	135	87	10000111	RW	5	Color correction matrix (1 , 3)
700	BC	cc21	142	8E	10001110	RW	5	Color correction matrix (2 , 1)
701	BD	cc22	59	3B	00111011	RW	5	Color correction matrix (2 , 2)
702	BE	cc23	141	8D	10001101	RW	5	Color correction matrix (2 , 3)
703	BF	cc31	129	81	10000001	RW	5	Color correction matrix (3 , 1)
704	C0	cc32	153	99	10011001	RW	5	Color correction matrix (3 , 2)
705	C1	cc33	59	3B	00111011	RW	5	Color correction matrix (3 , 3)
748	EC	led_th1_t	0	00	00000000	RW	5	
749	ED	led_th1_h	0	00	00000000	RW	5	
750	EE	led_th1_m	0	00	00000000	RW	5	
751	EF	led_th2_t	0	00	00000000	RW	5	
752	F0	led_th2_h	0	00	00000000	RW	5	
753	F1	led_th2_m	0	00	00000000	RW	5	
754	F2	led_th3_t	0	00	00000000	RW	5	
755	F3	led_th3_h	0	00	00000000	RW	5	
756	F4	led_th3_m	0	00	00000000	RW	5	
757	F5	led_th4_t	0	00	00000000	RW	5	
758	F6	led_th4_h	0	00	00000000	RW	5	
759	F7	led_th4_m	0	00	00000000	RW	5	
761	F9	user_cs	32	20	00100000	RW	5	

(Group C : continue)

1/4 inch VGA class Analog/Digital Output NTSC/PAL CMOS Image Sensor

▶ Register Tables (Group D)

GROUP D								
#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
768	00	DeviceID_H	16	10	00010000	RO	0	device ID
769	01	DeviceID_L	48	30	00110000	RO	0	
770	02	RevNumber	1	01	00000001	RO	0	revision number
771	03	bank	0	00	xxxxxx00	RW	5	register group selector
830	3E	af_edge_sum_4	0	0		RO	0	edge data for auto focus(T)
831	3F	af_edge_sum_3	0	0		RO	0	edge data for auto focus(H)
832	40	af_edge_sum_2	0	0		RO	0	edge data for auto focus(M)
833	41	af_edge_sum_1	0	0		RO	0	edge data for auto focus(L)

(Group D : continue)

▶ Register Tables (Detailed) : Group A

Register names are written in *slanted* characters. To differentiate between decimal, binary, and hexa numbers, (d, b, and h) are appended. The sensor should be reset by RSTB pin set low, after power is up, for at least 16 master clock periods. And then all read-write registers are initialized by internal ROM for about 3 ms. So we recommend you to write data to registers after initialization.

(0-3) DeviceID, RevNumber, Register Selector

GROUP A								
#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
0	00	DeviceID_H	16	10	00010000	RO	0	device ID
1	01	DeviceID_L	48	30	00110000	RO	0	
2	02	RevNumber	1	01	00000001	RO	0	revision number
3	03	bank	0	00	xxxxxx00	RW	5	register group selector

Default : 00h(Device_ID_H) = 10h,
01h(Device_ID_L) = 30h,
02h(Rev_Number) = 00h,
03h(Register Selector)= 00h.

Description :

Indicates device ID, reversion number, Register Select.
Common registers of Group A(00h) / B(01h) / C(02h) / D(03h).

Register type
RO : Available Read Only
RW : Available Read and Write

< Group A >

(4) Chip mode

< Group A >

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
4	4	chip_mode	U	U	000000UU	RW	7	chip mode selection

Default : 04h = Variable according to wire-strapping

Description :

register name : chip_mode								
register #	bit#	name	default	U	default(h)	0U	default(b)	000000UU
04(d) 04(h)	7	x	0					
	6	x	0					
	5	x	0					
	4	x	0					
	3	x	0					
	2	x	0					
	1	chip_mode	U	Chip mode selection "00" - NTSC, (M)PAL "01"- PAL Else – VGA digital output only				
	0		U					

Chip_mode(1 : 0) : chip mode selection

The default value of this register is changed by wire-strapping under RESET='0'(HW/SW reset).

After reset, the register can be set with other values through SSCLK and SSDAT.

(5) Mirror

< Group A >

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
5	5	mirror	U	U	000000UU	RW	6	mirror mode selection

Default : 05h = Variable according to wire-strapping

Description :

register name : chip_mode								
register #	bit#	name	default	U	default(h)	0U	default(b)	000000UU
05(d) 05(h)	7	x	0					
	6	x	0					
	5	x	0					
	4	x	0					
	3	x	0					
	2	x	0					
	1	vm	U	vertical mirror ON/OFF				
	0	hm	U	horizontal mirror ON/OFF				

Mirror (1 : 0) : Vertical/Horizontal mirror

The default value of this register is changed by wire-strapping under RESET='0'(HW/SW reset).

After reset, the register can be set with other values through SSCLK and SSDAT.

(6-7) FrameWidth

< Group A >

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
6	6	framewidth_h	U	U	UUUUUUUU	RW	5	framewidth (H)
7	7	framewidth_l	U	U	UUUUUUUU	RW	5	framewidth (L)

Default : Variable according to wire-strapping

Description :

FrameWidth is the number of columns to be counted during one line time. Column counter value is incremented 1 by 1 until it reaches *FrameWidth*, then it is reset to 0.

Usage:

NTSC/NTSC-J/(M) PAL : 0359h

(B, D, G, H, I, N, Nc) PAL : 040Dh

VGA digital output only : 0359h

(8-9) FrameHeight

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
8	8	frameheight_h	2	02	00000010	RW	5	frameheight (H)
9	9	frameheight_l	U	U	UUUUUUUU	RW	5	frameheight (L)

Default : 08h = 02h, 09h = Variable according to wire-strapping

Description :

FrameHeight is the number of rows to be counted during one frame time. Row counter value is incremented 1 by 1 until it reaches *FrameHeight*, then it is reset to 0.

Usage:

NTSC/NTSC-J/(M) PAL : 020Ch

(B, D, G, H, I, N, Nc) PAL : 0207h

VGA digital output only : 020Ch

(10-17) WindowX / Y

< Group A >

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
10	0A	windowx1_h	0	00	00000000	RW	6	window X1 (H)
11	0B	windowx1_l	3	03	00000011	RW	6	window X1 (L)
12	0C	windowy1_h	0	00	00000000	RW	6	window Y1 (H)
13	0D	windowy1_l	1	01	00000001	RW	6	window Y1 (L)
14	0E	windowx2_h	2	02	00000010	RW	6	window X2 (H)
15	0F	windowx2_l	130	82	10000010	RW	6	window X2 (L)
16	10	windowy2_h	U	UU	00000UUU	RW	7	window Y2 (H)
17	11	windowy2_l	U	UU	UUUUUUUU	RW	7	window Y2 (L)

Default : 0Ah = 00h, 0Bh = 03h, 0Ch = 00h, 0Dh = 01h, 0Eh = 02h, 0Fh = 82h,
10h / 11h = Variable according to wire-strapping

Description :

Window can be defined by 4 parameters : *WindowX1, WindowY1, WindowX2*, and *WindowY2.* Serial image data stream out pixel by pixel. Window specifies the area of pixels that we are interested in. Hsync signal indicates if the image data output is from a pixel that lies within the window area or not. Output data stream does not stop for pixels lying outside the window : just the Hsync signal is de-asserted.

The actual window position in the frame is given as

upper right corner = (*Window X1 + 1*, *Window Y1*)

lower left corner = (*Window X2*, *Window Y2 - 1*)

All the coordinates are with respect to the maximum window origin (0, 0) of [Fig. 3]. Window position and size are with respect to the full sampling mode. It is not necessary to change the window parameters when sampling mode is switched between one and another.

(18-21) VsyncStartrow / VsyncStoprow

< Group A >

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
18	12	vsyncstartrow_h	0	00	00000000	RW	5	Output Vsync Row Start (H)
19	13	vsyncstartrow_l	14	0E	00001110	RW	5	Output Vsync Row Start (L)
20	14	vsyncstoprow_h	1	01	00000001	RW	5	Output Vsync Row Stop (H)
21	15	vsyncstoprow_l	238	EE	11101110	RW	5	Output Vsync Row Stop (L)

Default : 12h = 00h, 13h = 0Eh, 14h = 01h, 15h = EEh

Description :

VsyncStartRow: Output Vsync Row Start points

VsyncStopRow: Output Vsync Row Stop points

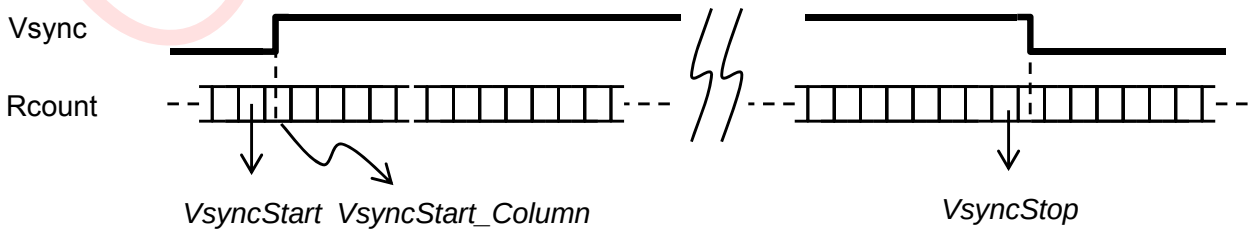
(22-23) VsyncColumn

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
22	16	vsynccolumn_h	0	00	00000000	RW	5	Output Vsync Column Start (H)
23	17	vsynccolumn_l	31	1F	00010000	RW	5	Output Vsync Column Start (L)

Default : 16h = 00h, 17h = 1Fh

Description :

VsyncColumn: Output Vsync Column start points



< Group A >

(25) Digital Gain

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
25	19	digitalgain	64	40	01000000	RW	6	Digital Gain

Default : 19h = 40h

Description :

Digital Gain

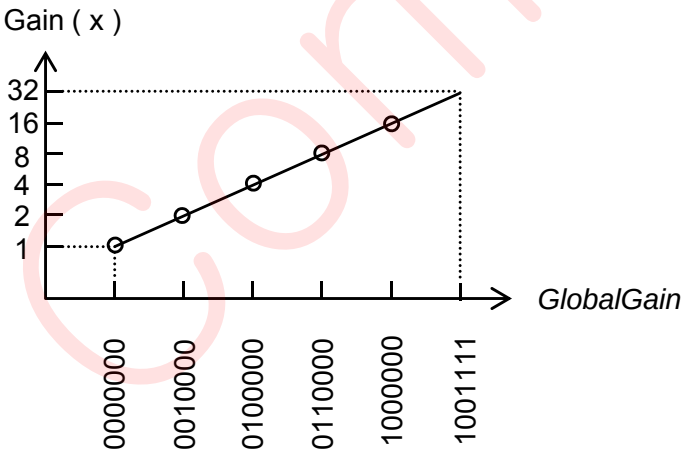
(26-27) Globalgain

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
26	1A	globalgain	0	00	00000000	RW	6	Globalgain(Globalgain for odd frame at dual exposure mode)

Default : 1Ah = 00h

Description :

GlobalGain has effect on all of R, G, and B pixel outputs. Raw R, G, B data are amplified by a common factor of *GlobalGain*. The relation between *GlobalGain* and amplification factor is shown in the picture below.



Maximum value of *GlobalGain* is 1001111. Gain factors for *GlobalGain* larger than or equal to 1010000 are not defined.

(33-38) Integration Time

< Group A >

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
33	21	inttime_H	0	00	00000000	RW	6	Integration Time (H)
34	22	inttime_M	128	80	10000000	RW	6	Integration Time (M)
35	23	inttime_L	0	00	00000000	RW	6	Integration Time (L)

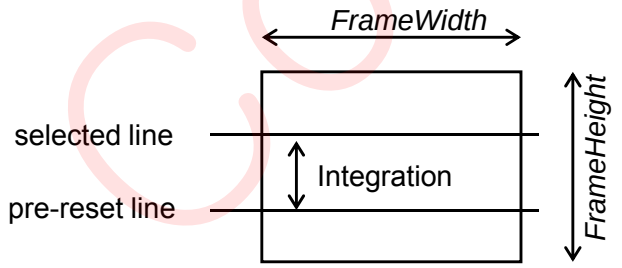
Default : 21h = 00h, 22h = 80h, 23h = 00h

Description :

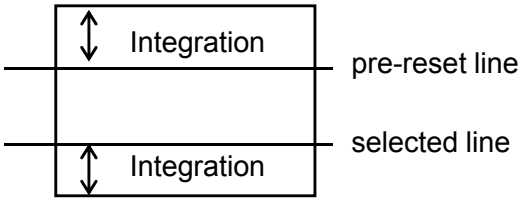
There are 3 bytes of registers to control the photo-charge accumulation interval for each pixel. 4Ch and 4Dh registers indicate how many line times the integration will continue until they are all reset. 4Eh register further sub-divide one line time into 256 smaller intervals. Total integration time is the sum of the integral multiple and fractional parts of one line time.

As the row counter value is incremented from 0 to *FrameHeight*, each line relevant to the row count is selected and all pixel data of that line is read out all at once. The read- out operation involves pixel reset pulses, so all pixels that are selected and read out are reset to initial states.

To control exposure time, there runs another counter to select and reset a line other than the one that is selected to be read out. The space between the two lines is equal to the number of integration lines. There are two possible situations concerning the position of selected line and reset line. The 1st case is where the pre-reset counter runs ahead of read-out counter. And the other case Is just the reverse of the 1st one. The number of integration lines is different for the two cases as is shown in the left figures. Since the basic unit of integration time for PC1030N is 1/ 256 line time, it is easy to implement Auto Exposure algorithms without worrying about strong light environment where the image may change abruptly in brightness or it may even blink.



Case 1. Reset line preceding select line



Case 2. Select line preceding reset line

(39-43) White Balance R/G/B gain

< Group A >

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
39	27	wb_rgain	64	40	01000000	RW	6	Red gain for white balance
40	28	wb_ggain	64	40	01000000	RW	6	Green gain for white balance
41	29	wb_bgain	64	40	01000000	RW	6	Blue gain for white balance

Default : 27h = 40h, 28h = 40h, 29h = 40h

Description :

White Balance Red gain :

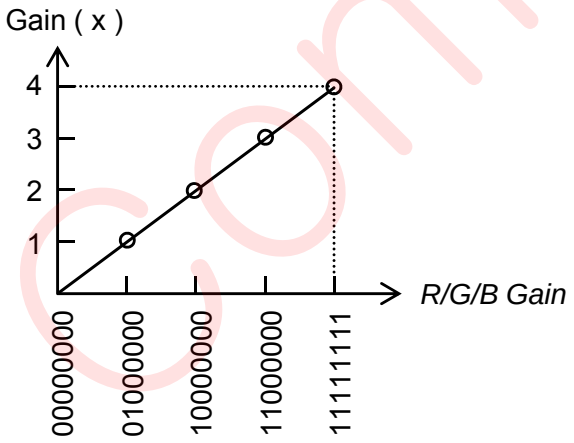
RedGain is the multiplication factor for red pixel output. Total gain factor for red pixels is (gain from *GlobalGain*) * (gain from *RedGain*).

White Balance Green gain :

G1/G2 pixels are those green pixels whose nearest neighbors are red pixels or blue pixels.

White Balance Blue gain :

BlueGain is similar to *RedGain*.



R / G / B gain can be used for white balance control. Bit7 of *R/G/B Gain* is weighted by 2, bit6 by 1 and the other consecutive bits are weighted by 1/2, 1/4, 1/8, … respectively. That is, *R/G/B gain* is a binary number with decimal point between bit6 and bit5.

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< Group A >

(49) Analog control 06

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
49	31	analog_control_06	89	59	01011001	RW	5	analog control register 06

Default : 31h = 59h

Description :

register name : analog_control_06								
register #	bit#	name	default	**89**	default(h)	**59**	default(b)	**01011001**
49(d) 31(h)	7	Reserved	0					
	6		1					
	5	pad_drivability	0	Data & VSYNC PAD pad drivability control register				
	4		1					
	3	Reserved	1					
	2		0					
	1		0					
	0	Reserved	1					

(50) Analog control 07

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
50	32	analog_control_07	0	00	00000000	RW	5	analog control register 07

Default : 32h = 00h

Description :

register name : analog_control_07								
register #	bit#	name	default	**0**	default(h)	**00**	default(b)	**00000000**
50(d) 32(h)	7	motion_pad_en	0	motion output pad enable				
	6	Reserved	0					
	5	dac_pd	0	DAC power down				
	4	Reserved	0					
	3		0					
	2	Reserved	0					
	1	Reserved	0					
	0	Reserved	0					

< Group A >

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(51) Analog control 08

< Group A >

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
51	33	analog_control_08	5	5	00000101	RW	5	analog control register 08

Default : 33h = 05h

Description :

register name : analog_control_08								
register #	bit#	name	default	5	default(h)	05	default(b)	00000101
51(d) 33(h)	7	ledctl_en	0	LEDCTL pad enable				
	6	ledctl_drv	0	LEDCTL pad drivability				
	5		0					
	4	Reserved	0					
	3	hsync_drv	0	hsync pad drivability				
	2		1					
	1	pclk_drv	0	pclk pad drivability				
	0		1					

(52) Analog control 09

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
52	34	analog_control_09	0	0	00000000	RW	5	analog control register 09

Default : 34h = 00h

Description :

register name : analog_control_09								
register #	bit#	name	default	0	default(h)	00	default(b)	00000000
52(d) 34(h)	7	pclk_delay	0	output pixel clock delay 000 : no delay 001b : 2.5ns 010b : 5ns 011b : 7.5ns 100b : 10ns 101b : 12.5ns 110b : 15ns 111b : 17.5ns				
	6		0					
	5		0					
	4	Reserved	0					
	3	Reserved	0					
	2	Reserved	0					
	1	Reserved	0					
	0	Reserved	0					

< Group A >

< Group A >

(53) PixelBias

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
53	35	pixelbias	1	01	00000001	RW	5	pixel bias

Default : 20h = 01h

Description :

Pixel array has a source follower circuit for each column to buffer the photo-diode signal voltage. The source follower bias current is determined as an integral multiple of 1uA.

Ipixel = *PixelBias* * 1uA

(54) CompBias

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
54	36	compbias	15	0F	00001111	RW	5	compbias

Default : 36h = 0Fh

Description :

Comparator amp bias

(55) Soft reset

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
55	37	soft_reset	0	00	xxxxxxx0	RW	5	software reset

Default : 37h = 00h

Description :

soft_reset(0) : Software reset bit

(57) Bayer Control 02

< Group A >

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
57	39	bayer_control_02	240	F0	11110000	RW	6	bayer control register 02

Default : 39h = F0h

Description :

register name : bayer_control_02								
register #	bit#	name	default	**240**	default(h)	**F0**	default(b)	**11110000**
57(d) 39(h)	7	clkdiv(2:0)	1	**Pixel Clock Divide** 000b : master clock x 1/2 001b : master clock x 1/3 010b : master clock x 1/4 011b : master clock x 1/6 100b : master clock x 1/8 101b : master clock x 1/16 111b : master clock x 1 (default) – for NTSC / PAL				
	6		1					
	5		1					
	4	Reserved	1					
	3	Reserved	0					
	2	Reserved	0					
	1	Reserved	0					
	0	Reserved	0					

(62) Bayer Control 07

< Group A >

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
62	3E	bayer_control_07	0	00	00000000	RW	5	bayer control register 07

Default : 3Eh = 00h

Description :

register name : bayer_control_07								
register #	bit#	Name	default	0	default(h)	00	default(b)	00000000
62(d) 3E(h)	7	Reserved	0					
	6	Reserved	0					
	5	frmvar_en	0	**Variable Frame rate mode** '0' : disable '1' : enable (for VGA digital output only)				
	4	Reserved	0					
	3		0					
	2		0					
	1		0					
	0		0					

(235 - 254) Parking_guide

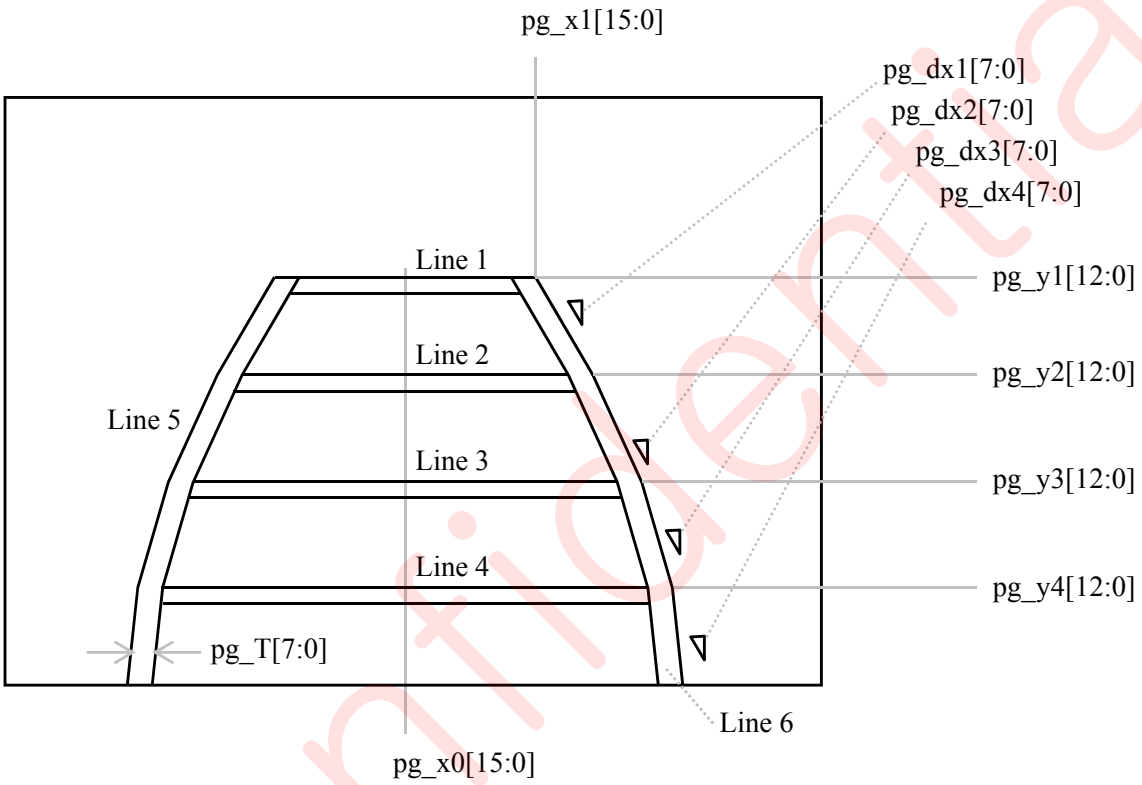
< Group A >

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
235	EB	pg_x0_h	0	00	00000000	RW	5	Horizontal Center position
236	EC	pg_x0_l	0	00	00000000	RW	5	
237	ED	pg_x1_h	0	00	00000000	RW	5	Honrizontal Distance from Horizontal Center
238	EE	pg_x1_l	0	00	00000000	RW	5	
239	EF	pg_y1_h	0	00	00000000	RW	5	Vertical position of Horizontal Line 1
240	F0	pg_y1_l	0	00	00000000	RW	5	
241	F1	pg_y2_h	0	00	00000000	RW	5	Vertical position of Horizontal Line 2
242	F2	pg_y2_l	0	00	00000000	RW	5	
243	F3	pg_y3_h	0	00	00000000	RW	5	Vertical position of Horizontal Line 3
244	F4	pg_y3_l	0	00	00000000	RW	5	
245	F5	pg_y4_h	0	00	00000000	RW	5	Vertical position of Horizontal Line 4
246	F6	pg_y4_l	0	00	00000000	RW	5	
247	F7	pg_dx1	0	00	00000000	RW	5	Slope of Horizontal Line 1 to Line2
248	F8	pg_dx2	0	00	00000000	RW	5	Slope of Horizontal Line 2 to Line3
249	F9	pg_dx3	0	00	00000000	RW	5	Slope of Horizontal Line 3 to Line4
250	FA	pg_dx4	0	00	00000000	RW	5	Slope of Horizontal Line 4 to End line
251	FB	pg_bottom_h	0	00	00000000	RW	5	Bottom Limit of Parking guide
252	FC	pg_bottom_l	0	00	00000000	RW	5	
253	FD	pg_T	0	00	00000000	RW	5	Parking guide Line Thick
254	FE	pg_bg_clamp	200	C8	11001000	RW	5	Transparency of parking guide line

Default : EBh = 00h, EAh = 00h, EBh = 00h, ECh = 00h, EDh = 00h, ECh = 00h, EEh = 00h,
EFh = 00h, F0h = 00h, F1h = 00h, F2h = 00h, F3h = 00h, F4h = 00h, F5h = 00h, F6h = 00h,
F7h = 00h, F8h = 00h, F9h = 00h, FAh = 00h, FBh = 00h, FCh = 00h, FDh = 00h, FEh = C8h

Description :

pg_x0 : Horizontal Center position
pg_x1 : Horizontal Distance form Horizontal Center
pg_y1[12:0] : Vertical Position of Horizontal Line 1
pg_y2[12:0] : Vertical Position of Horizontal Line 2
pg_y3[12:0] : Vertical Position of Horizontal Line 3
pg_y4[12:0] : Vertical Position of Horizontal Line 4
pg_y1[15:13] : Color of Line 1, Line 5 and Line 6 (show next page)
([15] – Red, [14] – Green, [13] – Blue)
pg_y2[15:13] : Color of Line 2 ([15] – Red, [14] – Green, [13] – Blue)
pg_y3[15:13] : Color of Line 3 ([15] – Red, [14] – Green, [13] – Blue)
pg_y4[15:13] : Color of Line 4 ([15] – Red, [14] – Green, [13] – Blue)
pg_dx1 : slope of Horizontal Line 1 to Line 2
pg_dx2 : slope of Horizontal Line 2 to Line 3
pg_dx3 : slope of Horizontal Line 3 to Line 4
pg_dx4 : slope of Horizontal Line 4 to End Line
pg_bottom : bottom limit of Parking guide
pg_T : Line Thickness
pg_bg_clamp : Transparency of parking guide line



[Fig] Parking guide Diagram

▶ Register Tables (Detailed) : Group B

(260) ISP Function Control 0

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
260	4	isp_func_0	255	FF	11111111	RW	6	ISP control register 00

Default : 04h = FFh

Description :

register name : isp_function_control_00								
register #	bit#	name	default	255	default(h)	FF	default(b)	11111111
260(d) 04(h)	7	ccr_en	1	**Color Correction** '0' : Color correction disable '1' : Color correction enable (default)				
	6	Reserved	1					
	5	lpf_en	1	**Low Pass Filter** '0' : Disable. '1' : Enable. (default)				
	4	Reserved	1					
	3	Reserved	1					
	2	edge_en	1	**Edge Enhancement** '0' : Disable '1' : Enable (default)				
	1	Reserved	1					
	0	Reserved	1					

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(262) ISP Function Control 2

< Group B >

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
262	6	isp_func_2	96	60	01100000	RW	6	ISP control register 02

Default : 06h = 60h

Description :

register name : isp_function_control_02								
register #	bit#	name	default	96	default(h)	60	default(b)	01100000
262(d) 06(h)	7	sephia_en	0	**Sephia** '0' : Disable (default) '1' : Enable				
	6	Reserved	1					
	5	Reserved	1					
	4	parking_guide_en	0	**Parking guide enable** '0' : Disable (default) '1' : Enable				
	3	reverse	0	**Reverse (reg_ae_ysel='3', Y601 selection)** '0' : Disable (default) '1' : Enable				
		Reserved	0					
	1		0					
	0	lens_en	0	**Lens Shading Enable** '0' : Disable '1' : Enable (default)				

(263) ISP Function Control 3

< Group B >

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
263	7	isp_func_3	203	CB	11001011	RW	6	ISP control register 03

Default : 07h = CBh

Description :

register name : isp_function_control_03								
register #	bit#	name	default	216	default(h)	D8	default(b)	11011000
263(d) 07(h)	7	Reserved	1					
	6		1					
	5	Reserved	0					
	4		0					
	3	gm_en	1	Gamma Correction '0' : Disable '1' : Enable (defualt)				
	2	Reserved	0					
	1	Reserved	1					
	0	Reserved	1					

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(264) I2C control 1

< Group B >

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
264	8	i2c_control_1	80	50	01010000	RW	5	I2C control register 01

Default : 08h = 50h

Description :

register name : i2c_control_1								
register #	bit#	name	default	80	default(h)	50	default(b)	01010000
264(d) 08(h)	7	Reserved	0					
	6		1					
	5		0					
	4		1					
	3	Reserved	0					
	2	clkoff	0	**Clock kill control register** '0' : Clock kill disable (default) '1' : Clock kill enable				
	1	stdby	0	**Register standby mode** '0' : Off (default) '1' : On				
	0	dout_en	0	**Digital data output enable** '0' : Disable (default) '1' : Enable				

(265) Format

< Group B >

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
265	9	format	0	00	00000000	RW	2	Output Format control register

Default : 09h = 00h

Description :

register name : format_control								
register #	bit#	name	default	**0**	default(h)	**00**	default(b)	**00000000**
265(d) 09(h)	7	format_control	0	0 : CB Y CR Y 1 : CR Y CB Y 2 : Y CB Y CR 3 : Y CR Y CB 4 : RGRG...GBGB, Raw Bayer 5 : GBGB...RGRG, Raw Bayer 6 : GRGR...BGBG, Raw Bayer 7 : BGBG...GRGR, Raw Bayer 12 : mono Sensor 13 : YYYY				
	6		0					
	5		0					
	4		0					
	3		0					
	2		0					
	1		0					
	0		0					

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(266) Format2

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
266	A	format2	0	00	00000000	RW	6	Output Format2 control register

Default : 0Ah = 00h

Description :

register name : format2								
register #	bit#	name	default	**0**	default(h)	**00**	default(b)	**00000000**
266(d) 0A(h)	7	dout_select	1	"01" - CCIR656 interlaced, "10" – 320x240 (320x288), Else – VGA digital output only				
	6		0					
	5	Reserved	0					
	4	Reserved	0					
	3	dout_field_mode	0	select 320x240(288) digital output (even or odd : default=odd)				
	2	Reserved	0					
	1	Reserved	0					
	0	Reserved	0					

dout_select :

"01b" – ITU-R BT656(CCIR656) interlaced format output.

"10b" – i) Horizontal sub-sampled YCbCr422 and one field output among odd and even fields concurrent with analog composite(27MHz master clock) at 4d ≤ Format register ≤

else – VGA digital output only

dout_field_mode (for 320x240(288)) :

'0' – odd field selected

'1' – even field selected

(267) Sync control 0

< Group B >

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
267	0B	sync_control_0	0	00	00000000	RW	6	Synchronization control register 00

Default : 0Bh = 00h

Description :

register name : sync_control_00								
register #	bit#	name	default	0	default(h)	00	default(b)	00000000
267(d) 0B(h)	7	Reserved	0					
	6	sync_drop[1:0]	0	**Vsync Drop (VD), sync_drop[1]** '0' : disable. (default) '1' : enable. **Hsync Drop (HD), sync_drop[0]** '0' : disable. (default) '1' : enable.				
	5		0					
	4	sync_pclkrate	0	**pclk rate control**				
	3		0					
	2		0					
	1		0					
	0		0					

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(268) Sync control 1

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
268	0C	sync_control_1	2	02	00000010	RW	6	Synchronization control register 01

Default : 0Ch = 02h

Description :

register name : sync_control_01								
register #	bit#	name	default	2	default(h)	02	default(b)	00000010
268(d) 0C(h)	7	hiz	0	**Output Pad set to Hi Impedance (HiZ)** '0' : disable. (default) '1' : enable.				
	6	sync_vsyncPolarity	0	**Vsync Polarity Change** '0' : disable. (default) '1' : enable.				
	5	sync_hsyncAllLines	0	**Active High of Hsync All Lines** '0' : Disable. (default) '1' : Enable.				
	4	sync_hsyncPolarity	0	**Hsync Polarity Change** '0' : Disable. (default) '1' : Enable.				
	3	sync_pclkwindow	0	**PCLK Window** '0' : Disable. (default) '1' : Enable.				
	2	sync_pclkPolarity	0	**PCLK Polarity** '0' : Disable. (default) '1' : Enable.				
	1	stdbyLevel	1	**Stand by Level** '0' : Output level in stand by mode. (default) '1' : Hiz in stand by mode.				
	0	Reserved	0					

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(275-282) CCIR656 Sync Index Value

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
275	13	sync_blankEAV_f0	182	B6	10110110	RW	5	blank EAV of field0(odd) or blank EAV of frame
276	14	sync_blankSAV_f0	171	AB	10101011	RW	5	blank SAV of field0(odd) or blank SAV of frame
277	15	sync_activEAV_f0	157	9D	10011101	RW	5	active EAV of field0(odd) or active EAV of frame
278	16	sync_activSAV_f0	128	80	10000000	RW	5	active SAV of field0(odd) or active SAV of frame
279	17	sync_blankEAV_f1	241	F1	11110001	RW	5	blank EAV of field1(even)
280	18	sync_blankSAV_f1	236	EC	11101100	RW	5	blank SAV of field1(even)
281	19	sync_activEAV_f1	218	DA	11011010	RW	5	active EAV of field1(even)
282	1A	sync_activSAV_f1	199	C7	11000111	RW	5	active SAV of field1(even)

Default : 13h = B6h, 14h = ABh, 15h = 9Dh, 16h = 80h, 17h = F1h, 18h = ECh, 19h = DAh, 1Ah = C7h

Description :

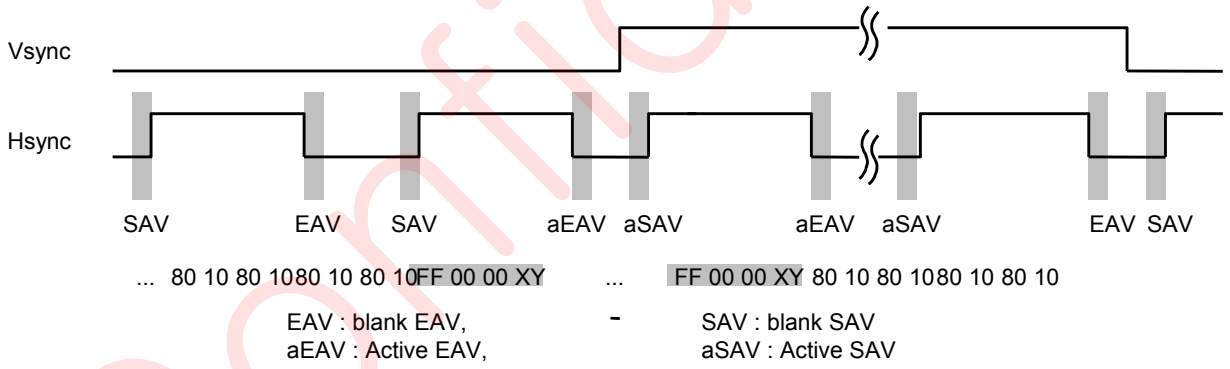
EAV and SAV signals are inserted for synchronization purposes.

BlankSAV : Blank Range Start of Video

BlankEAV : Blank Range End of Video

ActiveSAV : Active Range Start of Video

ActiveEAV : Active Range Stop of Video



Usage:

i) dout_select(format2 register) = “00b” or “11b”

- sync_blank_EAV_f0 ~ sync_activSAV_f0 registers used.

ii) dout_select(format2 register) = “01b”

- sync_blank_EAV_f0 ~ sync_activSAV_f0 registers used for odd field.
- sync_blank_SAV_f1 ~ sync_activSAV_f1 registers used for even field.

iii) dout_select(format2 register) = “10b”

- sync_blank_EAV_f0 ~ sync_activSAV_f0 registers used only.

.

(283-286) Sync CCIR

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#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
283	1B	sync_ccirFF	255	FF	11111111	RW	5	CCIR data format FFh
284	1C	sync_ccir00	0	00	00000000	RW	5	CCIR data format 00h
285	1D	sync_ccir80	128	80	10000000	RW	5	CCIR data format 80h
286	1E	sync_ccir10	16	10	00010000	RW	5	CCIR data format 10h

Default : 1Bh = FFh, 1Ch = 00h, 1Dh = 80h, 1Eh = 10h

Description :

CCIR data format FFh

CCIR data format 00h

CCIR data format 80h

CCIR data format 10h

(288-290) Scale

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
288	20	scale_x	32	20	00100000	RW	6	Horizontal scale factor (20h = x1)
289	21	scale_y	U	U	UUUUUUUU	RW	6	Vertical scale factor (20h = x1)
290	22	scale_th	4	04	00000100	RW	6	scale threshold

Default : 80h = 20h, 81h = variable with wire-strap setting, 82h = 04h

Description :

Scale X : 80h, Horizontal scale factor 20h = x1

Scale Y : 81h, Horizontal scale factor 20h = x1

Scale Th : 82h, Scale threshold

Usage:

i) NTSC, NTSC-J or (M)PAL

- scale_x = 20h, scale_y = 40h(x1/2)

ii) PALs

- scale_x = 20h, scale_y = 35h(x3/5)

(292-293) yContast / yBrightness

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
292	24	ycontrast	64	40	01000000	RW	6	Y contrast
293	25	ybrightness	1	01	00000001	RW	6	Brightness

Default : 24h = 40h, 25h = 01h

Description :

Luminous (Y) = Conversion Y x Contrast + Brightness

* Brightness : 2's complement arithmetic ; range (-128) ~ (+127)

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(294) Y Max

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
294	26	ymax	254	FE	11111110	RW	6	max. Y

Default : 26h = FEh,

Description :

Out Y Maximum (Clamping) data.

YUV : 1 ~ Y_clamp * 0, 255 : CCIR656 special number.

(295-296) Sepia Color : Cb tone / Cr tone

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
295	27	sephia_cb	192	C0	11000000	RW	6	Cb sephia
296	28	sephia_cr	64	40	01000000	RW	6	Cr sephia

Default : 27h = C0h, 28h = 40h

Description :

fixed color (Cb / Cr) data when sepia or color vignette mode.

Cb Color tone : sephia_cb

Cr Color tone : sephia_cr

(302-304) Edge Enhancement

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
302	2E	edge_gain	36	24	00100100	RW	5	Reference Edge Gain - 1
303	2F	edge_thp	16	10	00010000	RW	5	Positive Edge Threshold

Default : 2Eh = 10h , 2Fh = 10h, 30h = 1Fh

Description :

Edge Gain : 0x04 = x1

Edge Threshold : Positive Edge enhancement threshold.

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(314-328) Gamma Coefficient

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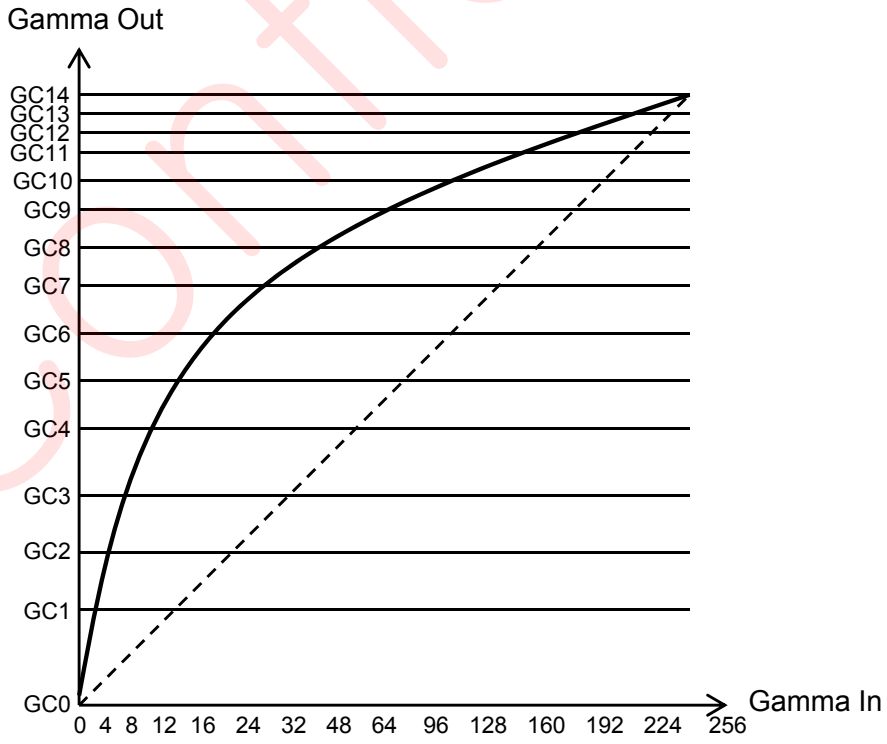
#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
314	3A	gm_y0	0	00	00000000	RW	5	Gamma Y0
315	3B	gm_y1	12	0C	00001100	RW	5	Gamma Y1
316	3C	gm_y2	25	19	00011001	RW	5	Gamma Y2
317	3D	gm_y3	39	27	00100111	RW	5	Gamma Y3
318	3E	gm_y4	52	34	00110100	RW	5	Gamma Y4
319	3F	gm_y5	75	4B	01001011	RW	5	Gamma Y5
320	40	gm_y6	92	5C	01011100	RW	5	Gamma Y6
321	41	gm_y7	116	74	01110100	RW	5	Gamma Y7
322	42	gm_y8	134	86	10000110	RW	5	Gamma Y8
323	43	gm_y9	164	A4	10100100	RW	5	Gamma Y9
324	44	gm_y10	186	BA	10111010	RW	5	Gamma Y10
325	45	gm_y11	206	CE	11001110	RW	5	Gamma Y11
326	46	gm_y12	224	E0	11100000	RW	5	Gamma Y12
327	47	gm_y13	241	F1	11110001	RW	5	Gamma Y13
328	48	gm_y14	255	FF	11111111	RW	5	Gamma Y14

Default : 00h, 0Ch, 19h, 27h, 34h, 4Bh, 5Ch, 74h, 8Ch, A4h, BAh, CEh, E0h, F1h, FFh

Description :

Gamma Correction is applied to RGB signal which ranges from 0 to 255 to compensate non-linear characteristics of display brightness vs input brightness. In many cases, power function of 0.45 is used as gamma function for CRT display.



GC : Gamma coefficient

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(330-344) Lens Shading Compensation

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
330	4A	lens_gainr	0	00	00000000	RW	5	Red lens gain
331	4B	lens_gaing1	0	00	00000000	RW	5	Gr lens gain
332	4C	lens_gaing2	0	00	00000000	RW	5	Gb lens gain
333	4D	lens_gainb	0	00	00000000	RW	5	Blue lens gain
336	50	lens_rx	0	00	00000000	RW	5	red lens x origin
337	51	lens_ry	0	00	00000000	RW	5	red lens y origin
338	52	lens_g1x	0	00	00000000	RW	5	green1 lens x origin
339	53	lens_g1y	0	00	00000000	RW	5	green1 lens y origin
340	54	lens_g2x	0	00	00000000	RW	5	green2 lens x origin
341	55	lens_g2y	0	00	00000000	RW	5	green2 lens y origin
342	56	lens_bx	0	00	00000000	RW	5	blue lens x origin
343	57	lens_by	0	00	00000000	RW	5	blue lens y origin
344	58	lens_scale	81	51	01010001	RW	5	East/West/South/North lens scale factor

Default : 4Ah = 00h, 4Bh = 00h, 4Dh = 00h, 50h = 00h, 51h = 00h
52h = 00h, 53h = 00h, 54h = 00h, 55h = 00h, 56h = 00h, 57h = 00h, 58h = 51h

Description :

Lens Gain R : Lens Shading Gain. 0x20 = x 1 gain.
Lens Gain G1 : Lens Shading Gain. 0x20 = x 1 gain.
Lens Gain G2 : Lens Shading Gain, 0x20 = x 1 gain.
Lens Gain B : Lens Shading Gain. 0x20 = x 1 gain.
Lens Red XY Origin : Window center origin Red XY value for Lens shading compensation
Lens Green XY Origin : Window center origin Green XY value for Lens shading compensation
Lens Blue XY Origin : Window center origin Blue XY value for Lens shading compensation
Lens Scale : East/West/South/North lens scale factor

(351-360) Edge data for auto focus

< Group B >

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
351	5F	af_cweight	7	07	00000111	RW	6	af center weight
352	60	af_cwinx1_h	1	01	00000001	RW	6	af window X1_H
353	61	af_cwinx1_l	104	68	01101000	RW	6	af window X1_L
354	62	af_cwinx2_h	2	02	00000010	RW	6	af window X2_H
355	63	af_cwinx2_l	48	30	00110000	RW	6	af window X2_L
356	64	af_cwiny1_h	0	00	00000000	RW	6	af window Y1_H
357	56	af_cwiny1_l	179	B3	10110011	RW	6	af window Y1_L
358	66	af_cwiny2_h	1	01	00000001	RW	6	af window Y2_H
359	67	af_cwiny2_l	72	48	01001000	RW	6	af window Y2_L
360	68	af_edge_th	0	00	00000000	RW	6	af edge threshold

Default : 5Fh = 07h, 60h = 01h, 61h = 68h, 62h = 02h, 63h = 30h, 64h = 00h, 65h = B3h
66h = 01h, 67h = 48h, 68h = 00h

Description :

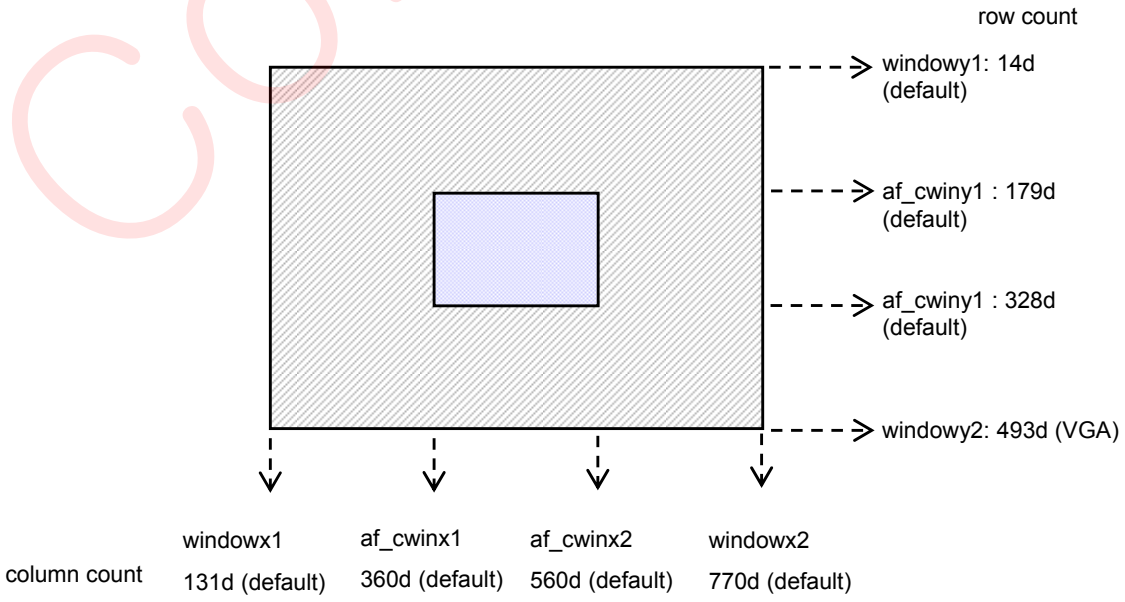
af_cweight : center weight of edge

*af_edge_sum=center_edge_sum * af_cweight +peri_edge_sum*(16-af_cweight) / 16*

af_cwinx1, af_cwinx2, af_cwiny1, af_cwiny2 : AF Center window x and y position
af_edge_th : edge threshold for af_edge_sum

Related Reg.: BankA – windowx1(0A,0Bh), windowy1(0C,0Dh), windowx2(0E,0Fh), windowy2(10,11h)
BankD – af_edge_sum4~1 (38~3Bh)

* AF Center window



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(362) TP control 0

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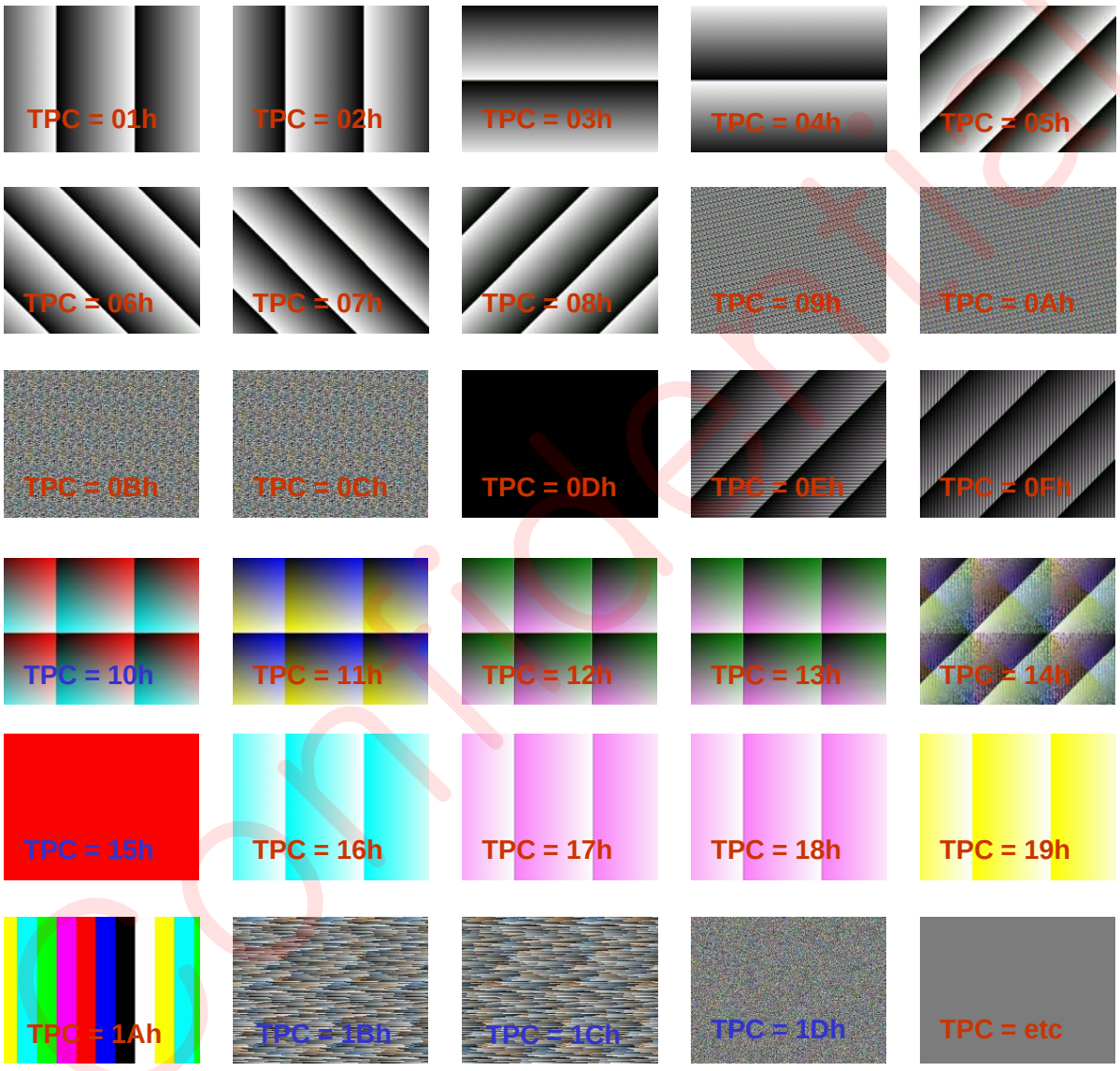
#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
362	6A	tp_control_0	0	00	00000000	RW	5	Test Pattern control register 00



(363~367) TP control 1~5

< Group B >

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
363	6B	tp_control_1	255	FF	11111111	RW	5	Test Pattern control register 01
364	6C	tp_control_2	255	FF	11111111	RW	5	Test Pattern control register 02
365	6D	tp_control_3	255	FF	11111111	RW	5	Test Pattern control register 03
366	6E	tp_control_4	255	FF	11111111	RW	5	Test Pattern control register 04

Default : 6Bh = FFh, 6Ch = FFh, 6Dh = FFh, 6Eh = FFh, 6Fh = 00h

Description :

tp_control_1 : R of Bayer
tp_control_2 : G1 of Bayer
tp_control_3 : G2 of Bayer
tp_control_4 : B of Bayer

(374) Filcker Control 2

< Group B >

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
374	76	flicker_control2	U	U	UUUUUUUU	RW	5	flicker mode control register 02

Default : 76h = variable with wire_strapping

Description :

register name : flicker_control_2								
register #	bit#	name	default	0	default(h)	00	default(b)	00000000
374(d) 76(h)	7	Reserved	U					
	6	fd_en	U	Auto flicker detection enable				
	5	Reserved	U					
	4	Reserved	U					
	3	manual_A	U	Manual_A				
	2	manual_B	U	Manual_B				
	1	Reserved	U					
	0		U					

Mode	Bit3 (manual60)	Bit2 (manual50)	Bit6 (fd_en)
Normal (flicker mode off)	0	0	0
Manual 60Hz flicker mode	1	0	0
Manual 50Hz flicker mode	0	1	0
Auto Flicker Detection	0	0	1

(392-413) Filcker cancellation method2

< Group B >

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
401	91	fd_period_a_h	U	U	UUUUUUU	RW	5	flicker period for CASE A (H)
402	92	fd_period_a_m	U	U	UUUUUUU	RW	5	flicker period for CASE A (M)
403	93	fd_period_a_l	U	U	UUUUUUU	RW	5	flicker period for CASE A (L)
404	94	fd_period_b_h	U	U	UUUUUUU	RW	5	flicker period for CASE B (H)
405	95	fd_period_b_m	U	U	UUUUUUU	RW	5	flicker period for CASE B (M)
406	96	fd_period_b_l	U	U	UUUUUUU	RW	5	flicker period for CASE B (L)
407	97	fd_period_c_h	U	U	UUUUUUU	RW	5	flicker period for 1/20 sec (H)
408	98	fd_period_c_m	U	U	UUUUUUU	RW	5	flicker period for 1/20 sec (M)
409	99	fd_fheight_a_h	U	U	UUUUUUU	RW	5	flicker frameheight for CASE A (H)
410	9A	fd_fheight_a_l	U	U	UUUUUUU	RW	5	flicker frameheight for CASE A (L)
411	9B	fd_fheight_b_h	U	U	UUUUUUU	RW	5	flicker frameheight for CASE B (H)
412	9C	fd_fheight_b_l	U	U	UUUUUUU	RW	5	flicker frameheight for CASE B (L)

Default : 91h ~ 9Ch = variable with wire_strapping,

Description :

FD Period A : Exposure period A
FD Period B : Exposure period B
FD Period C : Exposure period C
FD Frame Height A : Frame Height for each state A
FD Frame Height B : Frame Height for each state B

(420) Encoder control

< Group B >

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
420	A4	encoder control	0	00	00000000	RW	5	encoder control

Default : A4h = 00h

Description :

register name : Encoder control								
register #	bit#	name	default	**0**	default(h)	**00**	default(b)	**00000000**
420(d) A4(h)	7	encoder_off	0	'1' – encoder off, '0' – encoder on				
	6	Reserved	0					
	5	Reserved	0					
	4	enc_colorbar_en	0	Colorbar on/off				
	3	enc_colorbar_mode	0	'0'-100% color bar, '1'-75% color bar				
	2	Reserved	0					
	1	Reserved	0					
	0	Reserved	0					

(421) enc_scfreq

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
421	A5	enc_scfreq	U	UU	UUUUUUUU	RW	5	subcarrier frequency selection

Default : A5h : wire-strapping register

Description :

enc_scfreq : sub-carrier frequency selection

"00" : 3.579545 MHz for (M) NTSC, NTSC-J

"01" : 4.43361875 MHz for (B, D, G, H, I, N) PAL

"10" : 3.58205625 MHz for (Nc) PAL

"11" : 3.57561149 MHz for (M) PAL

(422-437) Composite level parameters

< Group B >

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
422	A6	enc_sync	16	10	00010000	RW	5	sync level
423	A7	enc_blankH	0	00	00000000	RW	5	blank level
424	A8	enc_blankL	U	UU	UUUUUUUU	RW	5	
425	A9	enc_pedestal	U	UU	UUUUUUUU	RW	5	pedestal
426	AA	enc_burst	U	UU	UUUUUUUU	RW	5	burst amplitude
427	AB	enc_Ygain	U	UU	UUUUUUUU	RW	5	Y convergence gain from YCbCr to YUV
428	AC	enc_Ugain	U	UU	UUUUUUUU	RW	5	U convergence gain from YCbCr to YUV
429	AD	enc_Vgain	U	UU	UUUUUUUU	RW	5	V convergence gain from YCbCr to YUV
430	AE	enc_Yrange_H	3	03	xxxxx011	RW	5	max. luminance
431	AF	enc_Yrange_L	32	20	00100000	RW	5	
432	B0	enc_Crange_H	1	01	xxxxx001	RW	5	max. amplitudes of chrominance
433	B1	enc_Crange_L	U	U	UUUUUUUU	RW	5	
434	B2	enc_chroma_max_H	3	03	xxxxx011	RW	5	maximum chrominance of composite output
435	B3	enc_chroma_max_L	U	U	UUUUUUUU	RW	5	
436	B4	enc_chroma_min_H	0	00	xxxxx000	RW	5	minmum chrominance of composite output
437	B5	enc_chroma_min_L	U	U	UUUUUUUU	RW	5	

Default : A6h = 10h, A7h = 00h, AEh = 03h, AFh = 20h, B0h = 01h, B2h = 03h, B4h = 00h
A8h, A9h, AAh, ABh, ACh, ADh, B1h, B3h, B5h : wire-strapping registers (refer to page14)

Description : please refer to next page.

enc_sync : sync_level
enc_blank : blank level
enc_pedestal : pedestal level
enc_burst : burst amplitude
enc_Y/U/Vgain: Conversion gain of YCbCr to YUV
enc_Yrange : separate Y range into positive and negative regions.
enc_Crange : define maximum level of Chrominance
enc_chroma_max: define maximum level of Composite.
enc_chroma_min: define minimum level of Composite.

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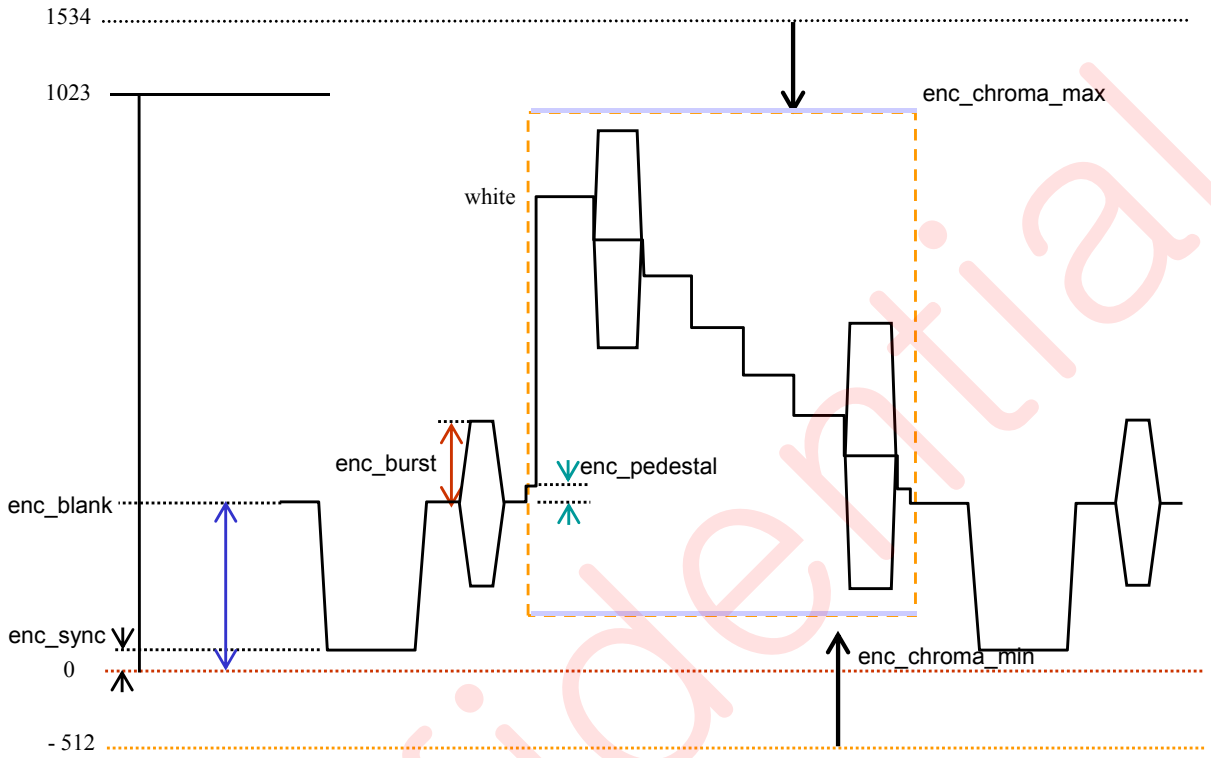
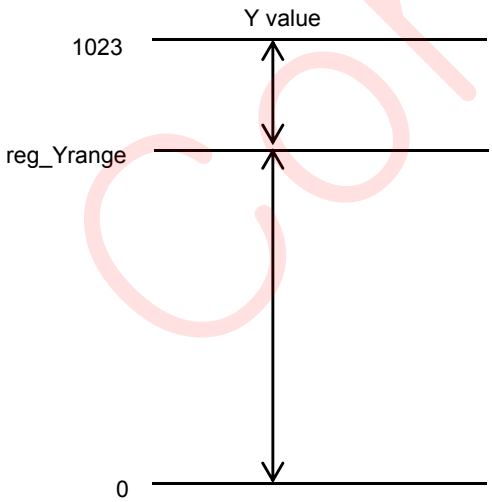
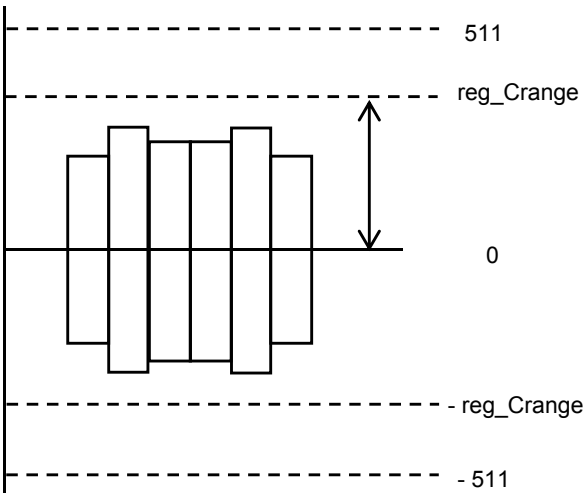


reg_chroma_max/min registers define the max. and min. of active data level.



reg_Yrange defines the boundary between positive or negative number of Y before composition.

In colorbar, Y might be negative values. It is the reason why the register exists.



reg_Crange designates the maximum amplitude of chroma.

It can be one of 0 to 511.

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(473) burst_toffset

< Group B >

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
473	D9	burst_toffset	0	00	00000000	RW	5	Burst Time offset

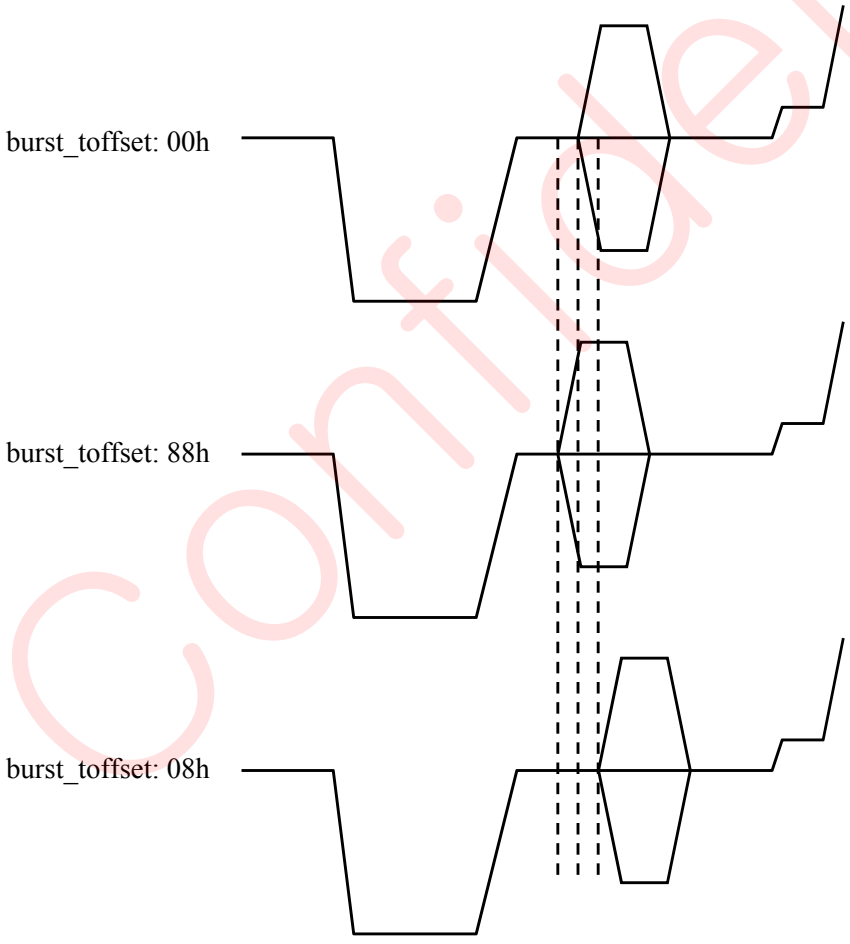
Default : D9h = 00h

Description :

burst_toffset : Burst time offset

It changes burst position on Back Porch.

msb: sign, other bits : magnitude



(485-496) motion detection

< Group B >

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
485	E5	md_yth	64	40	01000000	RW	5	Y(luminance) threshold for motion detection
486	E6	md_diff	64	40	01000000	RW	5	Difference of brightness between current and previous frames
487	E7	md_interval	8	08	00001000	RW	5	frame interval for motion detection
489	E9	md_section7	255	FF	11111111	RW	5	masks of 64 sections on one frame
490	EA	md_section6	255	FF	11111111	RW	5	
491	EB	md_section5	255	FF	11111111	RW	5	
492	EC	md_section4	255	FF	11111111	RW	5	
493	ED	md_section3	255	FF	11111111	RW	5	
494	EE	md_section2	255	FF	11111111	RW	5	
495	EF	md_section1	255	FF	11111111	RW	5	
496	F0	md_section0	255	FF	11111111	RW	5	

Default : E5h = 40h, E6h = 40h, E7h = 08h, E9h ~ F0h = all FFh

Description :

md_yth: Threshold of Y (luminance) mean difference between current and previous frames at the same section.

md_diff: Difference between entire current and previous frame's brightness means

md_interval: define frame interval for motion detection.

md_section7~0 : masks of 64 sections on one frame

md_section7(7) – mask bit for 63rd section,

md_section7(6) – mask bit for 62nd section,

md_section7(5) – mask bit for 61st section,

…

md_section0(7) – mask bit for 7th section,

md_section0(6) – mask bit for 6th section,

md_section0(5) – mask bit for 5th section,

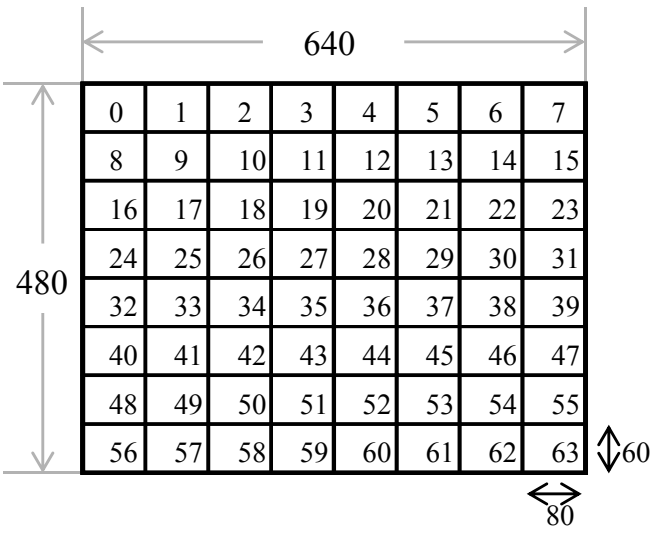
md_section0(4) – mask bit for 4th section,

md_section0(3) – mask bit for 3rd section,

md_section0(2) – mask bit for 2nd section,

md_section0(1) – mask bit for 1st section,

md_section0(0) – mask bit for 0th section



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▶ Register Tables (Detailed) : Group C

(516) Auto control 1

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
516	04	auto_control_1	152	98	10011000	RW	6	auto control register 01

Default : 04h = 98h

Description :

register name : auto_control_01								
register #	bit#	name	default	**152**	default(h)	**98**	default(b)	**10011000**
516(d) 04(h)	7	Reserved	1					
	6	Reserved	0					
	5	Reserved	0					
	4	Reserved	1					
	3	Reserved	1					
	2	Auto White Balance Register Update	0	**Auto White Balance Register update** '0' : Update by internal function (default) '1' : Update by external interface				
	1	Auto Exposure Register Update(1:0)	0	**Auto Exposure Register update** 00b : Update by Internal function. (default) 01b : Update by Exposure register 10b : Update by External_Inttime & Linear Gain 11b : Update by Inttime & Globalgain register				
	0		0					

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(518) Auto control 3

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
518	06	auto_control_3	144	90	10010000	RW	5	auto control register 03

Default : 06h = 90h

Description :

register name : auto_control_03								
register #	bit#	name	default	**0**	default(h)	**00**	default(b)	**00000000**
518(d) 06(h)	7	Reserved	1					
	6	LED Control 1 EN	0	**LED Control 1 Enable** '0' : Disable (default) '1' : Enable				
	5	LED Control 2 EN	0	**LED Control 2 Enable** '0' : Disable (default) '1' : Enable				
	4	Reserved	1					
	3	Reserved	0					
	2	Reserved	0					
	1	Reserved	0					
	0		0					

(519-521) External Integration Time

< Group C >

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
519	07	ext_inttime_h	0	00	00000000	RW	6	External Integration Time (H)
520	08	ext_inttime_m	128	80	10000000	RW	6	External Integration Time (M)
521	09	ext_inttime_l	0	00	00000000	RW	6	External Integration Time (L)

Default : 07h = 00h, 08h = 80h, 09h = 00h

Description :

Manual external integration time

(522-523) External linear Globalgain

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
522	0A	ext_glbg_h	1	01	00000001	RW	6	External Globalgain (H)
523	0B	ext_glbg_l	0	00	00000000	RW	6	External Globalgain (L)

Default : 0Ah = 01h, 0Bh = 00h

Description :

Manual external Globalgain.

(524-527) Exposure Register

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
524	0C	exposure_t	0	00	00000000	RW	6	Current Exposure (T)
525	0D	exposure_h	0	00	00000000	RW	6	Current Exposure (H)
526	0E	exposure_m	128	80	10000000	RW	6	Current Exposure (M)
527	0F	exposure_l	0	00	00000000	RW	6	Current Exposure (L)

Default : 0Ch (Exposure Register - T) = 00h
0Dh (Exposure Register - H) = 00h
0Eh (Exposure Register - M) = 80h
0Fh (Exposure Register - L) = 00h

Description :

Exposure[31:0] : "*Exposure*" register means abstract exposure level of sensor. Larger the value of *Exposure*, effectively longer exposure time. LSB of *Exposure* corresponds to 1/256 line exposure time. User can write *Exposure* register only when AE function is disabled.

(528-529) Exposure FrameHeight

< Group C >

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
528	10	expFrmH_H	2	02	00000010	RW	5	Reference Exposure FrameHeight (H)
529	11	expFrmH_L	12	0C	00001100	RW	5	Reference Exposure FrameHeight (L)

Default : 10h = 02h, 11h = 0Ch

(530-533) Middle / Maximum FrameHeight

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
530	12	midfrmheight_h	2	02	00000010	RW	5	Middle FrameHeight (H)
531	13	midfrmheight_l	12	0C	00001100	RW	5	Middle FrameHeight (L)
532	14	maxfrmheight_h	2	02	00000010	RW	5	Max FrameHeight (H)
533	15	maxfrmheight_l	12	0C	00001100	RW	5	Max FrameHeight (L)

Default : 12h = 02h, 13h = 0Ch, 14h = 02h, 15h = 0Ch

(534-542) Middle / Maximum / Minimum Exposure

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
534	16	minexp_h	0	00	00000000	RW	5	Middle Exposure (T)
535	17	minexp_m	0	00	00000000	RW	5	Middle Exposure (H)
536	18	minexp_l	12	0C	00001100	RW	5	Middle Exposure (M)
537	19	midexp_t	0	00	00000000	RW	5	Max Exposure (T)
538	1A	midexp_h	65	41	01000001	RW	5	Max Exposure (H)
539	1B	midexp_m	159	9F	10011111	RW	5	Max Exposure (M)
540	1C	maxexp_t	0	00	00000000	RW	5	Min Exposure (H)
541	1D	maxexp_h	65	41	01000001	RW	5	Min Exposure (M)
542	1E	maxexp_m	159	9F	10011111	RW	5	Min Exposure (L)

Default : 16h = 00h, 17h = 00h, 18h = 0Ch, 19h = 00h, 1Ah = 41h, 1Bh = 9Fh, 1Ch = 00h, 1Dh = 41h
1Eh = 9Fh

(549) AE center Weight

< Group C >

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
549	25	ae_c_weight	3	03	00000011	RW	6	AE Center Weight

Default : 25h = 03h,

Description :

Center window weight (CW) for back light compensation.

$$\text{Bright mean} = \frac{(Yc \times CW) + (Yp \times (16 - CW))}{16}$$

Yc : Center window Y mean

Yp : Periphery Y mean.

(550-551) Auto Exposure Speed

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
550	26	ae_up_speed	8	08	00001000	RW	6	AE upside Speed
551	27	ae_down_speed	12	0C	00001100	RW	6	AE downside Speed

Default : 26h = 08h, 27h = 0Ch

Description :

AE up Speed : AE speed applied when exposure is decreasing.

AE down Speed : AE speed applied when exposure is increasing

(552) Auto Exposure Lock

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
552	28	ae_lock	10	0A	00001010	RW	6	AE lock range

Default : 28h = 0Ah,

Description :

set margin of Auto Exposure function.

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(564) User wYt

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
564	34	user_wyt	128	80	10000000	RW	2	user Y target

Default : 34h = 80h

Description :

User weight Y target offset

(590-597) AE Window

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
590	4E	ae_winx_h	0	00	00000000	RW	5	AE window start X position(H)
591	4F	ae_winx_l	26	1A	00011010	RW	5	AE window start X position(L)
592	50	ae_winy_h	0	00	00000000	RW	5	AE window start Y position(H)
593	51	ae_winy_l	U	UU	UUUUUUUU	RW	5	AE window start Y position(L)
594	52	ae_width_h	2	02	00000010	RW	5	AE window Width (H)
595	53	ae_width_l	108	6C	01101100	RW	5	AE window Width (L)
596	54	ae_height_h	U	UU	UUUUUUUU	RW	5	AE window Height (H)
597	55	ae_height_l	U	UU	UUUUUUUU	RW	5	AE window Height (L)

Default : 4Eh = 00h, 4Fh = 1Ah, 50h = 00h, 52h = 02h, 53h = 6Ch,
51h , 54h , 55h – wire strapping register (refer to page14)

Description :

ae_winx : AE window start X position

ae_winy : AE window start Y position

ae_width : AE window Width

ae_height : AE window Height

(598-605) AE Center Window

< Group C >

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
598	56	ae_cwinx_h	0	00	00000000	RW	5	AE Center window start X position(H)
599	57	ae_cwinx_l	210	D2	11010010	RW	5	AE Center window start X position(L)
600	58	ae_cwiny_h	0	00	00000000	RW	5	AE Center window start Y position(H)
601	59	ae_cwiny_l	U	UU	UUUUUUUU	RW	5	AE Center window start Y position(L)
602	5A	ae_cwidth_h	0	00	00000000	RW	5	AE Center window Width (H)
603	5B	ae_cwidth_l	200	C8	11001000	RW	5	AE Center window Width (L)
604	5C	ae_cheight_h	0	00	00000000	RW	5	AE Center window Height (H)
605	5D	ae_cheight_l	U	UU	UUUUUUUU	RW	5	AE Center window Height (L)

Default : 56h = 00h, 57h = D2h, 58h = 00h, 5Ah = 00h, 5Bh = C8h, 5Ch = 00h
59h, 5Dh – wire strapping register (refer to page14)

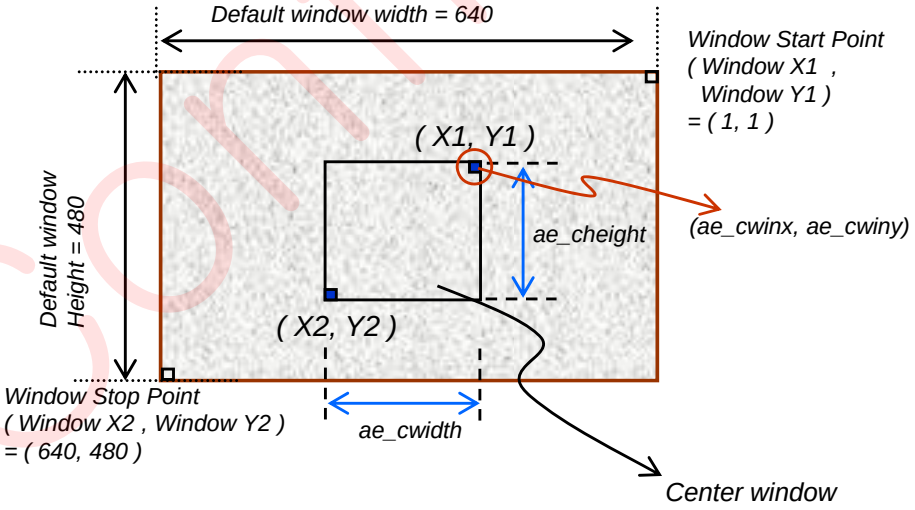
Description :

ae_cwinx : AE Center window start X position

ae_cwiny : AE Center window start Y position

ae_cwidth : AE Center Window Width

ae_cheight : AE Center Window Height



(666-675) AWB Window

< Group C >

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
666	9A	awb_winx1_h	0	00	00000000	RW	5	AWB window start X position(H)
667	9B	awb_winx1_l	124	7C	01111100	RW	5	AWB window start X position(L)
668	9C	awb_winy1_h	0	00	00000000	RW	5	AWB window start Y position(H)
669	9D	awb_winy1_l	46	2E	00101110	RW	5	AWB window start Y position(L)
670	9E	awb_winx2_h	3	03	00000011	RW	5	AWB window end X position (H)
671	9F	awb_winx2_l	0	00	00000000	RW	5	AWB window end X position(L)
672	A0	awb_winy2_h	1	01	00000001	RW	5	AWB window end Y position(H)
673	A1	awb_winy2_l	202	CA	11001010	RW	5	AWB window end Y position(L)
674	A2	awb_deltax	0	00	00000000	RW	5	AWB delta X for awb center window
675	A3	awb_deltay	0	00	00000000	RW	5	AWB delta Y for awb center window

Default : 9Ah = 00h, 9Bh = 7Ch, 9Ch = 00h, 9Dh = 2Eh, 9Eh = 03h, 9Fh = 00h, A0h = 01h,
A1h = CAh, A2h = 00h, A3h = 00h

Description :

awb_winx1 : AWB window start X position

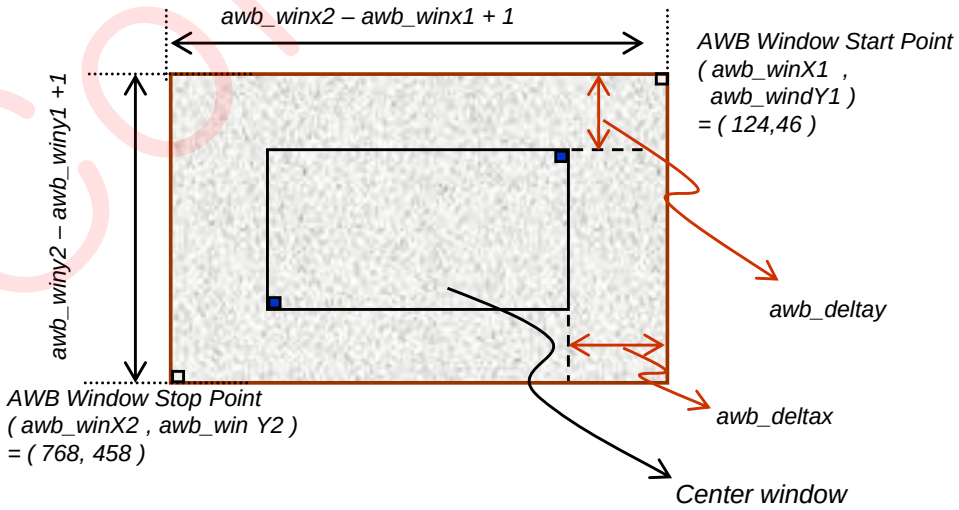
awb_winy1 : AWB window start Y position

awb_winx2 : AWB Window end X position

awb_winy2 : AWB Window end Y position

awb_deltax : AWB delta X for awb center window from awb_winx1 and awb_winx2

awb_deltay : AWB delta Y for awb center window from awb_winy1 and awb_winy2



reference count : rcount and ccount

< Group C >

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(676-677) AWB R/B ratio

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
676	A4	awb_rgratio	128	80	10000000	RW	5	AWB Red/Green Ratio
677	A5	awb_bgratio	128	80	10000000	RW	5	AWB Blue/Green Ratio

Default : A4h = 80h, A5h = 80h

Description :

awb_rgratio : Red mean target = Evaluate Green mean x R ratio / 128

awb_bgratio : Blue mean target = Evaluate Green mean x B ratio / 128

(678) Auto White Balance Lock

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
678	A6	awb_lock	2	02	00000010	RW	5	AWB lock range

Default : A6h = 02h,

Description :

awb_lock : Set margin of Auto White Balance functions

(679) Auto White Balance Speed

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
679	A7	awb_speed	8	08	00001000	RW	5	AWB speed (target AWB step numbers : 16 steps need to approach at One Time)

Default : A7h = 08h,

Description :

awb_speed : Auto White Balance evaluate speed.

(697-705) Color Correction Coefficients

< Group C >

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
697	B9	cc11	56	38	00111000	RW	5	Color correction matrix (1 , 1)
698	BA	cc12	165	A5	10100101	RW	5	Color correction matrix (1 , 2)
699	BB	cc13	13	0D	00001101	RW	5	Color correction matrix (1 , 3)
700	BC	cc21	147	93	10010011	RW	5	Color correction matrix (2 , 1)
701	BD	cc22	45	2D	00101101	RW	5	Color correction matrix (2 , 2)
702	BE	cc23	6	06	00000110	RW	5	Color correction matrix (2 , 3)
703	BF	cc31	131	83	10000011	RW	5	Color correction matrix (3 , 1)
704	C0	cc32	170	AA	10101010	RW	5	Color correction matrix (3 , 2)
705	C1	cc33	77	4D	01001101	RW	5	Color correction matrix (3 , 3)

Default : B9h = 38h, BAh = A5h, BBh = 0Dh, BCh = 93h, BDh = 2Dh, BEh = 06h, BFh = 83h,
C0h=AAh, C1h = 4Dh

Description :

$$\begin{pmatrix} R' \\ G' \\ B' \end{pmatrix} = \begin{pmatrix} cc11 & cc12 & cc13 \\ cc21 & cc22 & cc23 \\ cc31 & cc32 & cc33 \end{pmatrix} * \begin{pmatrix} R \\ G \\ B \end{pmatrix}$$

R', G' and B' are color corrected R,G and B

(748-750) LED Control Threshold

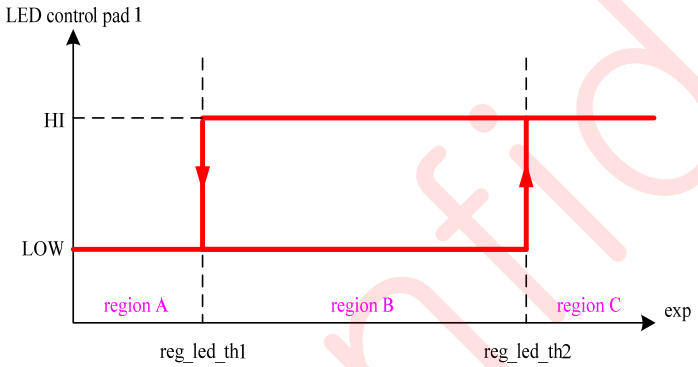
< Group C >

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
748	EC	led_th1_t	0	00	00000000	RW	5	led control threshold 1
749	ED	led_th1_h	0	00	00000000	RW	5	
750	EE	led_th1_m	0	00	00000000	RW	5	
751	EF	led_th2_t	0	00	00000000	RW	5	led control threshold 2
752	F0	led_th2_h	0	00	00000000	RW	5	
753	F1	led_th2_m	0	00	00000000	RW	5	
754	F2	led_th3_t	0	00	00000000	RW	5	led control threshold 2
755	F3	led_th3_h	0	00	00000000	RW	5	
756	F4	led_th3_m	0	00	00000000	RW	5	
757	F5	led_th4_t	0	00	00000000	RW	5	led control threshold 2
758	F6	led_th4_h	0	00	00000000	RW	5	
759	F7	led_th4_m	0	00	00000000	RW	5	

Default : All = 00h

Description :

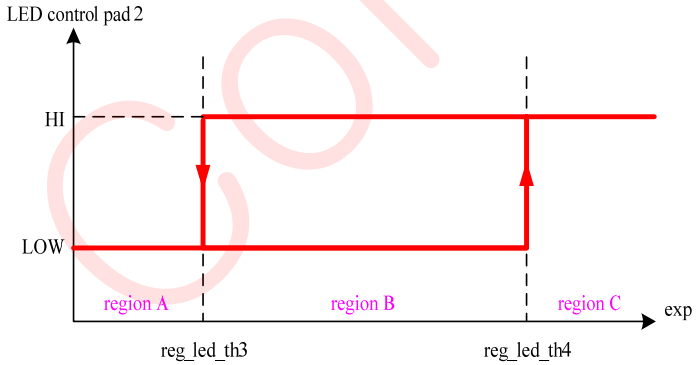
LED Control Threshold



exp < reg_led_th1 : LOW

reg_led_th1 < exp ≤ reg_led_th2 : HOLD

reg_led_th2 < exp : HIGH



exp < reg_led_th3 : LOW

reg_led_th3 < exp ≤ reg_led_th4 : HOLD

reg_led_th4 < exp : HIGH

(761) User CS

< Group C >

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
761	F9	user_cs	32	20	00100000	RW	5	user cs

Default : F9 = 20h

Description : User Color Saturation

▶ Register Tables (Detailed) : Group D

(825) af_edge_sum

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
830	3E	af_edge_sum_4	0	0		RO	0	edge data for auto focus(T)
831	3F	af_edge_sum_3	0	0		RO	0	edge data for auto focus(H)
832	40	af_edge_sum_2	0	0		RO	0	edge data for auto focus(M)
833	41	af_edge_sum_1	0	0		RO	0	edge data for auto focus(L)

Description :

af_edge_sum : edge data for auto focus support

▶ Electrical Characteristics

Absolute Maximum Ratings *

HVDD,AVDD Supply Voltage ---------- -0.3V to 4.5V
DVDD Supply Voltage ---------- -0.3V to 2.5V
DC Voltage at any input pin ---------- -0.3V to HVDD+0.3V
DC Voltage at any output pin ---------- -0.3V to HVDD+0.3V
Storage Temperature ---------- -40°C to + 125 °C

Table 4. DC Characteristics

Symbol	Descriptions	Min	Typ	Max	Unit
V_{DDD}	Digital VDD voltage relative to GND(DGND) level.	1.71	1.8	1.89	V
V_{DDA}	Analog voltage relative to GND(AGND) level.	2.66	2.8	2.94	V
HV_{DD}	High VDD(HVDD) voltage relative to GND(DGND) level.	2.66	2.8 3.3	3.47	V
I_{DDD}	Supply current at 60 fps. Currents are programmable through 2-wire serial interface. @				
	DVDD=1.8V		25.0		mA
	AVDD=2.8V		19.0		mA
	HVDD=2.8V		4.9		mA
	CVDD=2.8V		36.0		mA
I_{DDS}	Standby supply current@ DVDD=1.8V/AVDD=2.8V/HVDD=2.8V/CVDD=2.8V		9		uA
V_{IL1}	Input voltage LOW level			0.2*HVDD	V
V_{IH1}	Input voltage HIGH level	0.8*HVDD			V
V_{IL2}	Input voltage LOW level for rClk, rData.			0.2*HVDD	V
V_{IH2}	Input voltage HIGH level for rClk, rData	0.8*HVDD			V
C_{IN}	Input pin capacitance			10	pF
V_{OL1}	Output Voltage LOW			0.1*HVDD	V
V_{OH1}	Output Voltage HIGH	0.9*HVDD			V
V_{OL2}	Output Voltage LOW level for rClk, rData.			0.2	V
V_{OH2}	Output Voltage HIGH level for rData.	HVDD-0.2			V
I_{IN}	Input leakage current		0.005	1	uA
I_{OT}	Output leakage current		0.005	1	uA

* Excessive stresses may cause permanent damage to the device.

Table5. AC Characteristics (In case of HVDD=2.8V)

Cload=16pF

Symbol	Descriptions	Min	Typ	Max	Unit
f_{MCLK}	Master clock Frequency		27		MHz
duty	Master clock duty cycle		50		%
t1	Master clock rise/fall time		4.7		ns
t2	PCLK rise/fall time		3.5		ns
t3	PCLK rising edge to HSYNC		20.85		ns
t4	PCLK rising edge to digital output		19.75		ns
t5	MCLK rising edge to PCLK rising edge		21.45		ns
t6	PCLK rising edge to VSYNC		21.1		ns

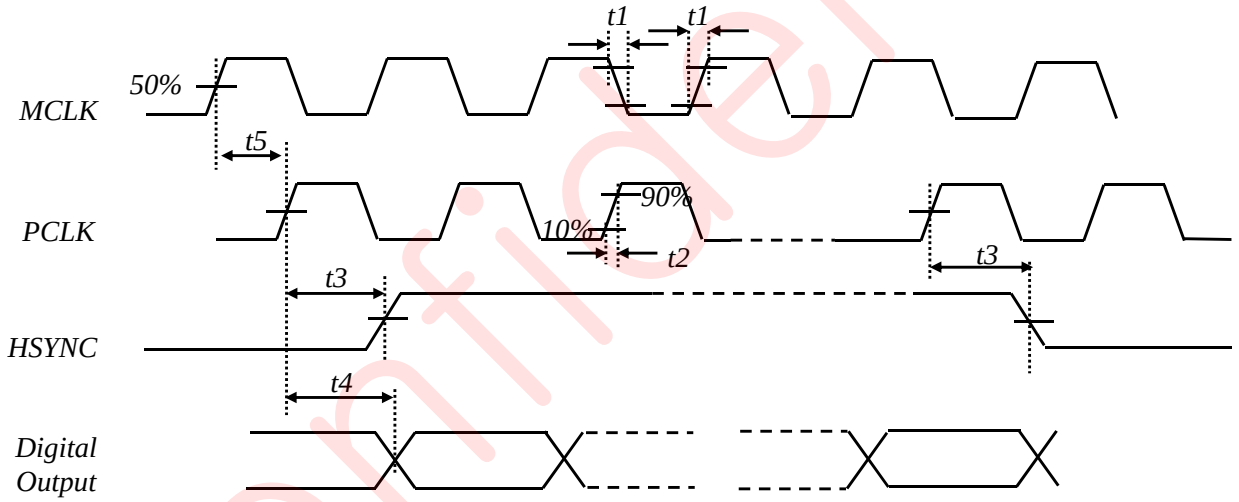


Fig. 12 Timing diagram of Clock, Data, and HSync

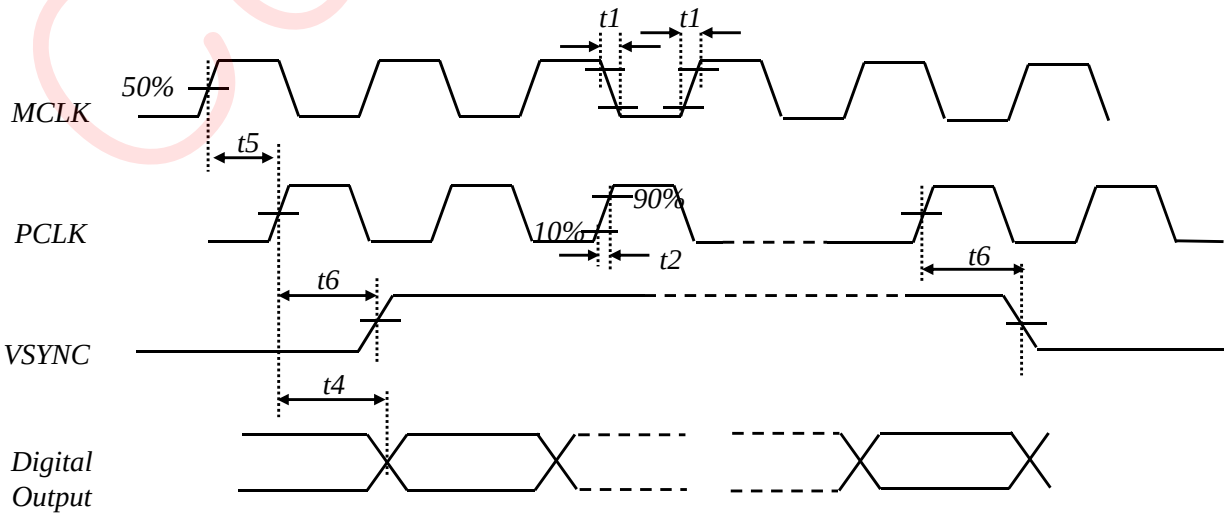


Fig. 13 Timing diagram of Clock, Data, and VSync

Table 6. Electro-Optical Characteristics (@ 60degree)

Symbol	Parameter	Notes	Min	Typ	Max	Unit
Sens	Sensitivity	1)		*3.16*		V/Lux.sec
Vsat	Saturation Level	2)		1.2		V
Vdrk	Dark Signal	3)		*47.9*		mV/sec
DR	Dynamic range	4)		*63.5*		dB

Notes :

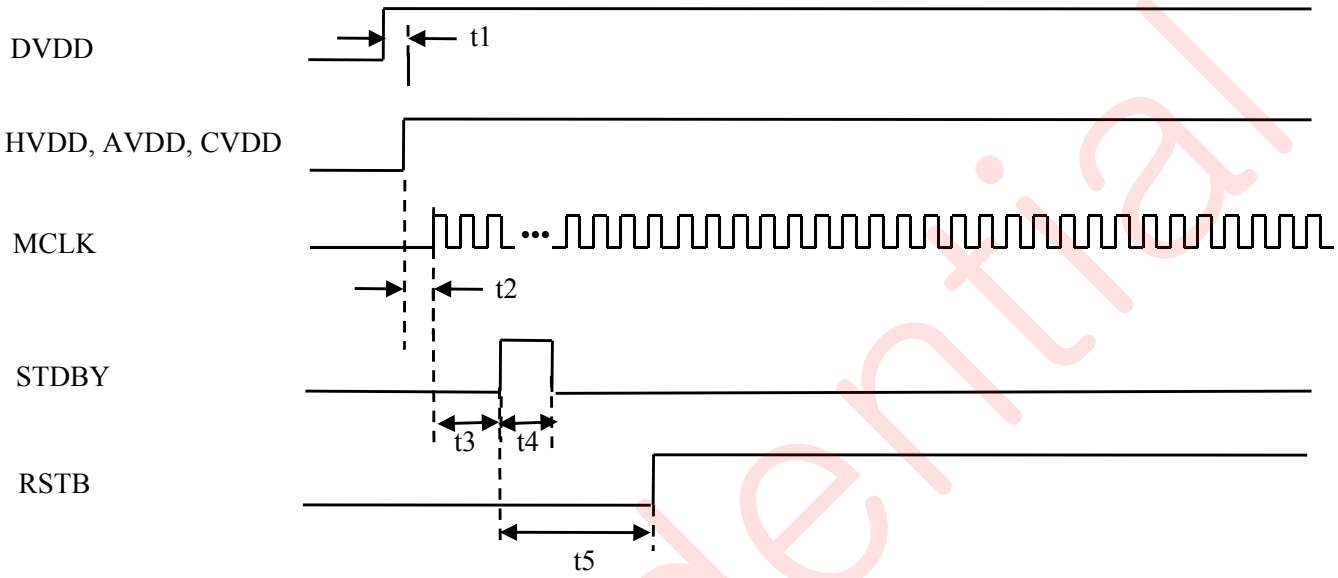
1) This value comes from the wafer test. The calculation sequence is as follows.
   (1) read the saturation level from evaluation pad
   (2) calculate One LSB.
   (3) Read output signal of Green pixels under illumination with output signal equal to 50% of saturation signal.
   (4) Read the Luminance and Integration Time when 50% of saturation signal.
   (5) Calculate the sensitivity using (1)~(4)
   = (the signal of Green pixels * one LSB) / (luminance * integration time)

2) Read the value of evaluation pad when all pixels are saturated in condition

3) Measured at the zero illumination.
   (1) read the dark signal average of all pixels for minimum integration time
   (2) read the dark signal average of all pixels for maximum integration time
   (3) [Dark signal @ maximum integration time] - [Dark signal @ minimum integration time]
   (4) convert to mV/sec unit

4) For frame rate=60 fps
   20*Log [Saturation Signal /Dark signal] [dB]

Power-On Sequence



Power-Off Sequence

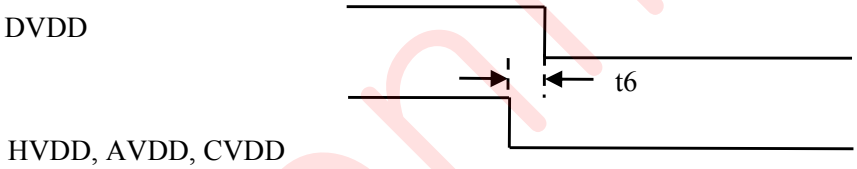


Table7. Recommended Power-On/Off sequence

Symbol	Descriptions	Min	Typ	Max	Unit
t1	From DVDD rising to HVDD, AVDD, CVDD rising	0			ns
t2	From HVDD rising to MCLK Start	0			ns
t3	From MCLK Start to STDBY rising	0			ns
t4	From STDBY rising to falling	2			ms
t5	From STDBY rising to RSTB rising	t4 x 10			ms
t6	From HVDD, AVDD, CVDD falling to DVDD falling	0			ns

1/4 inch VGA class Analog/Digital Output NTSC/PAL CMOS Image Sensor

▶ Application Note

- Revision Number

Reg. Addr. (Hex)	Read Value (Hex)	Register Name	Descriptions
02	00	*RevNum*	Revision Number of PC1030N

-Default Setting

PC1030N's default setting is considered to meet acquirement of SMPTE-170M.-2004.

- Register Groups

PC1030N has four Register Groups (Register A, B, C & D).

So, you must be careful and make sure that the correct register group is firstly selected before you access registers .

Register Group can be selected by Setting Reg.03h.

Address (Hex)	Write Value (Hex)	Register Name	Descriptions
03	**00**	*RegisterSel*	Select Register Group A
	01		Select Register Group B
	02		Select Register Group C
	03		Select Register Group D

Ex) When you want to write (or read) the value to Reg.04h in the Register Group A,

=> 1st > Write 0x00 to Reg.03h

2nd >Write (or Read) the value to Reg.04h

When you want to write (or read) the value to Reg.04h and 05h in the Register Group B,

=> 1st > Write 0x01 to Reg.03h

2nd >Write (or Read) the values of Reg.04h and 05h

< Notation >

We will use the following notation in this application note to separate registers according to the Register Group which they belong to.

Register Group	Notation	Example
A	A-	A-10 : Reg.10h in Register Group A
B	B-	B-4C : Reg.4Ch in Register Group B
C	C-	
D	D-	

- Flicker Free Mode

(1) Manual Flicker Free Mode

-Related Registers : Reg.B-76h, Reg.B-91h ~ B-96h , -Related Strap pin : D4,D5.

Flicker canceling mode can be set by not only writing registers directly but also controlling by strap pin as D4,D5. Strap setting can be ignored after register setting has been changed by EEPROM and external i2c master.

Reg. Addr. (Hex)	Register Name	Default Value (Hex)	Setting value	Descriptions
B-91	*PD_PeriodA (H)*	01	$256 * \frac{\text{MCLK Freq.} / \text{Frame Width}}{120}$	Flicker period
B-92	*PD_PeriodA (M)*	06		
B-93	*PD_PeriodA (L)*	3C		
B-94	*PD_PeriodB (H)*	01	$256 * \frac{\text{MCLK Freq.} / \text{Frame Width}}{100}$	Flicker period
B-95	*PD_PeriodB(M)*	3A		
B-96	*PD_PeriodB (L)*	AF		

Reg. Addr. (Hex)	Register Name	Default Value (Hex)	Setting Value	Descriptions
B-76	*FdControl02*	00	**80 / 88 / 84**	Off / 60Hz / 50Hz Flicker Free Enable

-Flicker Period Control Register Setting

ex) 60Hz flicker, MCLK = 27MHz, NTSC

Frame Width = *Frame Width (Reg A-06h,A-07h) + 1 = 858d.*

→ *FD_PeriodA = 256*(27000000 / 858) / (60*2) = 67132d = 1063Ch.*

→ *FD_PeriodA (H) = 01h, FD_PeriodA (M) = 06h, FD_PeriodA (L) = 3Ch.*

ex) 50Hz flicker, MCLK = 27MHz, NTSC

Frame Width = *Frame Width (Reg A-06h,A-07h) + 1 = 858d..*

→ *FD_PeriodB = 256*(27000000 / 776) / (50*2) = 80559d = 13AAFh.*

→ *FD_PeriodB (H) = 01h, FD_PeriodB (M) = 3Ah, FD_PeriodB (L) = AFh.*

**) Frame Width Value*

NTSC - 0359h (857d), PAL - 040Dh (1037d)

(2) Auto Flicker Detection Mode

PC1030N support auto flicker detection mode.

Reg. Addr. (Hex)	Appropriate value	Register Name	Default Value (Hex)	Descriptions
B-89	$\frac{256*256*4}{\text{60Hz flicker period (line)}}$	*Reserved*	03	
B-8A		*Reserved*	E8	
B-8B	$\frac{256*256*4}{\text{50Hz flicker period (line)}}$	*Reserved*	03	
B-8C		*Reserved*	42	
B-90	*Appropriate Value*	*FD_Th*	10	Flicker Detection Threshold
B-91	$256*\frac{\text{MCLK Freq.}/\text{Frame Width}}{120}$	*FD_PeriodA (H)*	01	Flicker Period for 60Hz flicker
B-92		*FD_PeriodA (M)*	06	
B-93		*FD_PeriodA (L)*	3C	
B-94	$256*\frac{\text{MCLK Freq.}/\text{Frame Width}}{100}$	*FD_PeriodB (H)*	01	Flicker Period for 50Hz flicker
B-95		*FD_PeriodB (M)*	3A	
B-96		*FD_PeriodB (L)*	AF	
B-97	$\frac{\text{MCLK Freq.}/\text{Frame Width}}{20}$	*FD_PeriodC (H)*	06	Period (line) for 20Hz
B-98		*FD_PeriodC (M)*	25	

Reg. Addr. (Hex)	Setting Value (Hex)	Register Name	Default Value (Hex)	Descriptions
B-76	**C0**	*FdControl02*	00	50Hz / 60Hz flicker Auto Detection

- Flicker Detection Control Registers Setting

ex) Frame Width = *Frame Width (Reg A-06h,A-07h) + 1 = 858d, MCLK = 27MHz, NTSC*

(1) FD_PeriodA (60Hz flicker) = 256(27000000 / 858) / (60*2) = 67132d = 1063Ch.*

→ *FD_PeriodA (H) = 01h, FD_PeriodA (M) = 06h, FD_PeriodA (L) = 3Ch.*

(2) FD_PeriodB (50Hz flicker) = 256(27000000 / 858) / (50*2) = 80559d = 13AAFh.*

→ *FD_PeriodB (H) = 01h, FD_PeriodB (M) = 3Ah, FD_PeriodB (L) = AFh*

(3) FD_PeriodC = (27000000 / 858) / 20 = 1573d = 625h.

→ *FD_PeriodC (H) = 06h, FD_PeriodC (M) = 25h*

*(4) Reg.B-89h ~ 8Ah = 256*256*4 / FD_PeriodA(H) = 256*256*4 / 262= 1000d = 3E8h*

→ *Reg.B-89h = 03h, Reg.B-8Ah = E8h*

*(5) Reg.A-8Bh ~ 8Ch = 256*256*4 / FD_PeriodB(H) = 256*256*4 / 314 = 834d = 342h*

→ *Reg.B-8Bh = 03h, Reg.B-8Ch = 42h*

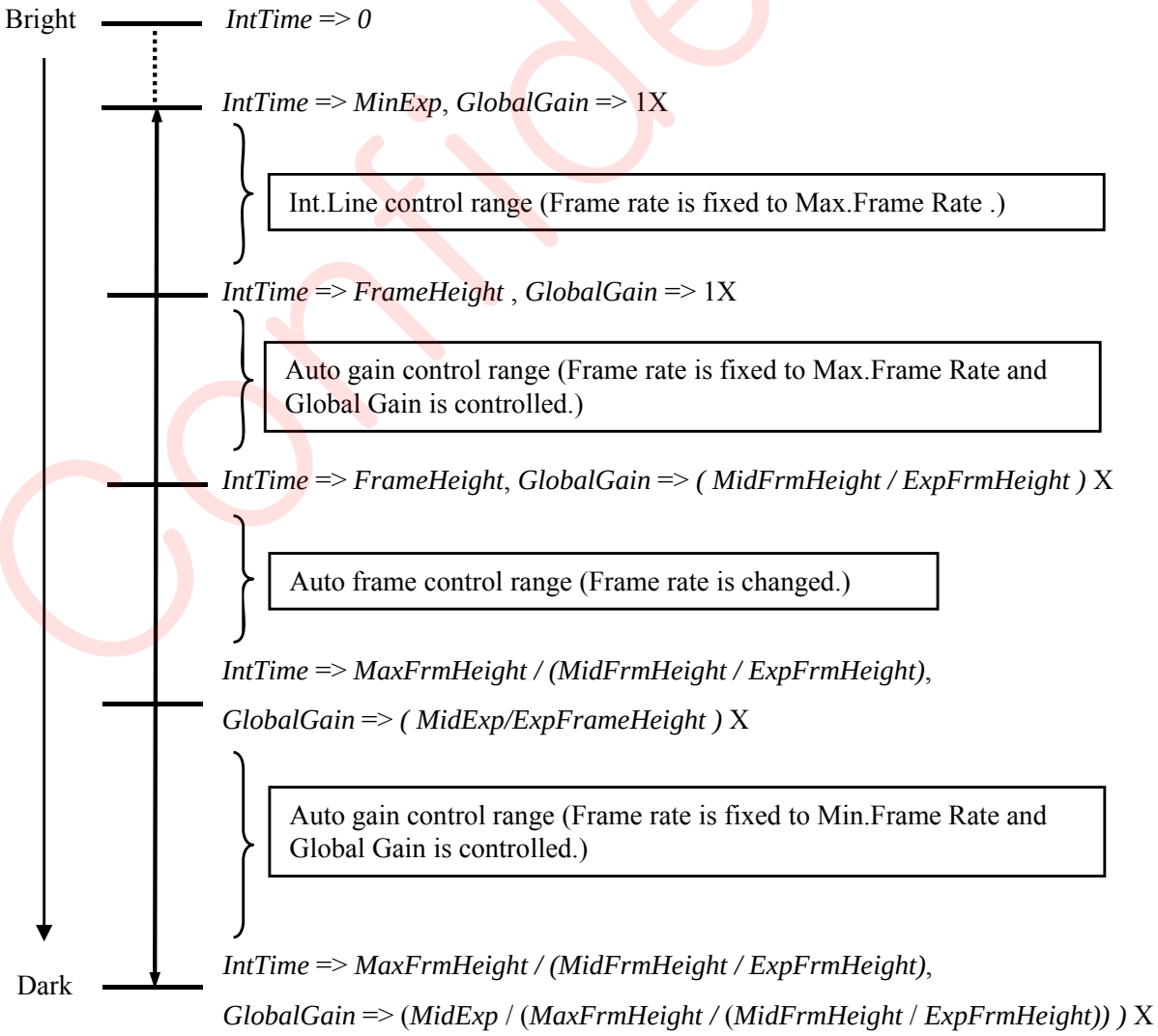
**) Frame Width Value - NTSC - 0359h (857d), PAL - 040Dh (1037d)*

- AE Control

(1) Internal AE Control

Related Registers : Int.Time(Reg.A-21h ~ A-26h), GlobalGain(Reg.A-1Ah, A-1Bh), AutoControl1(Reg.C-04h), MidFrmHeight(Reg.C-12h, C-13h), MaxFrmHeight(Reg.C-14h, C-15h), MidExp(Reg.C-19h ~ C-1Bh), MaxExp (Reg.C-1Ch ~ C-1Eh), MinExp(Reg.C-16 ~ C-18h), ExpFrmHeight(Reg.C-10 ~11h), AELock(Reg.C-28h)

If AEr bits of *AutoControl1(Reg.C-04h*) register is set to "00", *IntTime(Reg.A-21 h ~ A-26h)*, *GlbGain(Reg.A-1Ah, A-1Bh)* registers are automatically controlled by ISP to adjust overall brightness of sensor image. During auto exposure process, the average brightness of image is adjusted to get close to Target Exp. value with the margin set by *AELock*(*Reg.C-28h*) register. *IntTime* registers are controlled, at first. If Integration Line is limited to the *MaxFrmHeight*(*Reg.C-14h, C-15h*), then Global Gain is controlled. Variation of *GlbGain* and *IntTime* registers are limited by *MaxExp, MidExp*, *MinExp and MaxFrameHeight* registers described in the figure below.



Auto Frame Control Method can be used to get brighter image in dark condition. Frame rate is automatically controlled by ISP between Max.Frame Rate and Min.Frame Rate.

Max. Frame Rate = (MCLK frequency) / (Frame Height * Frame Width * 2)

Min. Frame Rate

= (MCLK frequency) / ((*MaxFrmHeight / Mid. Global Gain)** Frame Width * 2)

Max. Int. Time = *MaxFrmHeight / Mid. Global Gain* ------ (1)

Min. Int. Time = *MinExposure* ------ (2)

(Frame Height = *FrameHeight* + 1, Frame Width = *FrameWidth* + 1)

Min. Frame Rate is controlled by *MaxFrmHeight* register. *MaxFrmHeight* must be bigger than *ExpFrmHeight* and *MidFrmHeight*.(*MaxFrmHeight* >= *MidFrmHeight* >= *ExpFrmHeight*)

2) Auto Gain Control

Auto Gain Control Method can be used to get brighter image in dark condition. Global gain is controlled automatically by ISP between Max.Global Gain and Min.Global Gain.

Max. Gain = Max. Global Gain * Max. Digital Gain

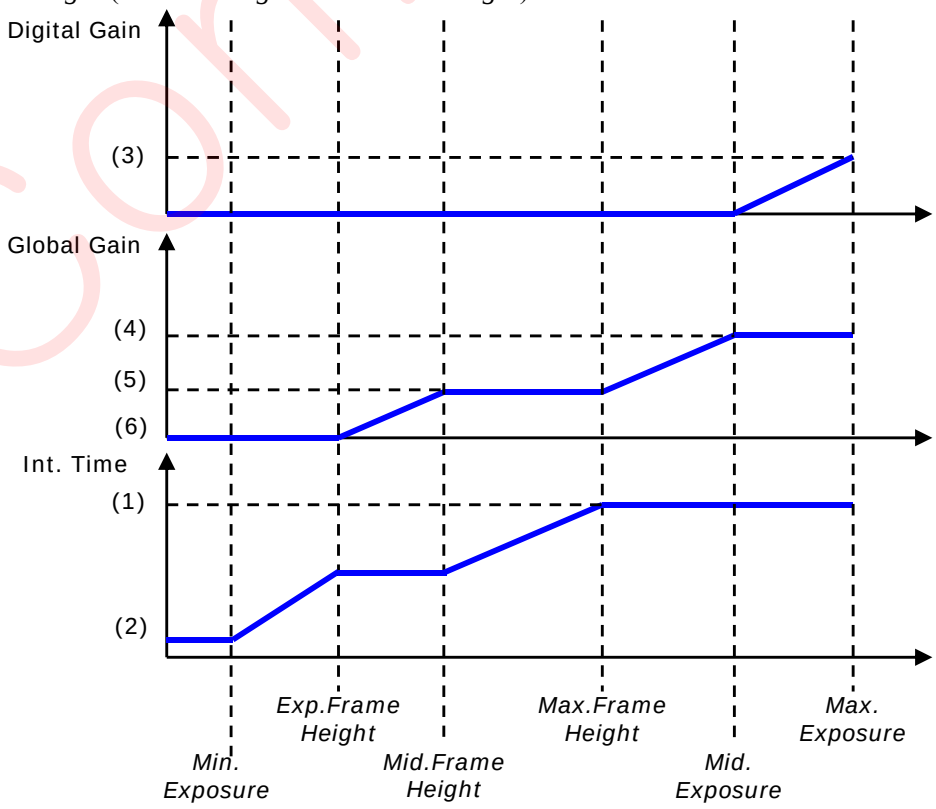
Max. Digital Gain = *(MaxExp / (*Max. Global Gain * Max. Int. Time*))* X ------ (3)

Max. Global Gain = (*MidExp* / Max. Int. Time*)* X ------- (4)

Mid. Global Gain = (*MidFrmHeight* / *ExpFrmHeight*) X ------ (5)

Min. Global Gain = 1X ------ (6)

MaxExp must be bigger than *MaxFrmHeight. (MaxExp* >= *MaxFrmHeight)* and *MidFrmHeight* must be bigger than *MaxFrmHeight* (*MidFrmHeight* >= *MaxFrmHeight*).



(2) External AE Control

1) Exposure Control Mode

Related Registers : AutoControl1 (Reg.C-04h), Exposure (Reg.C-0Ch ~ C-0Fh)

If you turn off internal AE function of PC1030N, you can control Integration line and Global gain through *Exposure (Reg.C-0Ch ~ C-0Fh)* registers for implementing external Auto Exposure function. *IntTime* (*Reg.A-21h ~ A-26h*) and *GlobalGain* (*Reg.A-1Ah, A-1Bh*) registers aren't accessible by user. *Exposure* (*Reg.C-0Ch ~ C-0Fh*) registers aren't controllable while internal AE is working.

- Disable Internal AE Function for This Mode

Reg. Addr. (Hex)	Register Name	Descriptions
C-04	*AutoControl1*	Set Bit 1 & 0 (AEr) to "01" to turn off internal AE function and control it by Exposure registers.
C-26	*AEUpSpeed*	Set this register to 00h
C-27	*AEDownSpeed*	Set this register to 00h

- Registers for External AE Control

Reg. Addr. (Hex)	Register Name	Descriptions
C-0C	*Exposure(T)*	Exposure register
C-0D	*Exposure(H)*	
C-0E	*Exposure(M)*	
C-0F	*Exposure(L)*	

(1) $MinExp < Exposure \leq FrameHeight$ (Int.Line Control Range)

(2) $FrmHeight < Exposure \leq MidExp$ (Global Gain Control Range)

(3) $FrameHeight < Exposure \leq MaxFrmHeight$ (Frame Rate Control Range)

Current Frame Rate = (MCLK freq.) / (*Exposure – (MidExp + FrameHeight)*) * Frame Width * 2)

Min. Frame Rate is limited by *MaxFrmHeight*.

(4) $MaxFrmHeight < Exposure \leq MaxExp$ (Global Gain Control Range)

Current Global Gain = (*MidExp* / *FrameHeight*) * (*Exposure* / *MaxFrmHeight*) X

Max.Gain is limited by *MaxExp*.

2) Manual External IntTime and Global Gain Control Mode

Related Registers : AutoControl1 (Reg.C-04h), ExtIntTime (Reg.C-07h ~ 09h), ExtLGlbG (Reg.C-0Ah, C-0Bh)

If you turn off internal AE function of PC1030N, you can control Integration line and Global gain through ExtIntTime *(Reg.C-07h ~ C-09h*) and ExtGlbG *(Reg.C-0Ah, C-0Bh*) registers for implementing external Auto Exposure function. *IntTime* (*Reg.A-21h ~ A-26h*) and *GlobalGain* (*Reg.A-1Ah, A-1Bh*) registers aren't accessible by user. ExtIntTime *(Reg.C-07h ~ C-09h*) and ExtGlbG *(Reg.C-0Ah, C-0Bh*) registers aren't controllable while internal AE is working.

- Disable Internal AE Function for This Mode

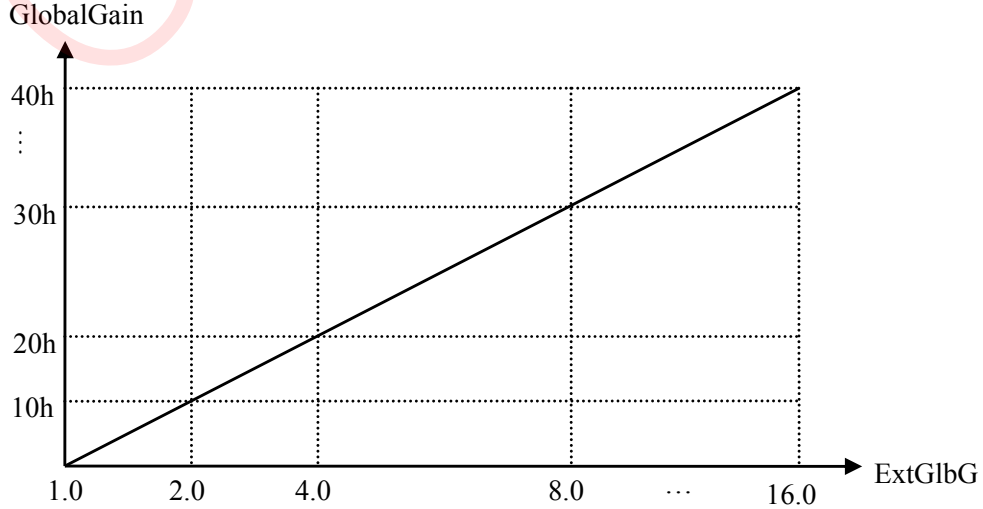
Reg. Addr. (Hex)	Register Name	Descriptions
C-04	*AutoControl1*	Set bit 1& 0 (AEr) to "10" to turn off internal AE function & control it by External Int.Time & External Global Gain.
C-26	*AEUpSpeed*	Set this register to 00h
C-27	*AEDownSpeed*	Set this register to 00h

- Registers for External AE Control

Reg. Addr. (Hex)	Register Name	Descriptions
C-07	*ExtIntTime(H)*	External Integration Time
C-08	*ExtIntTime(M)*	
C-09	*ExtIntTime(L)*	
C-0A	*ExtLGlbG(H)*	External Global Gain (1X : Reg.C-0Ah = 01h, Reg.C-0Bh = 00h (Min.) 16X : Reg.C-0Ah = 10h, Reg.C-0Bh = 00h (Max.))
C-0B	*ExtLGlbG(L)*	

(1) *IntTime = ExtIntTime*

(2) *ExtLGlbG*



- AWB Control

(1) Internal AWB Control

Related Registers : RGain(Reg.A-27h), GGain(Reg.A-28h), BGain(Reg.A-29h), AWBRratio(Reg.C-A4h), AWBBratio(Reg.C-A5h),

If WU of *AutoControl1(Reg.C-04*h) register is set to '1', *RGain*(*Reg.A-27h*) and *BGain*(*Reg.A-29h*) registers are automatically controlled by ISP to control the RGB ratio of sensor image. The ratio of average of R, G, B components can be controlled by *AWBRratio and AWBBratio* registers. Those ratios are defined according to the following relation,

$$\overline{B} = \frac{AWBBratio}{128} \times \overline{G} \qquad \overline{R} = \frac{AWBRratio}{128} \times \overline{G}$$

(2) External AWB Control

If you turn off internal AWB function of PC1030N, you can control R, G and B gains through *R, G* and *B Gain* (*Reg.A-27h ~ A-29h*) registers for implementing external Auto White Balance function. *R* and *B gain* registers aren't controllable while internal AWB is working.

- Disable Internal AWB Function

Reg. Addr. (Hex)	Register Name	Descriptions
C-04	*AutoControl1*	Set Bit 3(AWBr) to '0' to turn off internal AWB function.

- Registers for external AWB control

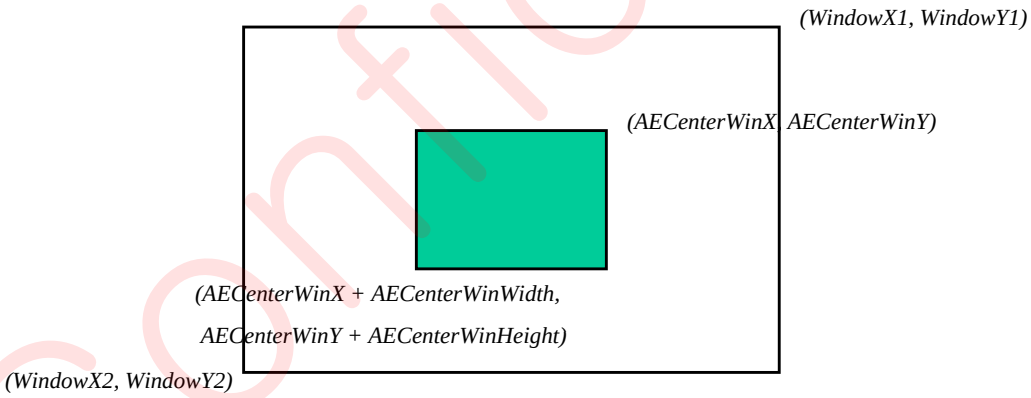
Reg. Addr. (Hex)	Register Name	Default Value (Hex)	Descriptions
A-27	*R Gain*	40	1X R Gain = 0x40 (2X = 0x80)
A-28	*G Gain*	40	1X G1 Gain = 0x40
A-29	*B Gain*	40	1X B Gain = 0x40

- Backlight Compensation

Related Registers : AECenterWinX (Reg.C-56h, C-57h), AECenterWinY (Reg.C-58h, C-59h),
AECenterWinWidth (Reg.C-5Ah, 5Bh), AECenterWinHeight (Reg.C-5Ch, 5Dh), AECenterWeight (Reg.C-25h)

1) Weight Window

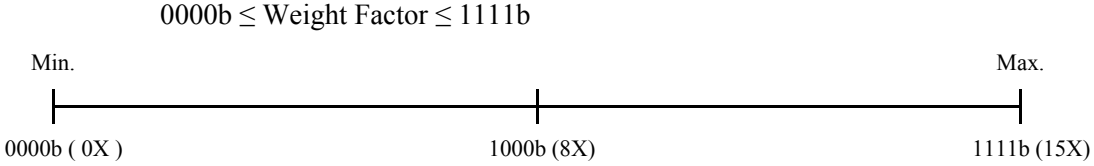
Reg. Addr. (Hex)	Register Name	Default Value (Hex)	Description
C-56	*AECenterWinX (H)*	00	**Minimum** : *WindowX1*(*Reg.A-0Ah, A-0Bh*)
C-57	*AECenterWinX (L)*	D2	
C-58	*AECenterWinY (H)*	00	**Maximum** : *WindowX2*(*Reg.A-0Eh, A-0Fh*)
C-59	*AECenterWinY (L)*	UU	
C-5A	*AECenterWinWidth (H)*	00	**Minimum** : *WindowY1*(*Reg.A-0Ch, A-0Dh*)
C-5B	*AECenterWinWidth(L)*	C8	
C-5C	*AECenterWinHeight (H)*	00	**Maximum**: *WindowY2*(*Reg.A-10h, A-11h*)
C-5D	*AECenterWinHeight (L)*	UU	



Window size is different according to output mode(NTSC:640x240, PAL:640x288).
Therefore user should set AE center window size consider window size.

2) Weight Factor

Weight Factor is controlled by AECenterWeight register (*Reg.C-25h*).



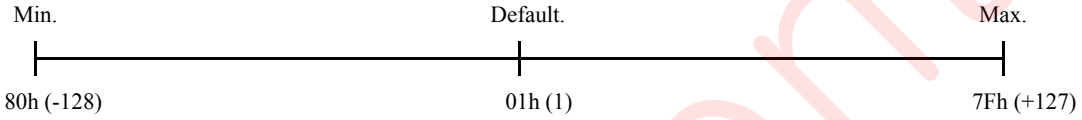
- Brightness / Y Contrast

-Related Registers : Brightness (Reg.B-25h), YContrast (Reg.B-24h)

Y *reault* = Y * (Ycontrast / 64) + Brightness

(1) Brightness

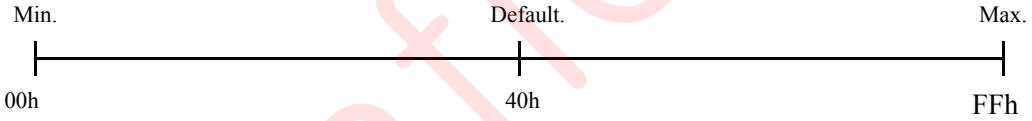
Brightness is controlled by *Brightness* register (*Reg.B-25h*). The default value of this register is 01h.



* Brightness : 2's compliment

(2) Y Contrast

Contrast is controlled by Y *Contrast* register (*Reg.B-24h*). The default value of this register is 40h.



- Color Correction Matrix

Related Registers : ColorMatrix11 (Reg.C-B9h) ~ ColorMatrix33 (Reg.C-C1h)

Color correction can be accomplished by color transform registers (*Reg.C-B9h ~ C-C1h*) by means of the following equation, where *CC* is 3x3 color correction matrix.

$$\begin{pmatrix} CT0 & CT1 & CT2 \\ CT3 & CT4 & CT5 \\ CT6 & CT7 & CT8 \end{pmatrix} = \begin{pmatrix} m00 & m01 & m02 \\ m10 & m11 & m12 \\ m20 & m21 & m22 \end{pmatrix} = 32 * CC$$

* m00 ~ m22 : (bit7) | (bit6 ~ bit0) = sign digit | magnitude

<Ex.>

$$\begin{pmatrix} m00 & m01 & m02 \\ m10 & m11 & m12 \\ m20 & m21 & m22 \end{pmatrix} = 32 * \begin{pmatrix} 1.7396 & -1.1444 & 0.4048 \\ -0.6039 & 1.4137 & 0.1902 \\ -0.1025 & -1.3094 & 2.4119 \end{pmatrix}$$

$$= \begin{pmatrix} 55.6672 & -36.6208 & 12.9536 \\ -19.3248 & 45.2384 & 6.0864 \\ -3.28 & -41.9008 & 77.1808 \end{pmatrix} = \begin{pmatrix} 38h & A5h & 0Dh \\ 93h & 2Dh & 06h \\ 83h & AAh & 4Dh \end{pmatrix}$$

- Sharpness Control

Related Registers : EdgeGain (Reg.B-2Eh), EdgeThreshold (Reg.B-2Fh)

Sharpness is controlled by *EdgeGain (Reg.B-2Eh)* and *EdgeThreshold* register *(Reg.B-2Fh).* All three values have the following Min. and Max. value.

$00h \leq EdgeGain \leq 3Fh$

$00h \leq EdgeThreshold \leq FFh$

The lowest sharpness level can be gotten by setting registers as follows.

EdgeGain = 00h, *EdgeThreshold* = FFh

And, the highest sharpness level can be gotten by setting registers as follows.

EdgeGain = 3Fh, *EdgeThreshold* = 00h

But, we recommend to set *EdgeThreshold* register value greater than 01h.

- Vertical / Horizontal Mirror

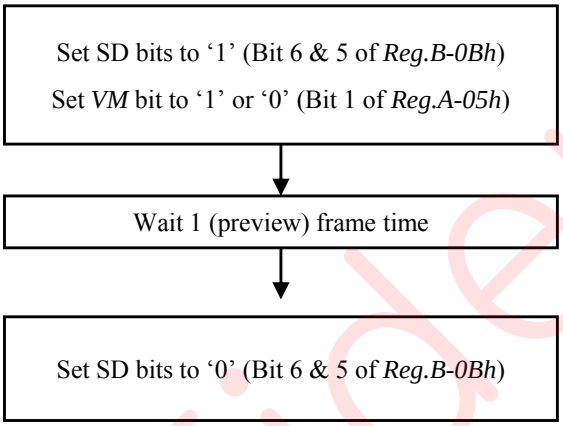
Related Registers : Mirror(Reg.A-05h), SyncControl0(Reg.B-0Bh). Related Strap pin : D6,D7.

Mirror mode can be set by not only writing registers directly but also controlling by strap pin as D6,D7.

Strap setting can be ignored after register setting has been changed by EEPROM and external i2c master.

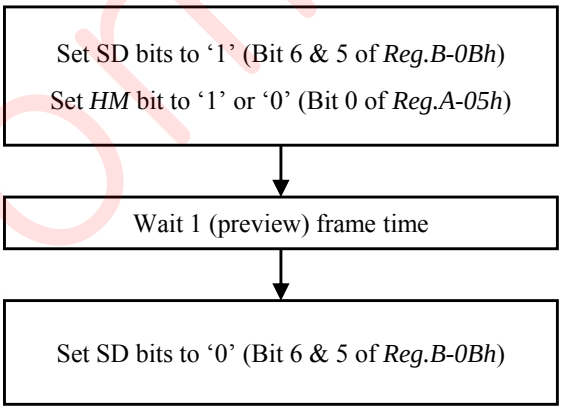
(1) Vertical Mirror

Vertical Mirror is controlled by *VM* bit (Bit 1 of *Reg.A-05h*).



(2) Horizontal Mirror

Horizontal Mirror is controlled by *HM* bit (Bit 0 of *Reg.A-05h*).



- Special Effect

(1) Color Effect

Related Registers : ISPControl2 (Reg.B-06h), CbTone (Reg.B-27h), CrTone (Reg.B-28h)

Reg. Addr. (Hex)	Setting value (Hex)	Register Name	Default Value (Hex)	Descriptions
B-06	**81**	*ISPControl2*	60	
B-27	***Appropriate Value***	*CbTone*	C0	
B-28	***Appropriate Value***	*CrTone*	40	

Sepia (Reg.B-27h : A0h, Reg.B-28h : 20h)

Green (Reg.B-27h : C0h, Reg.B-28h : C0h)

Aqua (Reg.B-27h : 20h, Reg.B-28h : C0h)

Red (Reg.B-27h : 00h, Reg.B-28h : 50h)

1/4 inch VGA class Analog/Digital Output NTSC/PAL CMOS Image Sensor

Cool (Reg.B-27h : 50h, Reg.B-28h : C0h)

Warm (Reg.B-27h : 90h, Reg.B-28h : 30h)

BW (Reg.B-27h : 00h, Reg.B-28h : 00h)

Antique (Reg.B-27h : 90h, Reg.B-28h : 10h)